Title of the Experiment:

Analysis of JK Flip Flop using eSim.

Theory :

This simple JK Flip Flop is the most widely used of all the Flip- Flop designs and is considered to be a universal input - output circuit. The JK Flip-Flop is basically a gated SR Flip- Flop with the addition of a clock input circuitry. It prevents the invalid output condition that can occur when both inputs S and R are equal to logic level 1. Due to this additional clocked input, a JK Flip-Flop has four possible input combinations, logic 1, logic 0, no change and toggle.

Schematic Diagram:

The circuit schematic of JK Flip-Flop in eSim is as shown below:

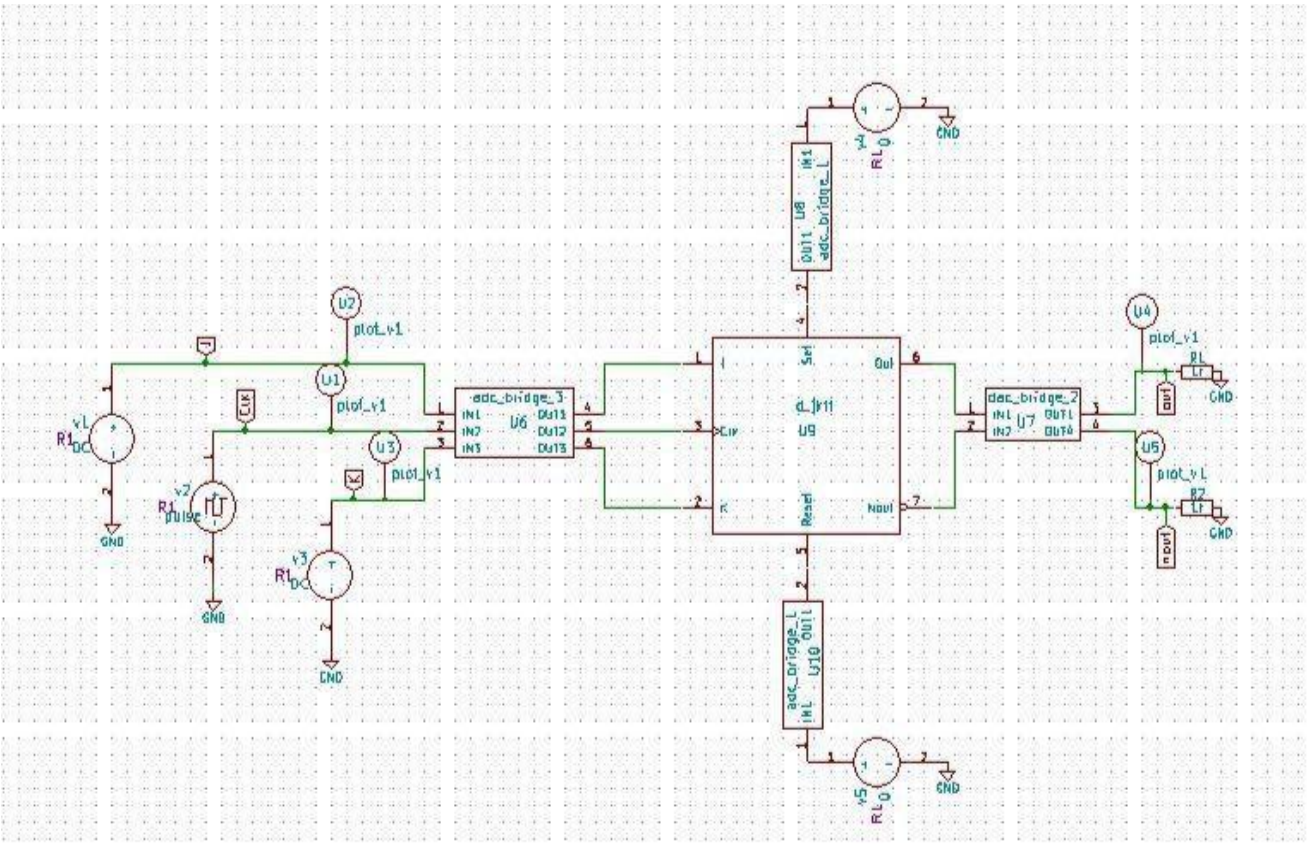

Figure 1: JK Flip-Flop using eSim

Simulation Results:

1. Python plots:

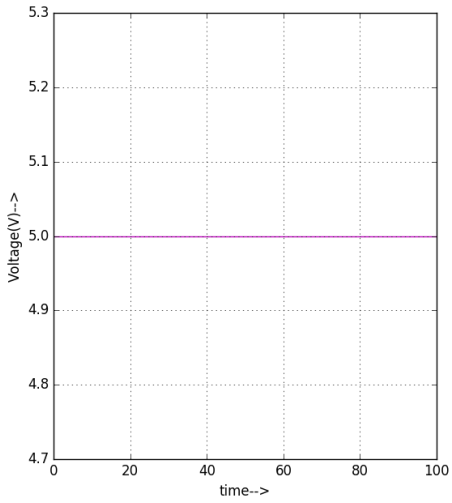

Figure 2: Out Plot

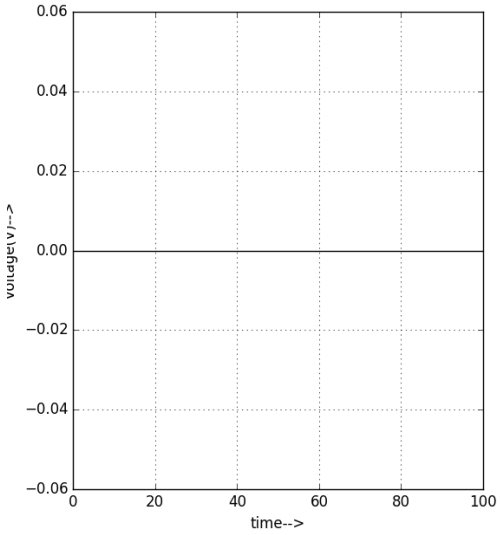

Figure 3: NOut Plot

2. Ngspice plots:

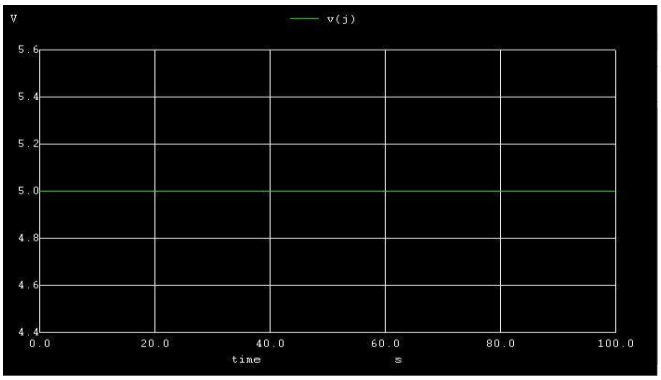

Figure 4: Ngspice Input-1 Plot

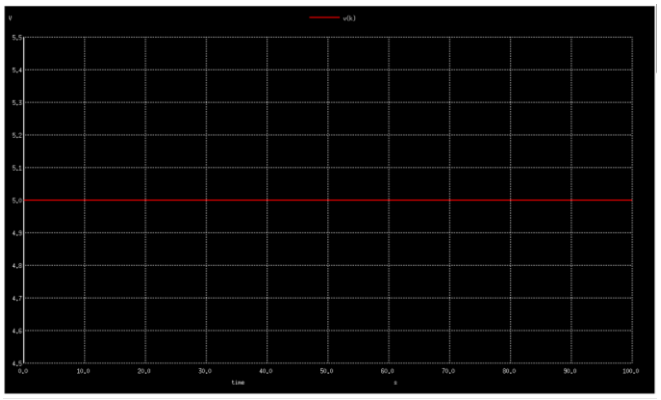

Figure 5: Ngspice Input-2 Plot

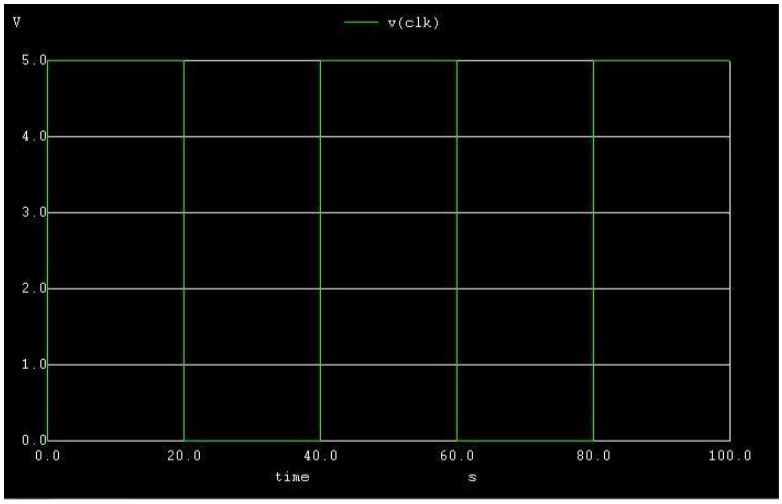

Figure 6: Ngspice Clock Input Plot

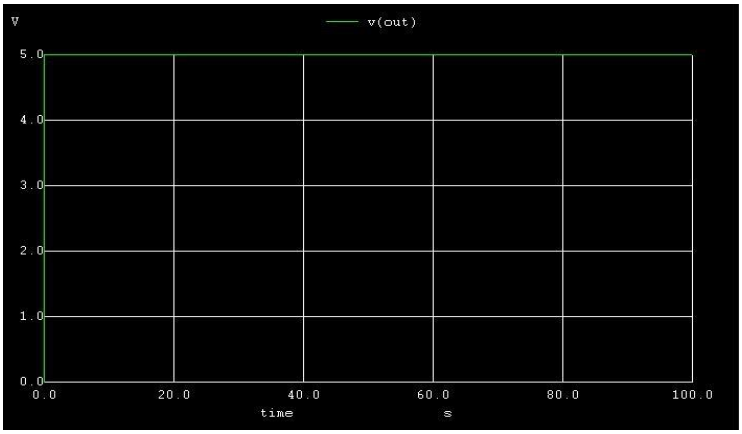

Figure 7: Ngspice Output-1 Plot

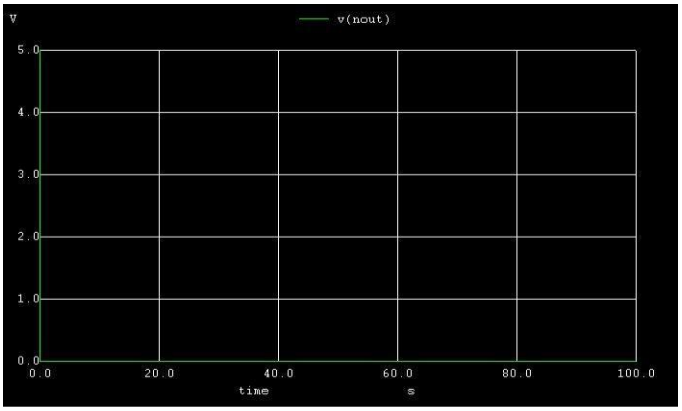

Figure 8: Ngspice Output-2 Plot

Reference:

[1] http://worldclassprogramme.com/JK-FlipFlop.php referred on 17/08/2017.