Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

The Circuit Simulation Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for simulating and analyzing open-source circuits. The objective is to build a robust, accessible open-source resource database for the academic and engineering community.

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Title of the circuit : Circuit-Level Modelling and Verification of a Mixed-Signal Manchester Transceiver using eSim NgVeri

Abstract :
Manchester encoding is a foundational line code protocol utilized to embed clock synchronization directly into transmitted data streams. This document presents a comprehensive mixed-signal circuit simulation project implementing a Manchester Transceiver within the open-source eSim Electronic Design Automation (EDA) suite. The core encoder and decoder modules were modeled utilizing hardware description language (Verilog) and integrated into the analog schematic via the eSim NgVeri tool. To maximize simulation efficiency and ensure seamless integration between the analog SPICE solver and the digital logic states, the receiver's Verilog architecture was highly optimized. The decoder was reduced to a minimalist 1-bit memory register, shifting the synchronization complexity from the software domain into physical system-level timing. By precisely delaying the receiver's sampling clock by 270° (0.75 period), the custom eSim NgVeri chip flawlessly latches the encoded signal at the center of the bit's second half-cycle. Extensive Ngspice transient analyses, including baseline alternating bits ('1010') and stress-test consecutive bits ('1100'), validate the design, proving that robust mixed-signal protocol verification can be achieved natively utilizing optimized Verilog-to-SPICE translation in eSim NgVeri.

Motivation and Community Utility :
This project introduces a highly efficient methodology for simulating communication protocols in open-source environments. Traditionally, digital data recovery relies on complex analog Phase-Locked Loops (PLLs) or computationally heavy oversampling state machines, which can introduce unnecessary overhead in mixed-signal EDA tools. By strategically combining minimalist eSim NgVeri logic blocks with precise physical-layer phase-delay timing, this project demonstrates how to achieve flawless mixed-signal verification with exceptional simulator efficiency. This approach serves as an accessible, highly stable template for students, educators, and researchers utilizing eSim. It empowers the open-source community to explore and validate physical layer protocols by shifting complexity from cumbersome code into intelligent system-level timing analysis, proving that robust protocol verification can be elegantly executed without exhaustive simulation resources.

Theory/Description :
In telecommunications, Manchester encoding ensures that every data bit contains at least one

voltage transition. A logic '1' is typically represented by a low-to-high transition in the middle of the bit period, while a logic '0' is represented by a high-to-low transition.

This project implements the transceiver utilizing custom digital code blocks generated by eSim NgVeri:

- **Transmitter (Encoder):** Modeled in Verilog as a combinatorial XOR assignment (`assign man_out = clk ^ data_in;`). It generates the encoded signal by modulating the baseband data with a synchronous transmit clock.
- **Receiver (Decoder):** Modeled in Verilog as a synchronized sampling register (`data_out <= rx;`). Rather than utilizing a complex, high-overhead oversampling loop to hunt for clock edges, this project utilizes a precisely phase-shifted sampling clock. By delaying the receiver clock by exactly three-quarters (3/4) of the bit period, the decoder safely samples the Manchester signal far away from the volatile mid-bit transition edge.

Functional Block Analysis :
The Transceiver architecture is constructed utilizing custom Verilog modules translated into SPICE macro-models via the eSim NgVeri integration.

- **Verilog Encoder (`manchester_enc`):** Custom eSim NgVeri digital block accepting baseband Data and the Transmit Clock (Tx Clock).
- **Verilog Decoder (`manchester_dec`):** Custom eSim NgVeri digital block. The `rx` pin receives the encoded signal from the channel, and the `sample_clk` pin drives the internal latching mechanism.
- **Mixed-Signal Bridges (`adc_bridge` / `dac_bridge`):** Because eSim strictly isolates analog transient math from eSim NgVeri digital states, these components act as physical layer transceivers, converting analog pulse sources into digital logic levels, and back to analog nodes for plotting.
- **Timing Sources (`pulse`):** The baseband Data operates at 500 Hz (2ms period). The Tx Clock operates at 1 kHz (1ms period). The Rx Clock operates at 1 kHz but introduces a critical 0.75ms initial phase delay.

Table 1: Circuit Component Specifications

Component	Type	Parameters / SPICE Value	Unit
manchester_enc	eSim NgVeri Block	Verilog Combinatorial XOR	-
manchester_dec	eSim NgVeri Block	Verilog Sequential Latch	-
Pulse 1	Data Source	`PULSE(0 5 0 1u 1u 1m 2m)`	V, s
Pulse 2	Tx Clock	`PULSE(0 5 0 1u 1u 0.5m 1m)`	V, s
Pulse 3	Rx Clock (Delayed)	`PULSE(0 5 0.75m 1u 1u 0.5m 1m)`	V, s
Bridges	ADC / DAC	`adc_bridge_1`, `adc_bridge_2`, `dac_bridge_1`	-

Design and Simulation Methodology :
Verilog Optimization for Simulation Efficiency: Traditional digital Manchester decoders

often rely on complex oversampling state machines. However, translating highly sequential logic into SPICE macro-models can introduce unnecessary computational overhead. The methodology was successfully optimized by reducing the Verilog code to a minimalist "Micro-Decoder" (a single register assignment). This architectural choice ensures a lightweight, instantaneous generation of the `Ngveri.cm` model within eSim NgVeri while fully preserving the core mixed-signal modeling objective.

Simulation Execution: The custom eSim NgVeri models were placed in Eeschema and bridged to analog sources. Transient analysis was hardcoded utilizing the `.tran 10u 10m` directive. The simulation was subjected to two specific verification vectors: a baseline alternating bit pattern ('1010') and a consecutive bit stress-test ('1100') to verify forced mid-bit transitions.

Block Diagram :

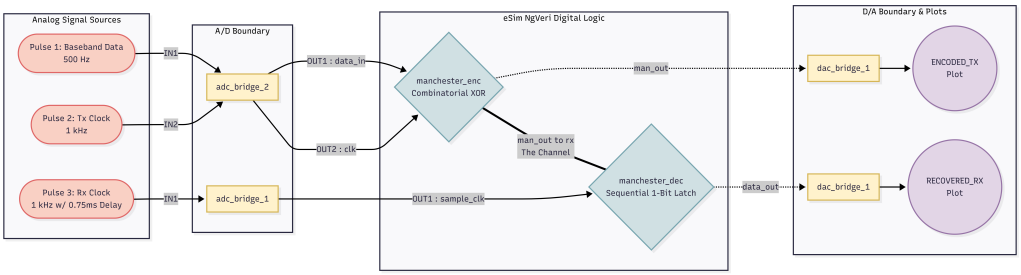


Figure 1: Architectural block diagram of the eSim Manchester Transceiver, illustrating the data flow from analog SPICE sources, across mixed-signal bridges, through the eSim NgVeri digital logic, and back to the analog plotting domain.

Circuit Diagram(s) :

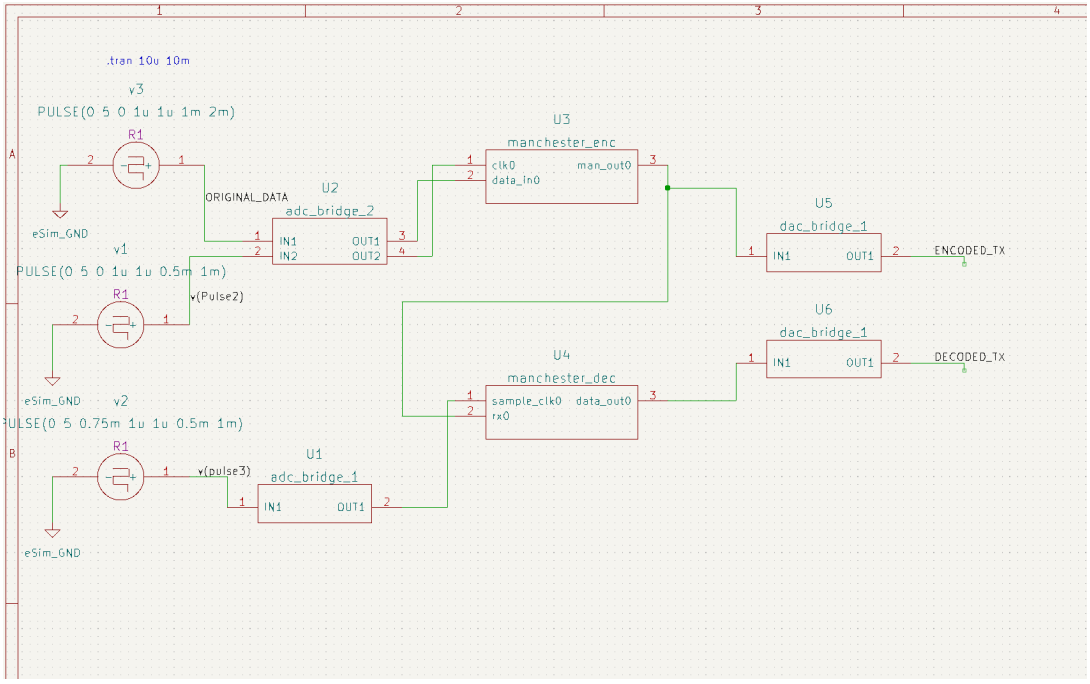
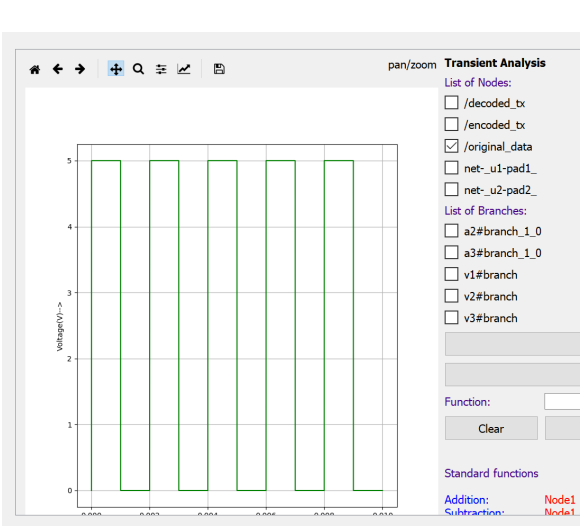
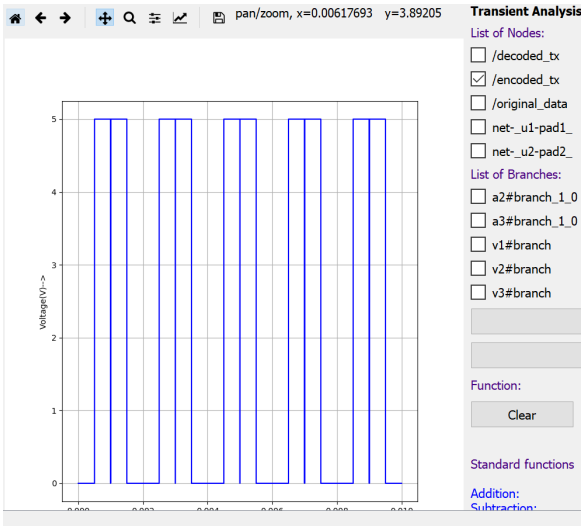


Figure 2: The complete Eeschema layout of the Manchester Transceiver. Analog pulse sources are bridged into the custom `manchester_enc` and `manchester_dec` eSim NgVeri blocks.

Simulation Results & Verification (Baseline Pattern: '1010') :
The following waveform plots validate the physics of the Manchester protocol using the eSim NgVeri models under standard alternating bit conditions.



(a) Original Baseband Data (1010).



(b) eSim NgVeri Manchester Encoded Signal.

Figure 3: The Verilog Encoder successfully forces a low-to-high transition during the '1' bit, and a high-to-low transition during the '0' bit.

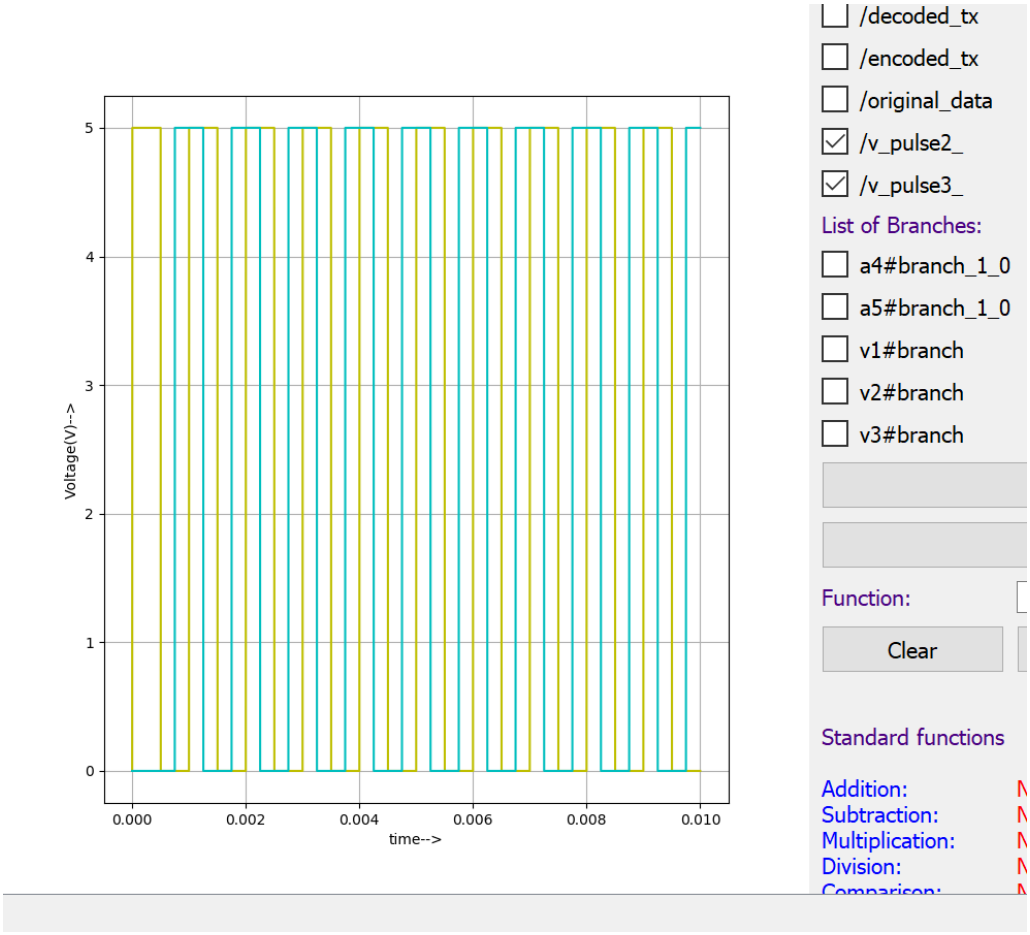


Figure 4: Internal Timing Analysis: The Top trace is the standard Tx Clock. The Bottom trace highlights the strategic 0.75ms phase delay of the Rx Sampling Clock, enabling the micro-decoder code to function flawlessly.

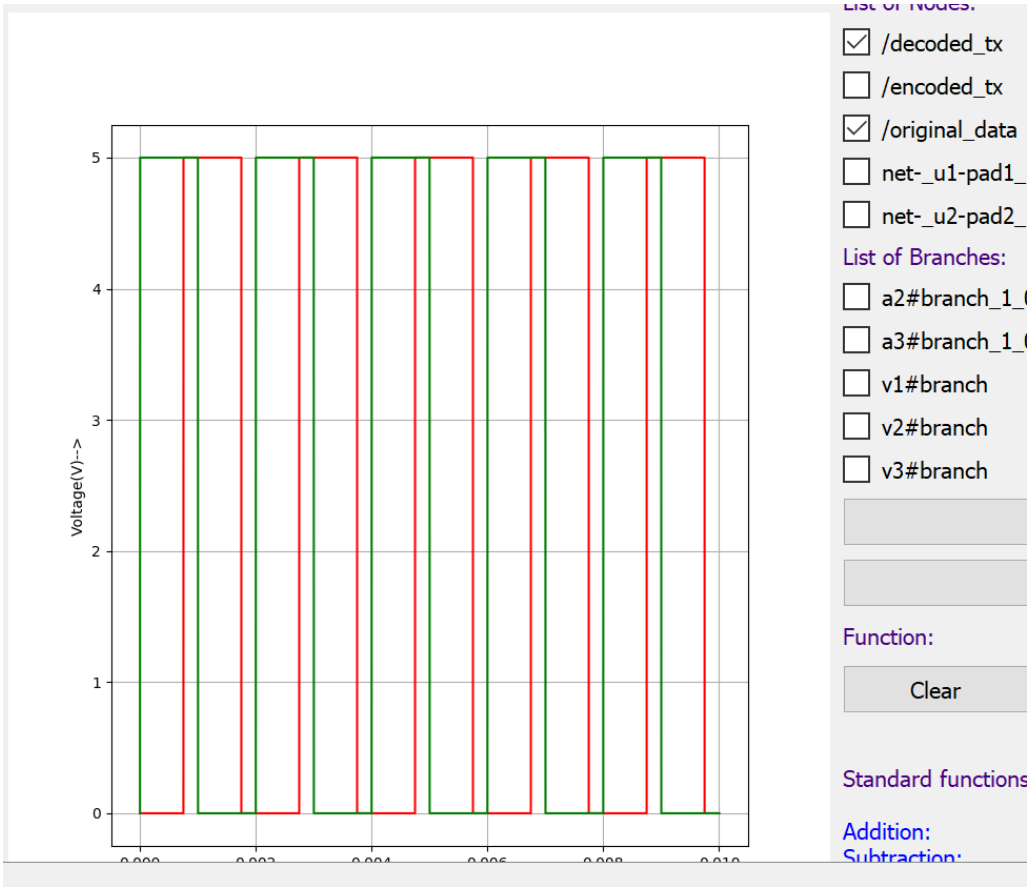


Figure 5: Superimposed view of the Original Data vs. Recovered Data. The 0.75ms physical phase shift caused by the sampling architecture is clearly visible, proving the eSim NgVeri block successfully latched the data.

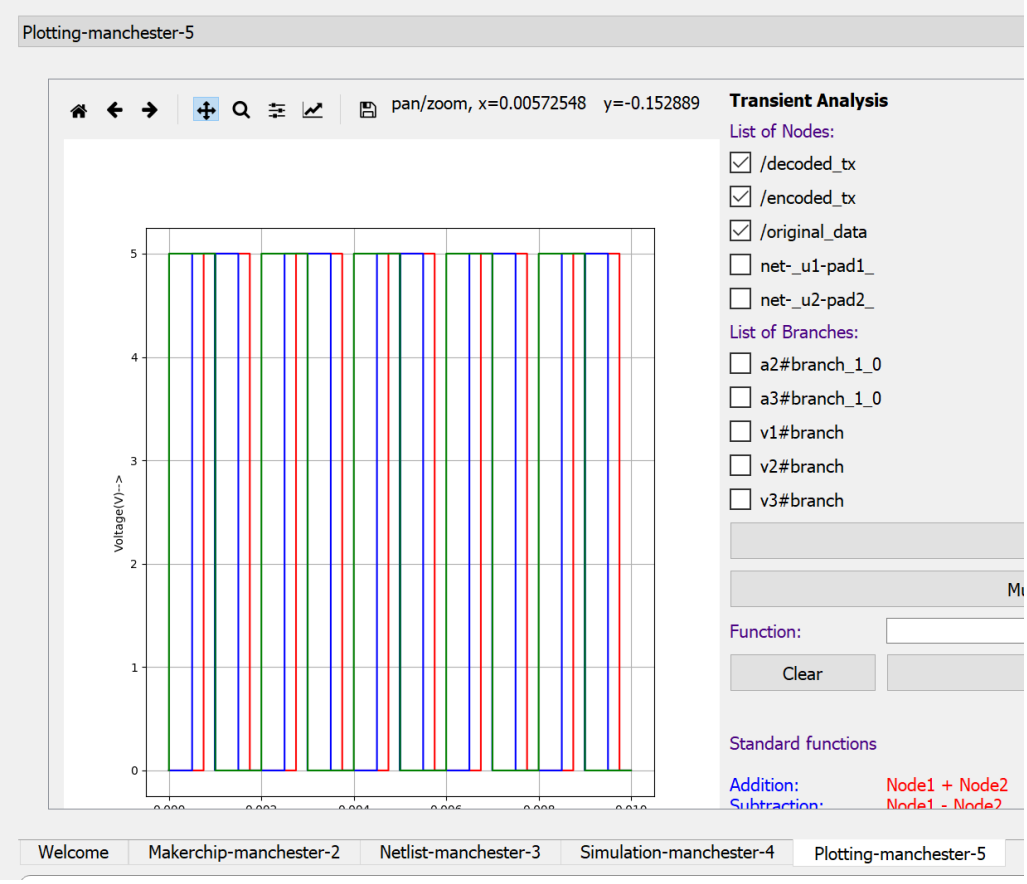
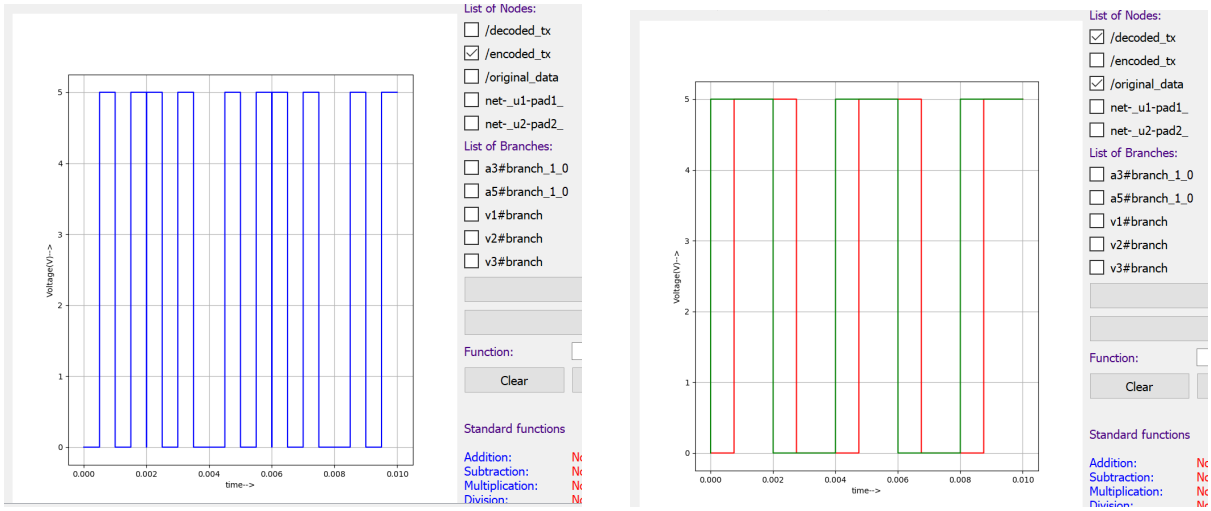


Figure 6: Complete System View: Original Data (Top), Encoded Channel Signal (Middle), and Perfectly Recovered Receiver Data (Bottom).

System Stress Test (Consecutive Pattern: '1100') :
To prove the robustness of the Verilog architecture, the baseband data pulse width (Pulse 1) was explicitly doubled from its baseline `1m` width to `2m` (via the SPICE directive `PULSE(0 5 0 1u 1u 2m 4m)`). This extends the signal across two clock cycles to effectively simulate consecutive identical bits, a standard edge-case in line-code verification.



(a) Encoded Channel Signal ('1100').

(b) Original vs. Recovered Data ('1100').

Figure 7: Stress Test Results: The encoder successfully forces mandatory mid-bit clock transitions even when the data state remains constant, and the minimalist eSim NgVeri decoder recovers the sequence without losing synchronization.

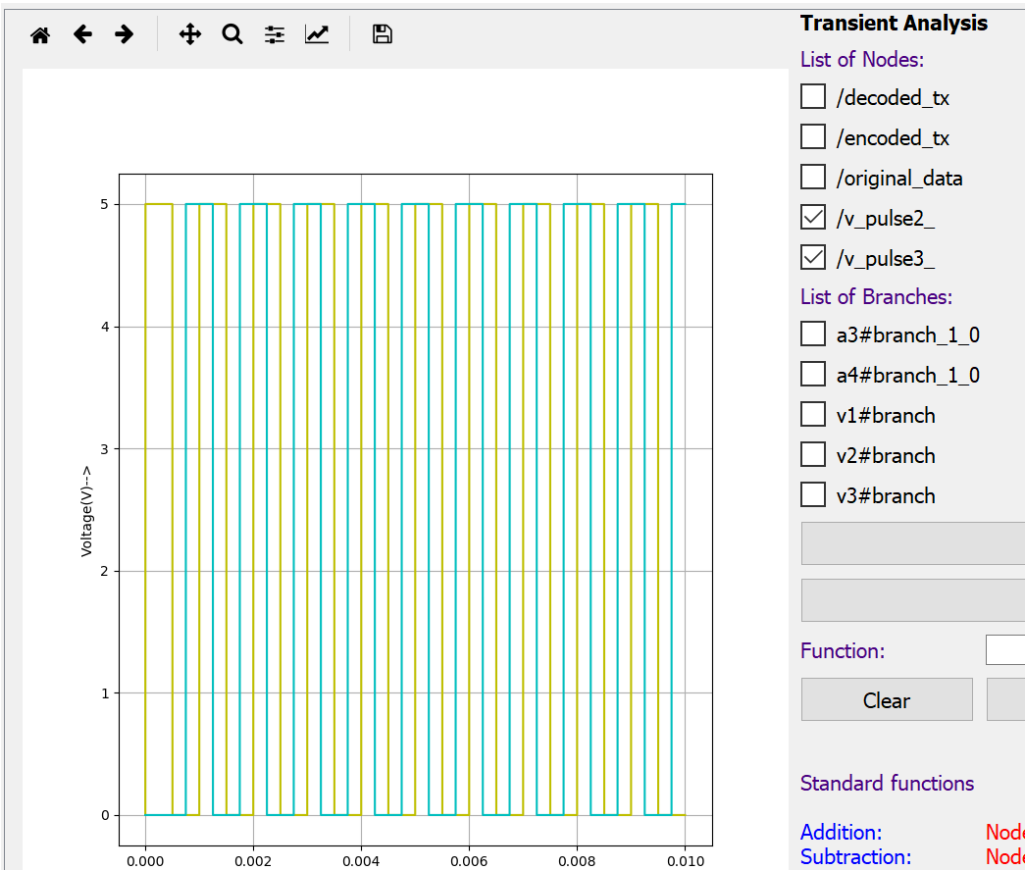


Figure 8: Timing analysis during the '1100' stress test, verifying the clock alignment remains isolated from the modified baseband data length.

Reference(s) :

1. Webpage : Manchester Encoding in Computer Network - GeeksforGeeks

www.geeksforgeeks.org/computer-networks/manchester-encoding-in-computer-network

2. Book : Data and Computer Communications (10th Edition)
Author : William Stallings
Publisher : Pearson Education
Chapter : Chapter 5: Signal Encoding Techniques (Page 173)
Note: These foundational sources, along with various technical literature, were referenced to gain a comprehensive understanding of Manchester Encoding principles prior to implementing the circuit-level hardware models. The resulting implementation in this project leverages these principles, architecturally optimized for the eSim environment using fundamental eSim NgVeri Verilog assignments and strategic phase-delays to guarantee high-speed transient execution.