Circuit-Level Modelling and Verification of Manchester Encoding and Decoding Protocol.

1. Introduction

In digital telecommunications, Manchester Encoding (also known as Phase Encoding) is a line code in which the encoding of each data bit has at least one transition and occupies the same time. Unlike standard binary signaling, the logic state is determined by the direction of the transition (high-to-low or low-to-high). This makes the signal "self-clocking," meaning a clock signal can be recovered from the data stream, which is vital for synchronization in systems like Ethernet (IEEE 802.3) and RFID.

2. Problem Statement

Standard digital transmission (Non-Return-to-Zero) faces two major challenges:

- Synchronization Loss: If a long string of zeros or ones is sent, the receiver can lose track of the clock timing.
- DC Bias: Continuous high signals create a DC component that can damage certain transmission hardware.
- There is a need to model a robust circuit-level system that combines data and clock into a single transmission line and successfully reconstructs the original data at the receiver end.

3. Objectives

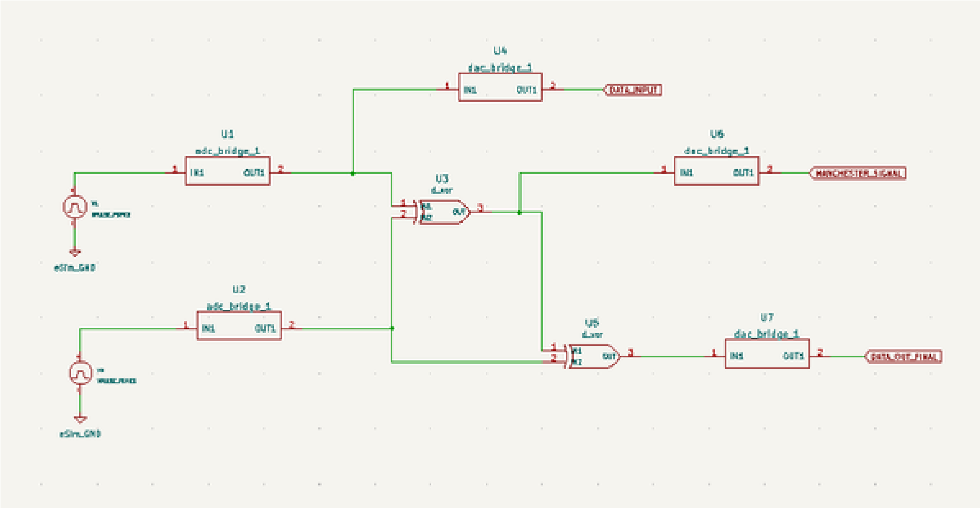
The primary objectives of this project are:

- To design a Manchester Encoder (Transmitter) and Decoder (Receiver) using digital logic gates in eSim v2.5.
- To implement a mixed-signal simulation environment using ADC and DAC bridges to interface analog sources with digital components.
- To verify the protocol through Transient Analysis by comparing the input data stream with the final recovered output.

4. Methodology

The project was executed following these steps:

- Schematic Design: Using eSim's KiCad interface to place XOR gates, pulse sources, and ground symbols.
- Hybrid Modeling: Incorporating adc_bridge components to convert analog pulse voltages into digital logic for the XOR gates, and dac_bridge components to convert digital outputs back into analog voltages for plotting.
- Parameter Configuration: Setting up pulse widths and periods for the Clock (1ms) and Data (8ms) to ensure a clear distinction during simulation.
- Netlist Generation: Converting the KiCad schematic into an Ngspice-compatible netlist (.cir).
- Simulation: Running a Transient Analysis for 20ms to capture multiple data cycles.
- Verification: Using the Python Plotting tool to visualize and compare data_input, manchester_signal, and data_out_final.

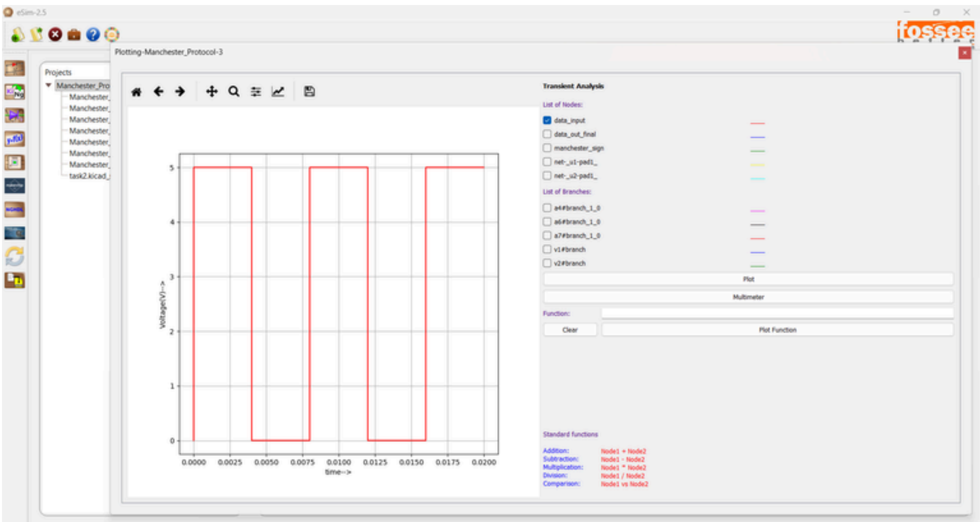


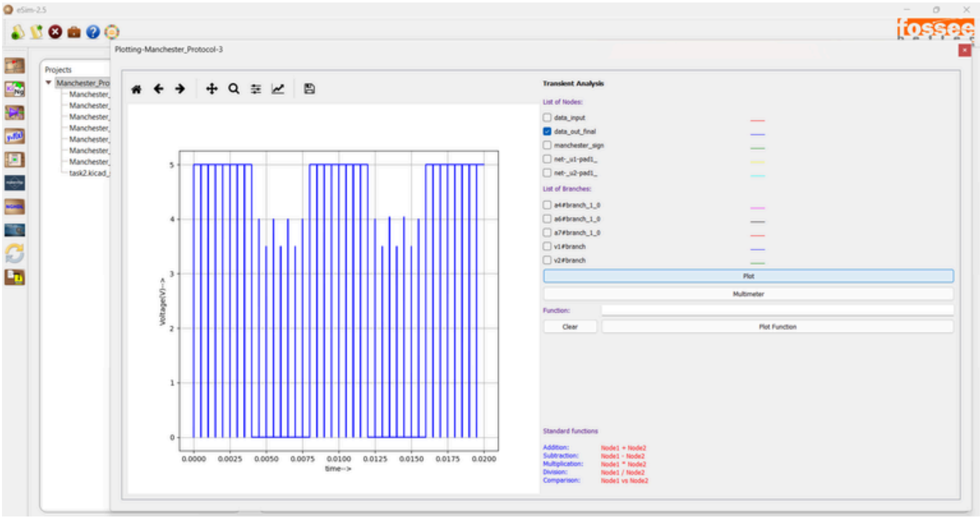
5. Circuit Explanation

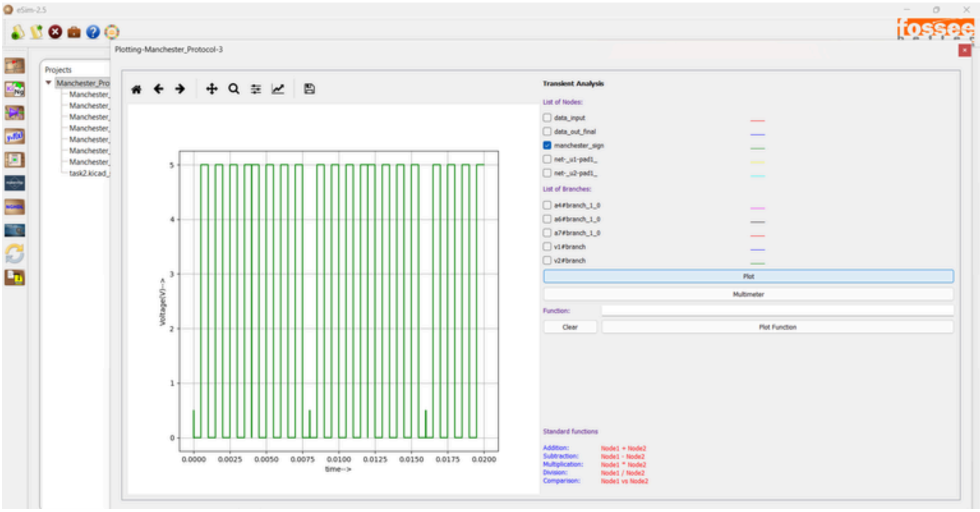
The circuit operates on the fundamental XOR (Exclusive OR) logic:

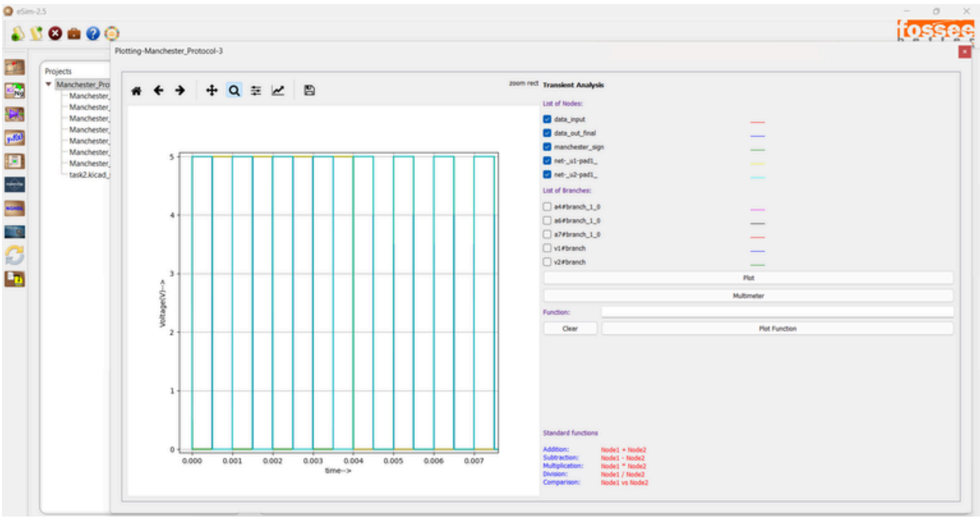
- Transmitter (Encoder):
- The Encoder takes two inputs: Digital Data and Synchronization Clock.
    - Logic:
    - Data⊕Clock=Manchester_OutputData⊕Clock=Manchester_Output
    - .
    - When the clock is high, the data is inverted. When the clock is low, the data remains unchanged. This ensures a transition occurs in the middle of every bit, creating the Manchester encoded signal.
- Transmission Channel:
- The encoded signal represents a single-wire communication line where the clock is "embedded" within the data.
- Receiver (Decoder):
- The Decoder extracts the original data by performing a second XOR operation using the shared synchronization clock.
    - Logic:
    - Manchester_Output⊕Clock=Original_DataManchester_Output⊕Clock=Original_Data
    - .
    - This inverse operation strips away the clock transitions, leaving the original binary logic levels.
- Bridges (ADC/DAC):
- Because XOR gates in eSim are digital models, the ADC Bridges act as translators for the input pulses. The DAC Bridges act as voltmeters that allow the digital results to be displayed as 0V-5V waveforms in the final plots.

6. Simulation









7. References

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- FOSSEE Project. eSim User Manual. IIT Bombay. https://esim.fossee.in/.
- IEEE Standard 802.3. Ethernet Working Group. (Standardized use of Manchester Encoding in 10BASE-T).
- Mano, M. M. (2017). Digital Design. Pearson. (XOR Logic gate applications in communication).

8. Conclusion

The Manchester Encoding and Decoding protocol was successfully modeled and verified using eSim v2.5. The simulation results accurately demonstrated that a digital message can be encoded and transmitted over a single line and then fully recovered at the receiver. By comparing the input and output waveforms, the data integrity was confirmed, and the protocol's self-clocking nature was verified at the circuit level. This project successfully demonstrates eSim's capability in modeling mixed-signal communication systems and meeting the technical requirements of the research task.