Title of the experiment:

Simulation Of A Digital Dice Circuit Using 555 Timer And Cd4017 Decade Counter

Theory:

A digital dice circuit serves as an electronic alternative to traditional physical dice, offering the advantage that it cannot be biased or physically distorted over time. This mixed-signal circuit is primarily constructed using a 555 timer IC and a CD4017 decade counter IC.

The analog stage utilizes the 555 timer configured in astable mode to generate a continuous, high-frequency square wave clock pulse. Through an Analog-to-Digital (ADC) bridge, this oscillated output is applied directly to the clock input (PIN 14) of the 4017 IC. The CD4017 operates as a digital sequencer, advancing its HIGH output to the next pin with every incoming clock pulse.

To represent the six faces of a die, six LEDs are connected to the first six outputs (Q0 to Q5) of the counter. To restrict the sequence to exactly six states, the seventh output (Q6) is wired directly back to the RESET PIN 15. This modulo-6 logic loop ensures that after the sixth LED illuminates, the sequence instantly restarts at the first LED. The oscillation frequency of the 555 timer is deliberately set high enough so the rapid flashing of the LEDs prevents anyone from predicting or cheating the final outcome.

Simulation of Human Interaction: In a physical hardware implementation, true randomization is achieved through the unpredictable duration of a human button-press, and removing power would turn off the entire circuit. To replicate this interaction within an Ngspice transient analysis, the physical switch is bypassed, and the main DC power supply is modeled as a Pulsed Voltage Source: PULSE(0 9 0 1u 1u 0.73 10). This applies an instantaneous 5V to the analog 555 timer for exactly 730 milliseconds, representing a specific, deterministic human interaction window (Δ t).

Furthermore, it is critical to note the behavioral nature of XSpice mixed-signal modeling. The CD4017 and ADC/DAC bridges are event-driven digital models without physical analog power rails. When the 5V pulse drops to 0V, only the analog 555 timer halts. The digital counter receives no further clock edges and latches onto its final logic state. The DAC bridge continuously translates this latched digital state into an analog 5V output, accurately allowing us to visualize the final "rolled" state on the indicator LEDs

Schematic Diagram:

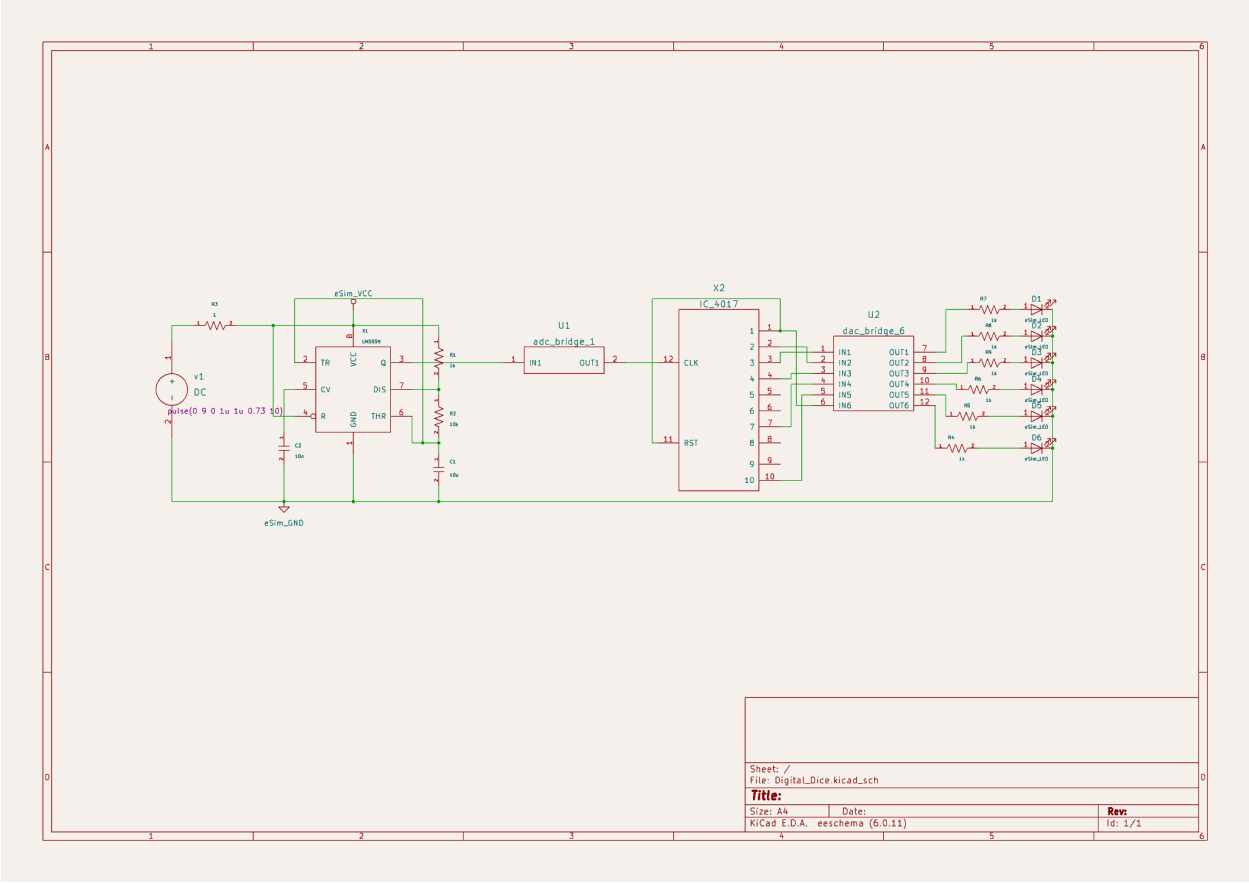
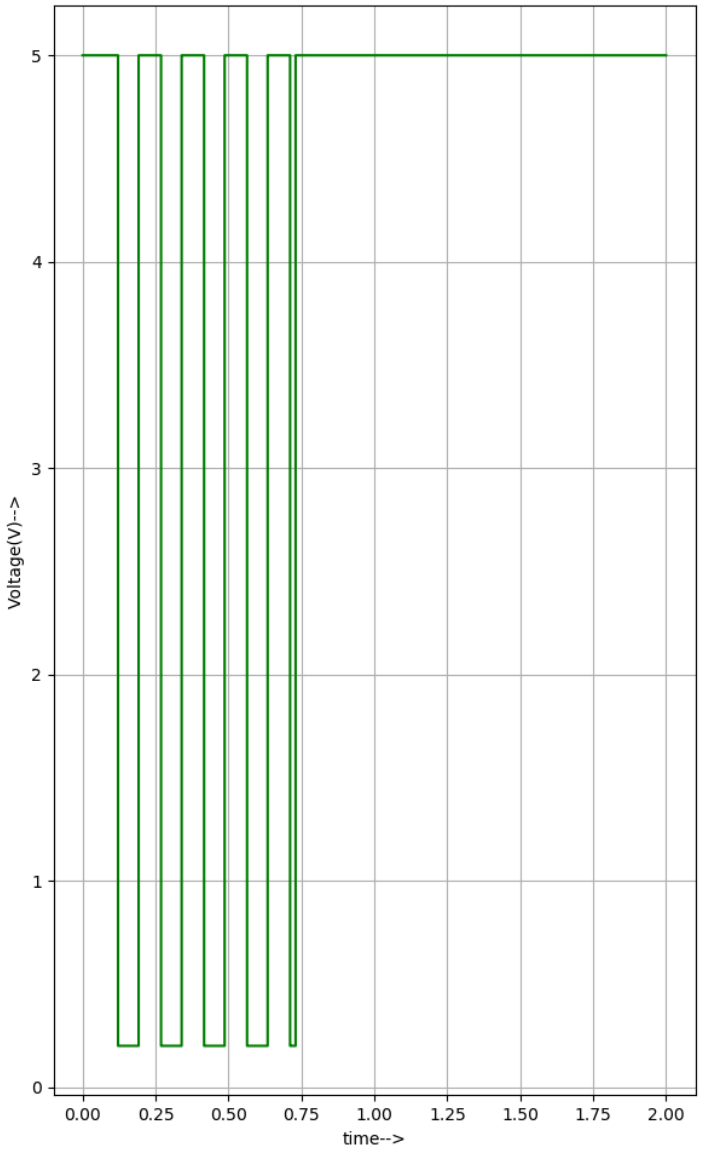


Figure 1: Mixed-signal schematic of the Digital Dice featuring LM555N and CD4017.

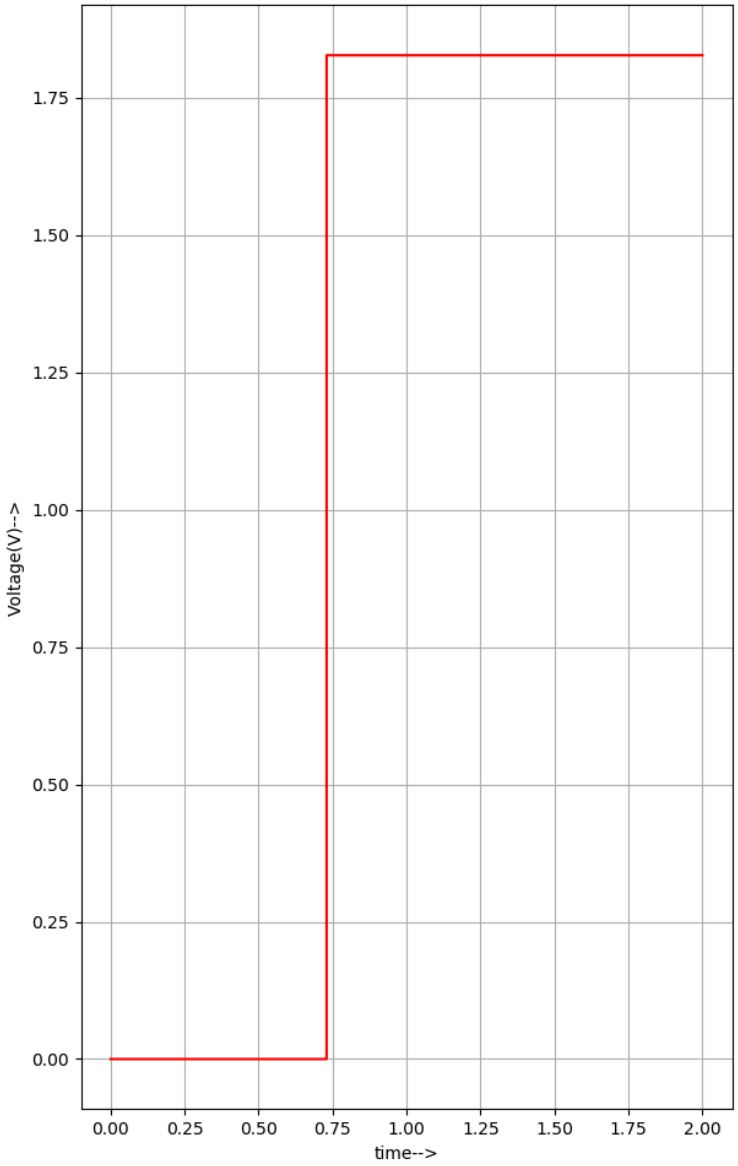
Simulation Results:

1. Ngspice / Python Plots



Plot 1: 555 Timer Clock Generation (Node: 555_Output).

Figure 2: Plot illustrating the astable multivibrator clock pulses during the 730ms power-on phase.



Plot 2: Final LED State and Forward Voltage (Node: LED_Anode).

Figure 3: Plot illustrating the sequential logic shift and the final randomized resting state of the LEDs.

Detailed Analysis of Results

1. Astable Multivibrator Clock Output (Reference: Plot 1)

The LM555N timer is configured in astable mode to serve as the clock generator. The theoretical oscillation frequency is determined by the timing components: R_1 = 1k ohms, R_2 = 10k ohms, and C_1 = 10 µF. Using the standard astable frequency formula f = 1.44 / ((R_1 + 2R_2) . C_1), the theoretical frequency is 1.44 / (21,000. 10µF) ≈ 6.86 Hz.

This yields a time period (T) of approximately 145 ms per pulse. The simulator applies a 5V power pulse for exactly 730 ms. Mathematically, 730 ms/ 145 ms ≈ 5.03 cycles. As observed in Plot 1, the simulator accurately outputs exactly 5 complete clock pulses peaking at the 5V supply limit before power drops to 0V, perfectly validating the theoretical RC time constant calculations.

2. Modulo-6 Logic and LED Forward Voltage (Reference: Plot 2)

Plot 2 captures the transient voltage across one of the output LEDs after the signal is translated back to the analog domain via the dac_bridge (configured with out_high=5.0). Before t = 0.73 s, the LED is briefly pulsed as the counter cycles. At exactly t = 0.73 s, the 555 clock halts, freezing the CD4017 counter. The plot demonstrates the counter locking into its final state, sending a latched HIGH logic signal to this specific LED.

The graph verifies that the signal stabilizes at approximately 1.85 V. The signal does not reach the full 5V bridge output; rather, it accurately reflects the characteristic forward voltage drop (V_f) of a standard Red LED model in SPICE. The remaining voltage (5 V - 1.85 V = 3.15 V) is dropped across the 1k\Omega current-limiting resistor. Using Ohm's Law (I = V/R), this demonstrates a safe continuous LED driving current of 3.15 mA. This analysis confirms both the successful modulo-6 operation of the digital sequencer and the mathematically sound analog modeling of the output load.

Conclusion :

Thus, we have successfully designed and simulated a mixed-signal Digital Dice circuit using eSim. By properly utilizing ADC and DAC bridges to isolate the digital counter, and by mathematically modeling human mechanical input through a pulsed voltage source, we verified the modulo-6 reset logic and obtained the appropriate cascading waveforms representing a randomized dice roll.

References:

1. eSim User Manual, FOSSEE, IIT Bombay.
2. Jayant, "Digital Dice Circuit using 555 Timer IC," Circuit Digest, Sept. 5, 2015.
3. Texas Instruments, "LM555 Timer Datasheet."
4. Texas Instruments, "CD4017B CMOS Counter/Divider Datasheet."