Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

The Circuit Simulation Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for simulating and analyzing open-source circuits. The objective is to build a robust, accessible open-source resource database for the academic and engineering community.

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Title of the circuit : 4-Stage Dickson Charge Pump using 180nm CMOS Technology

Abstract :
Charge Pumps are critical DC-DC converter circuits utilized to generate an output voltage significantly higher than the available supply voltage (V_{DD}), playing an essential role in low-voltage energy harvesting systems and integrated power management. This document presents a comprehensive circuit simulation project to design, parameterize, and simulate a 4-stage Dickson Charge Pump utilizing pure CMOS technology entirely within the open-source eSim electronic design automation (EDA) suite. Unlike legacy designs utilizing discrete diodes, this implementation employs diode-connected NMOS transistors carefully sized at W=10μm and L=180nm to minimize parasitic gate capacitance while maintaining optimal forward conduction. Two 1MHz anti-phase clocks (Φ and $\bar{\Phi}$) are capacitively coupled to the intermediate nodes via 10pF pumping capacitors to sequentially boost the voltage. Extensive Ngspice transient simulations validate the design, demonstrating successful capacitive voltage multiplication that overcomes inherent threshold (V_{th}) drops and progressive body-effect degradation to achieve a steady-state output of approximately 4.5V from a 1.8V DC input. By utilizing the generic 180nm CMOS device libraries natively bundled with eSim, this project demonstrates that professional-grade mixed-signal power management analysis can be achieved using entirely open-source platforms without relying on proprietary simulation tools.

Theory/Description :
A Charge Pump is a critical DC-DC converter circuit utilized to generate an output voltage significantly higher than the available supply voltage (V_{DD}). They are essential building blocks in modern integrated circuits, particularly for driving low-voltage analog systems, embedded sensors, or energy harvesting modules.

This project implements a foundational 4-stage Dickson Charge Pump utilizing pure CMOS technology. Unlike the original Dickson pump which used discrete diodes, this implementation uses diode-connected NMOS transistors (where the gate and drain are shorted). Two anti-phase, non-overlapping clocks (Φ and $\bar{\Phi}$) are capacitively coupled to the intermediate nodes of the NMOS chain. As the clocks alternate, charge is pushed sequentially from one stage to the next. While an ideal 4-stage pump with a 1.8V supply and 1.8V clocks would generate 9.0V, the practical output is limited by the threshold voltage (V_{th}) drops across each MOSFET and the progressive degradation caused by the body effect.

Functional Block Analysis :
The Dickson Charge Pump architecture is constructed from four highly interdependent functional sub-blocks.

- **Diode-Connected NMOS Chain (MD1–MD5):** Five NMOS transistors operating as unidirectional switches. They are explicitly sized at W=10μm and L=180nm to minimize parasitic gate capacitance (which would otherwise absorb the pumping charge) while maintaining sufficient forward current. The bulk pins are tied to ground, faithfully reproducing standard silicon substrate conditions and incorporating the real-world body effect into the simulation.
- **Pumping Capacitors (C_1–C_4):** These 10pF passive capacitors couple the 1.8V clock pulses into the intermediate nodes. At high frequencies (1MHz), they effectively bypass their own internal impedance to sequentially boost the voltage at each stage.
- **Output Smoothing Capacitor (C_{out}):** A 50pF capacitor that accumulates the final boosted charge and filters out the high-frequency clock switching noise to provide a steady DC output. The value is mathematically scaled against the equivalent resistance of the pump to ensure a visible and realistic charging time constant (τ) within the transient window.
- **Anti-Phase Clock Source:** Two 1MHz, 1.8V pulse sources provide the necessary voltage swing. Φ and $\bar{\Phi}$ operate with a pulse width of 0.5μs and are offset by a half-period (0.5μs) to drive the charge pump stages sequentially in anti-phase.

Table 1: Circuit Component Specifications (Native eSim 180nm Library)

Component	**Type**	**Parameters / Value**	**Unit**
MD1 – MD5	NMOS (Diode-Connected)	W = 10, L = 0.180 (CMOSN Level 8)	μm
C1 – C4	Pumping Capacitors	10	pF
Cout	Output Filter Capacitor	50	pF
V_in	Input DC Supply	1.8	V
Φ	Clock Source 1	1.8V Amp, 1MHz, $PW = 0.5\mu$s, $T_{delay} = 0$	V, Hz
$\bar{\Phi}$	Clock Source 2 (Inverted)	1.8V Amp, 1MHz, $PW = 0.5\mu$s, $T_{delay} = 0.5\mu$s	V, Hz

Design and Simulation Methodology :
Open-Source eSim Implementation: The Dickson Charge Pump serves as an excellent learning vehicle for exploring non-linear transient dynamics and parasitic behaviors in mixed-signal VLSI. While the original literature explores this using proprietary commercial tools, this project successfully designs and simulates the circuit completely within the open-source eSim environment. By utilizing the BSIM3v3.2 180nm CMOS library (`NMOS-180nm.lib`) provided natively with eSim, the project ensures 100% accessibility and reproducibility for the wider open-source community.

Simulation Execution: The design was captured natively in KiCad. The exported SPICE netlist was rigorously augmented to strictly govern the transient solver's initial conditions using the `.IC` directive (`.ic v(/v1)=0 v(/v2)=0...`). This prevents the Ngspice DC operating

point solver from prematurely charging the capacitors before the transient phase begins. The simulation utilizes a finely stepped `.TRAN 5e-09 500e-06` command to ensure the 1MHz clock edges are resolved with extreme mathematical accuracy.

Circuit Diagram(s) :

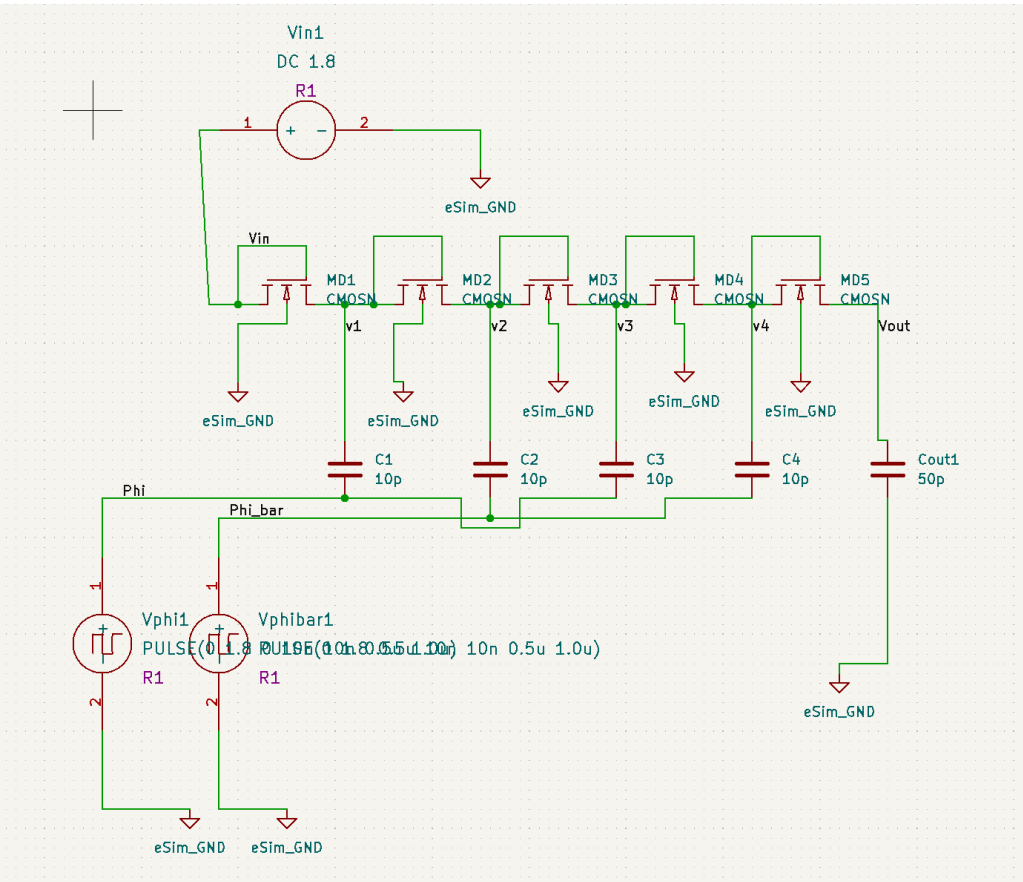
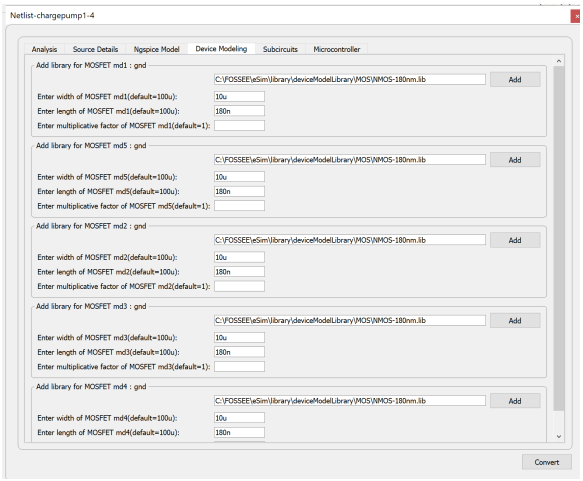
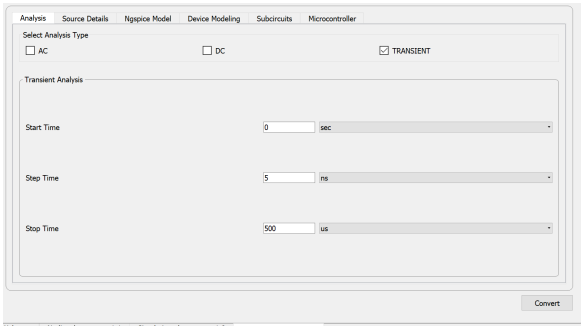


Figure 1: The complete eSim/KiCad schematic of the 4-stage Dickson Charge Pump, illustrating the diode-connected NMOS chain, alternating pumping capacitors, and automated simulation text block.



(a) Device Modeling configuration.



(b) Transient Analysis settings.

Figure 2: eSim GUI parameterization showcasing the 180nm model linking and strict $5ns$ transient step resolution required for 1MHz operation.

Block Diagram (s) :

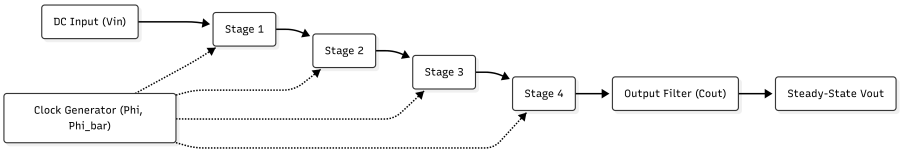
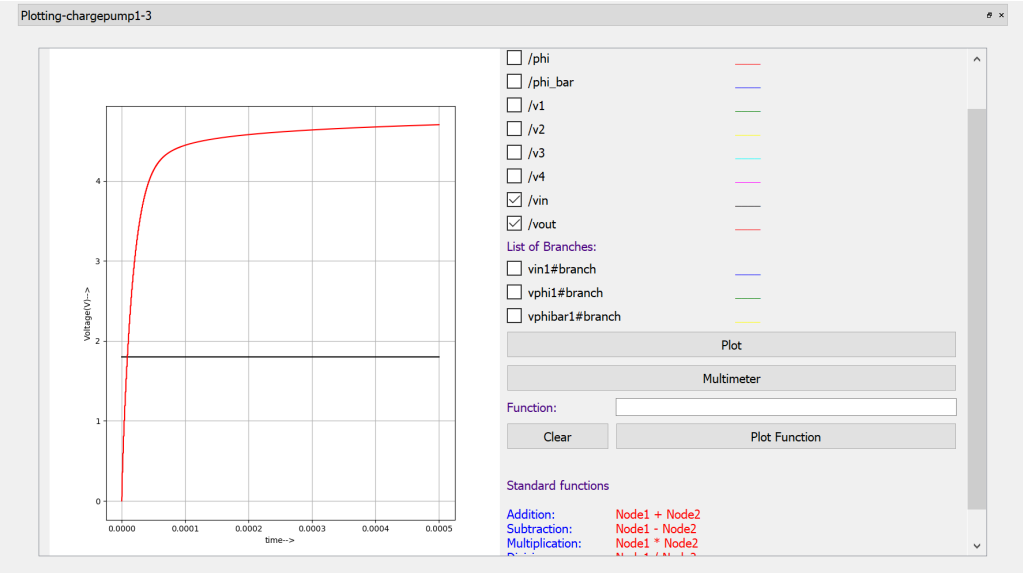
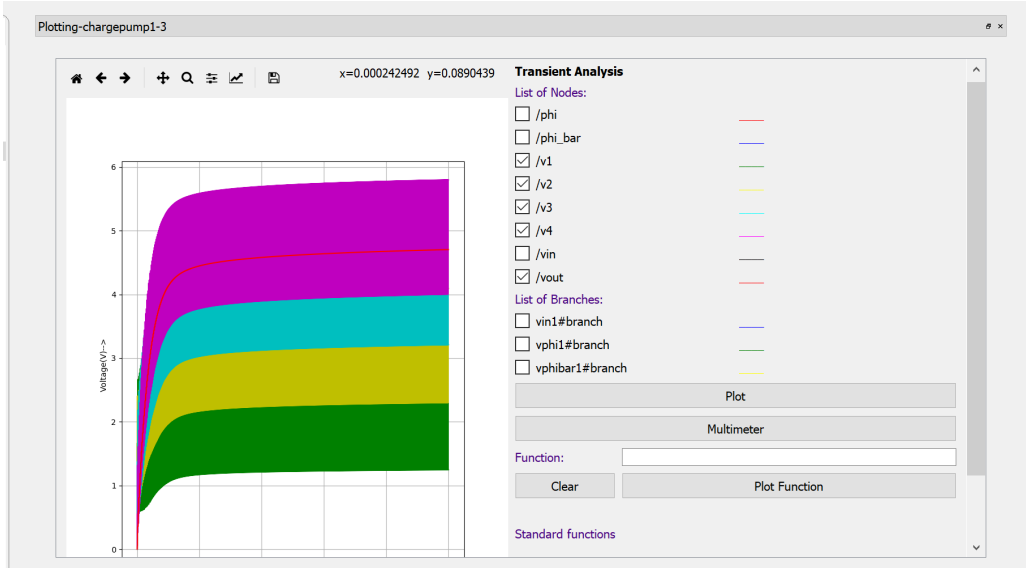


Figure 3: High-level architectural block diagram of the 4-stage Dickson Charge Pump showing the sequential voltage accumulation driven by the alternating clock phases.

Expected Results (Input, Output waveforms and/or Multimeter readings) :
The simulation demonstrates successful capacitive voltage multiplication, overcoming the inherent threshold drops of the NMOS chain. Expected graphical outputs generated via Ngspice include a primary voltage gain transient plot, a multiplier staircase plot, and high-resolution zoomed clock waveforms.
Inputs: DC Input Voltage (V_{in}) = 1.8V. Clock amplitude = 1.8V at 1MHz frequency. Internal nodes initialized to 0V.
Outputs: The transient analysis clearly validates the pumping action. The intermediate nodes display the expected staircase progression. The output voltage (V_{out}) charges the 50pF capacitor smoothly, reaching a steady-state DC voltage of approximately 4.5V, accompanied by the characteristic high-frequency switching ripple.



(a) The primary transient response showing V_{in} (1.8V) vs. V_{out} successfully settling at ≈4.5V.



(b) The internal node voltage progression demonstrating the multiplier staircase effect.

Figure 4: Ngspice simulation results showing the sequential charge accumulation and steady-state output.

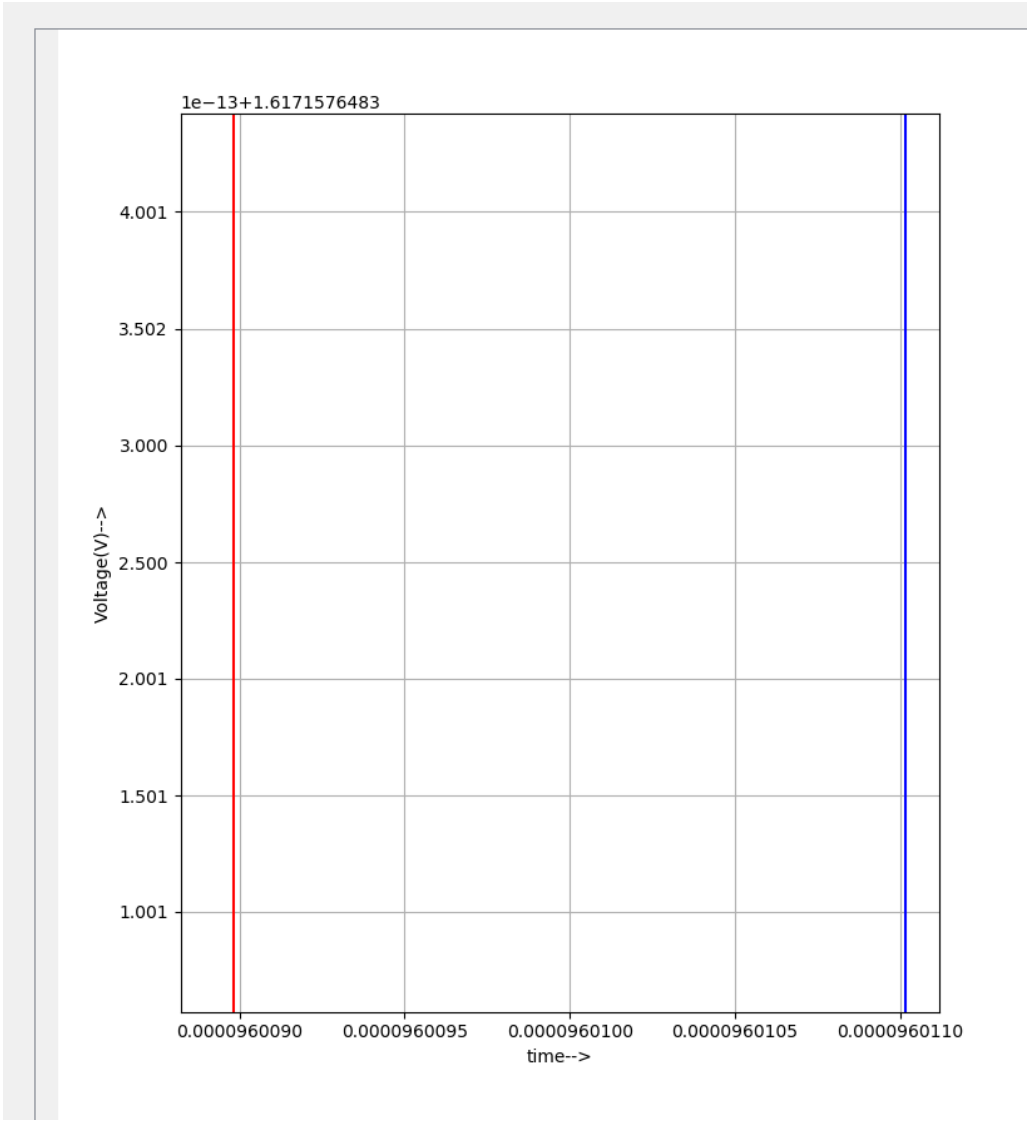


Figure 5: Zoomed verification of the 1MHz anti-phase clocks (Φ and $\bar{\Phi}$).

Research Paper/Journal/etc. :
Title : Analysis and design of dickson charge pump for EEPROM in 180nm CMOS technology
Author : M. El Alaoui, F. Farah, K. El Khadiri, H. Qjidaa, A. Aarab, R. El Alami
Journal : 2018 International Conference on Intelligent Systems and Computer Vision (ISCV), Fez, Morocco
Page No. : 1-5
DOI : https://doi.org/10.1109/ISACV.2018.8354067

Source/Reference(s) :

• T. Chien, "Charge Pumps: An Overview," Electrical Engineering review, University of Toronto.