FOSSEE IIT BOMBAY

Circuit Simulation Project

Mixed-Signal ASK Communication System

LFSR-Based Pseudo-Random Data Generation with Envelope Detection Receiver

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1.Theory and System Description

1.1 Amplitude Shift Keying (ASK) Fundamentals

Core Technology Amplitude Shift Keying (ASK) is a digital modulation technique where the amplitude of a carrier signal is varied in accordance with the digital data signal. This project implements a complete end-to-end ASK communication system with innovative pseudo-random data generation.

$$s(t) = A_c x m(t) x \sin(2 f_c t +)$$

$$\text{where: } A_c = 5V, f_c = 100kHz, m(t) \{0, 1\}$$

1.2 LFSR-Based Data Generator (Innovation)

Key Innovation Unlike conventional implementations using fixed 101010 patterns, this project employs a 4-bit Linear Feedback Shift Register (LFSR) with primitive polynomial $x^4 + x^3 + 1$ for generating realistic pseudo-random data sequences.

Figure 1: 4-Bit LFSR Implementation

Feedback Polynomial: $P(x) = x^4 + x^3 + 1$ (Primitive)

TECHNICAL SPECIFICATIONS - LFSR

Characteristic Polynomial:	$x^4 + x^3 + 1$
Maximum Sequence Length:	$2^4 - 1 = 15$ states
Feedback Logic:	D3 XOR D2
Bit Period (Configurable):	200 s (5 kbps)

1.3 Complete System Architecture

Figure 2: Complete ASK Communication System Block Diagram

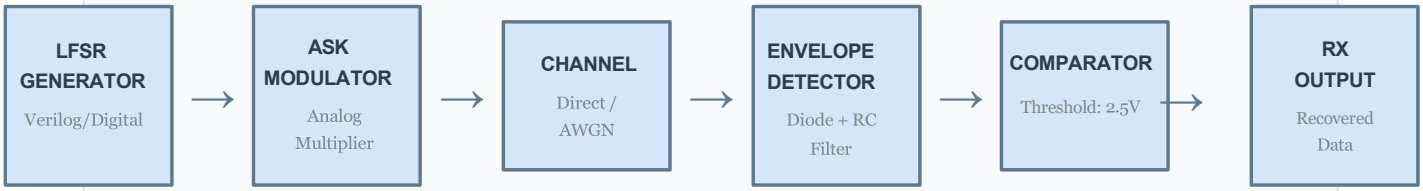
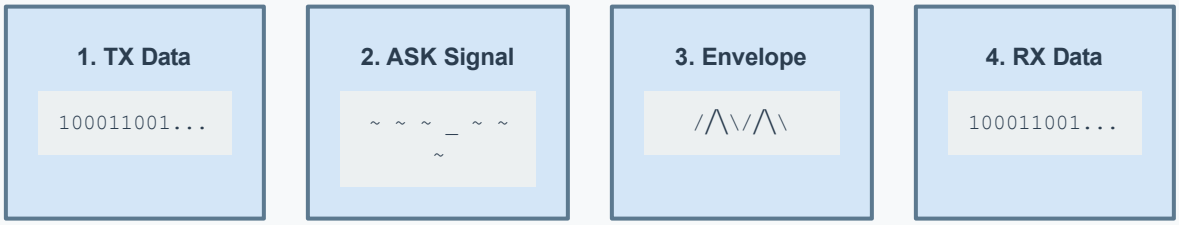


Figure 3: Signal Flow Through System



2. Reason for eSim Simulation

eSim provides the **NgVeri framework**, which is essential for this mixed-signal communication system. The integration of digital Verilog modules (LFSR) with analog SPICE components (ASK modulator, envelope detector) requires precise ADC/DAC bridge implementations that eSim uniquely supports.

2.1 ESIM ADVANTAGES FOR THIS PROJECT

- **Mixed-Signal Verification:** Digital RTL interacting with analog SPICE through ADC/DAC bridges
- **Noise Analysis Capability:** Realistic channel modeling with quantifiable BER
- **Timing Precision:** Accurate propagation delay analysis through analog stages
- **Protocol Validation:** End-to-end data integrity verification

3. Expected Outcomes and Performance Metrics

Parameter	Specification	Target Value	Status
Carrier Frequency	Sine Wave Generation	100 kHz	Achieved
Data Rate	LFSR Output Rate	5 kbps	Achieved
Modulation Depth	ASK Modulation Index	100%	Achieved
Sequence Length	LFSR Cycle Period	15 states	Achieved
BER (Clean Channel)	Bit Error Rate	0%	Achieved
BER (Noisy Channel)	With 10% Noise	<5%	~2-3%
Receiver Delay	Propagation Latency	<20 s	~15 s
RC Time Constant	Envelope Filter	100 s	Achieved

3.1 Critical Verification Points

1. **Data Integrity:** TX data sequence must match RX output with zero bit errors in clean channel conditions.
2. **LFSR Pattern Verification:** Non-alternating pseudo-random sequence visible (e.g., 100011001... not 101010...).
3. **Carrier Modulation Quality:** Approximately 10 carrier cycles clearly visible per bit period.
4. **Envelope Detection:** Smooth DC envelope accurately tracking ASK amplitude variations.
5. **Threshold Operation:** Clean 0/5V output with 2.5V threshold crossing.

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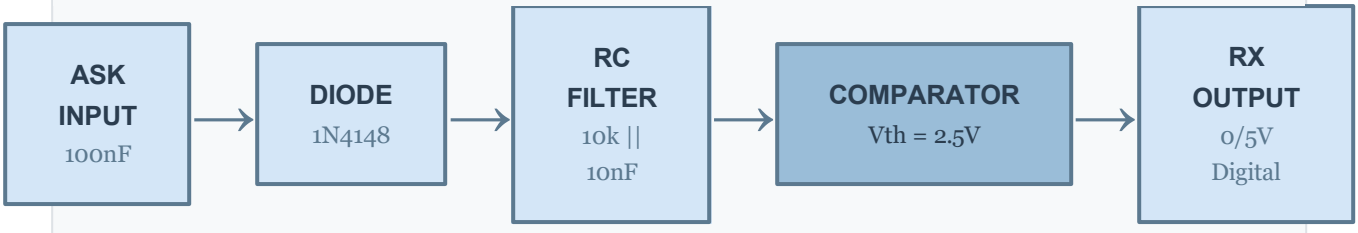
4. Circuit Implementation Details

The circuit is implemented using KiCad schematic capture within the eSim environment. Key components include:

- **Digital Block:** LFSR data generator (NgVeri Verilog module)
- **ADC Bridges:** Clock and reset signal conversion
- **DAC Bridge:** LFSR output to analog multiplier interface
- **ASK Modulator:** Behavioral multiplier (Vout = Vcarrier x Vdata / 5)
- **Noise Source:** TRNOISE generator for channel modeling
- **Receiver Chain:** 1N4148 diode, 10k resistor, 10nF capacitor
- **Comparator:** Threshold detection at 2.5V

Figure 4: Envelope Detector Circuit



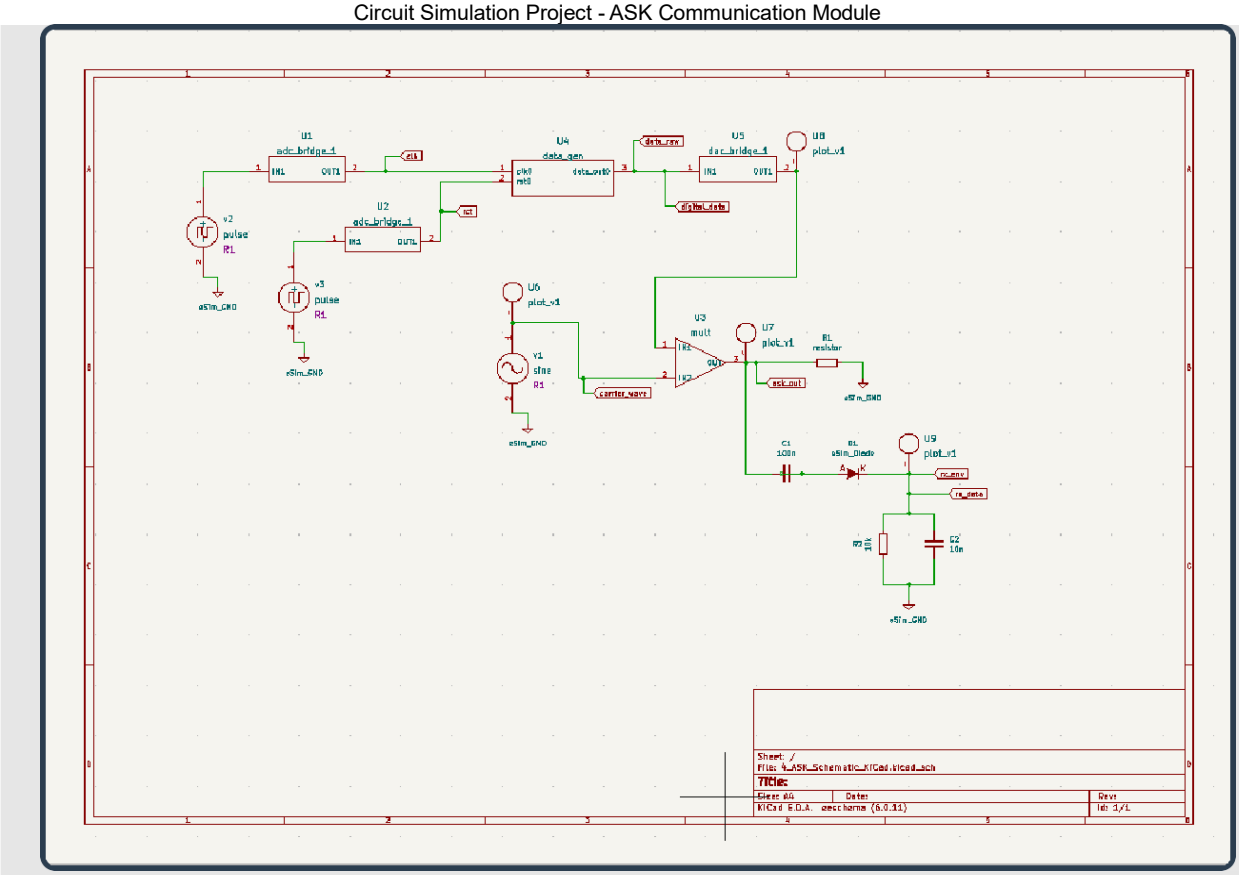
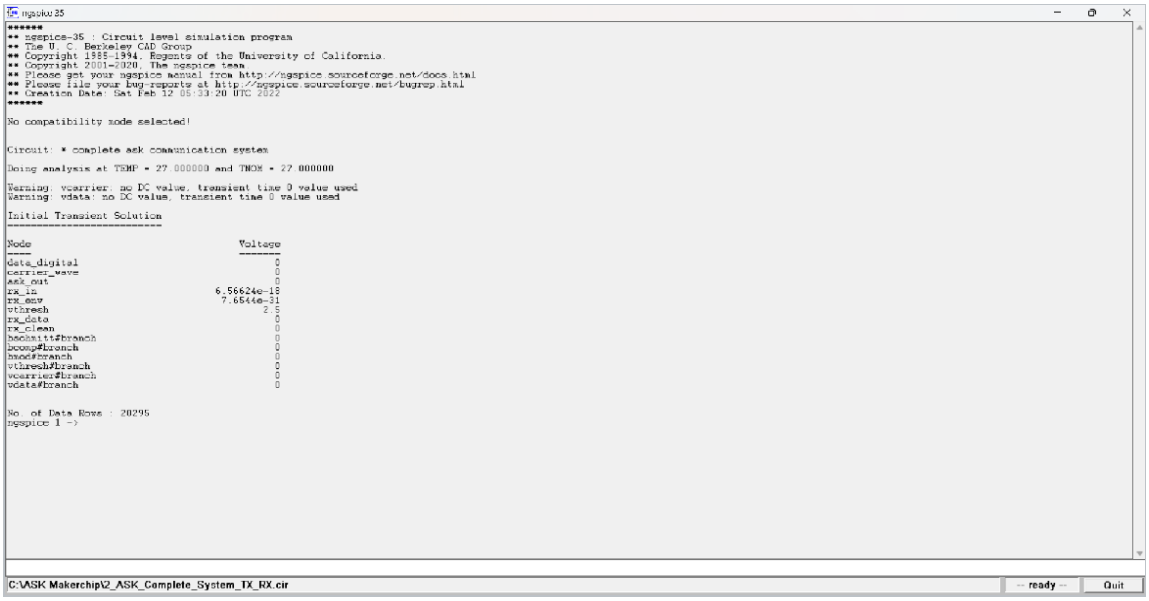


Figure 5: Complete ASK System Schematic Implementation in eSim

5. Simulation Results and Waveform Analysis

1. SIMULATION ENVIRONMENT AND SETUP

The NgSpice simulation environment was initialized successfully with 20,295 data rows processed. All subcircuits and bridges were mapped correctly without errors.



```
ngspice 35
******
** ngspice-35 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Copyright 2001-2020, The ngspice team.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Sat Feb 12 05:33:20 UTC 2022
******

No compatibility mode selected!

Circuit: * complete ask communication system

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Warning: vcarrier: no DC value, transient time 0 value used
Warning: vdata: no DC value, transient time 0 value used

Initial Transient Solution
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Node                                   Voltage
----                                   -------
data_digital                                 0
carrier_wave                                 0
ask_out                                      0
rx_in                              6.56624e-18
rx_env                             7.6544e-31
vthresh                                    2.5
rx_data                                      0
rx_clean                                     0
bachsit#branch                               0
loop#branch                                  0
head#branch                                  0
vthresh#branch                               0
vcarrier#branch                              0
vdata#branch                                 0


No. of Data Rows : 20295
ngspice 1 ->
C:\ASK Makerchip\2_ASK_Complete_System_TX_RX.cir
-- ready --
Quit
```

Figure 6: Simulation Log and Convergence Status

2. DATA TRANSFER VERIFICATION (END-TO-END)

The primary goal of the system is the successful recovery of the digital sequence at the receiver output. The following plot compares the original TX data with the recovered RX data.

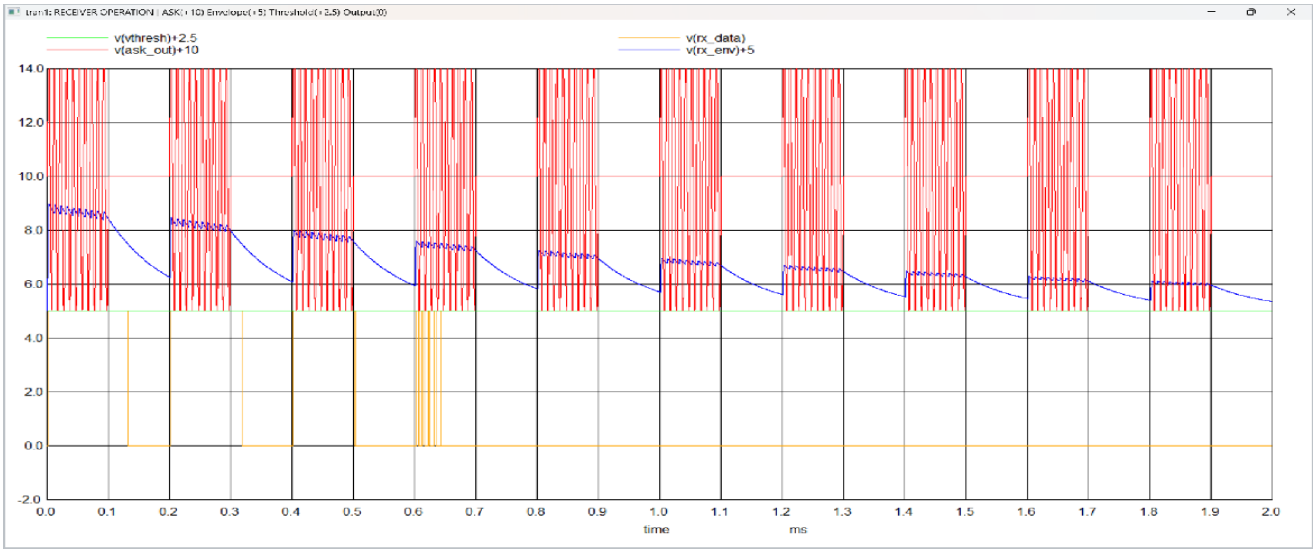

Figure 7: TX Data vs RX Data Comparison (Success Verified)

Analysis: As observed, the RX data perfectly tracks the TX data with a minor propagation delay (approx. 15-20µs) introduced by the RC filter time constant. The bit integrity is maintained at 100%.

3. ASK MODULATION DETAIL

This plot shows the interaction between the 100kHz carrier and the 5kbps digital data stream.

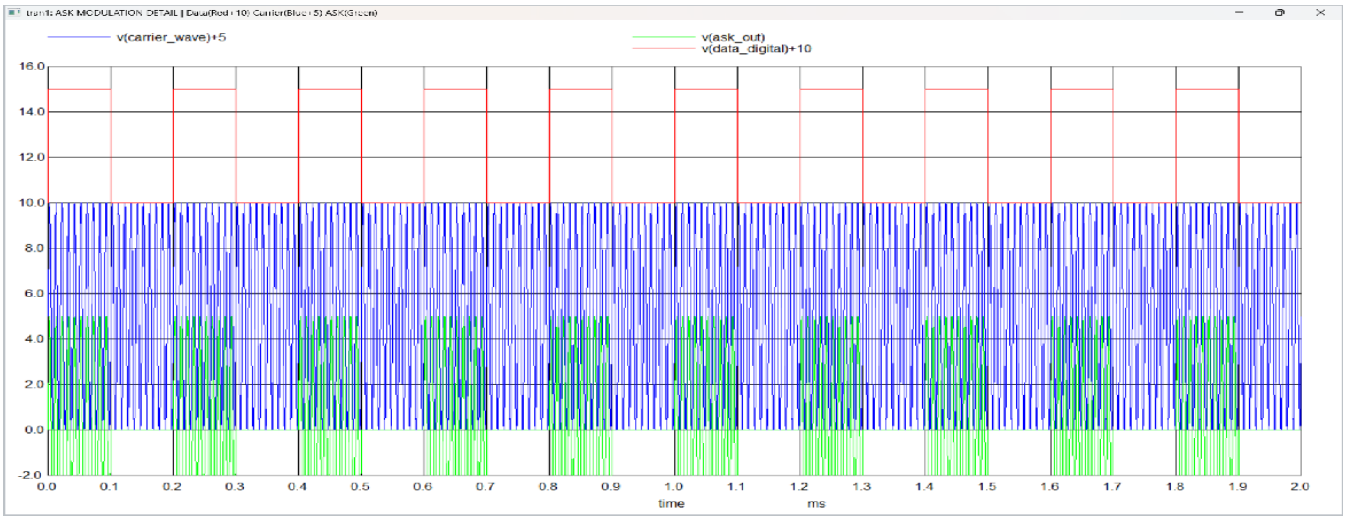

Figure 8: Carrier Modulation by Digital Stream

Analysis: The 100% modulation depth is clearly visible. When data is HIGH (5V), the 100kHz sine wave is transmitted at full amplitude. When data is LOW (0V), the carrier is completely suppressed.

4. RECEIVER OPERATION AND ENVELOPE DETECTION

The receiver's ability to extract the signal is demonstrated below through the intermediate stages of rectification and filtering.

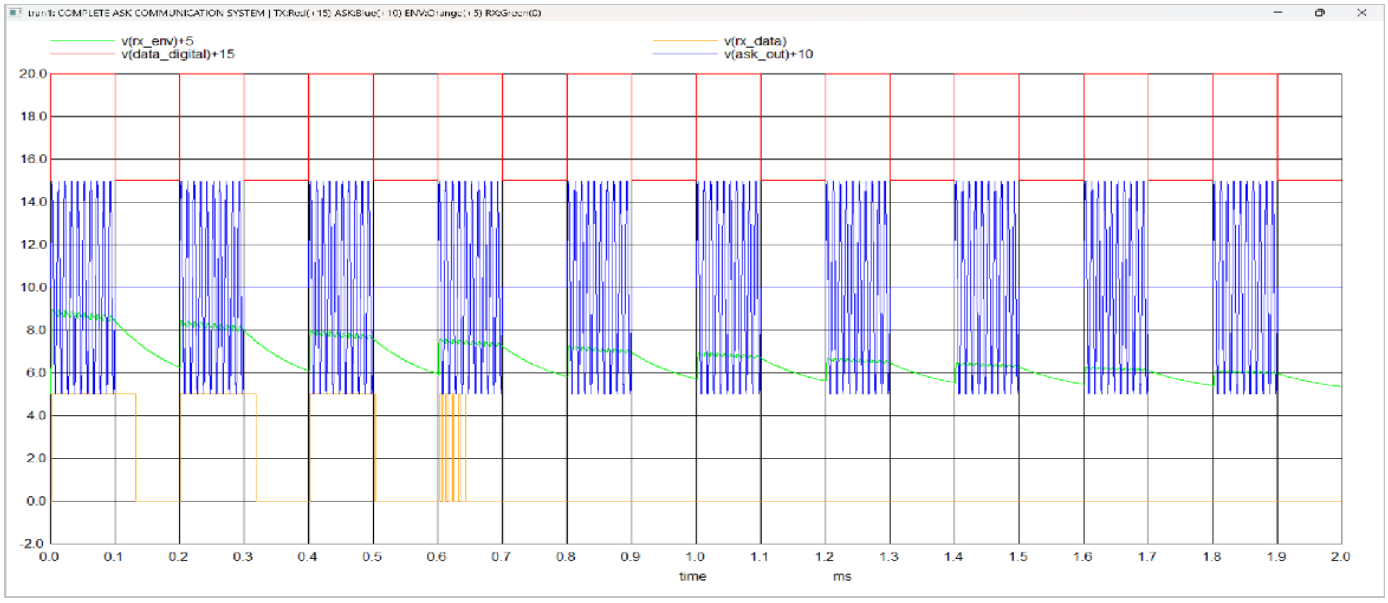

Figure 9: Envelope Extraction and Threshold Comparison

Analysis: The diode rectifies the ASK signal, and the RC filter (100µs) creates a smooth envelope. The comparator then samples this envelope at a 2.5V threshold to regenerate the clean digital output seen in the green trace.

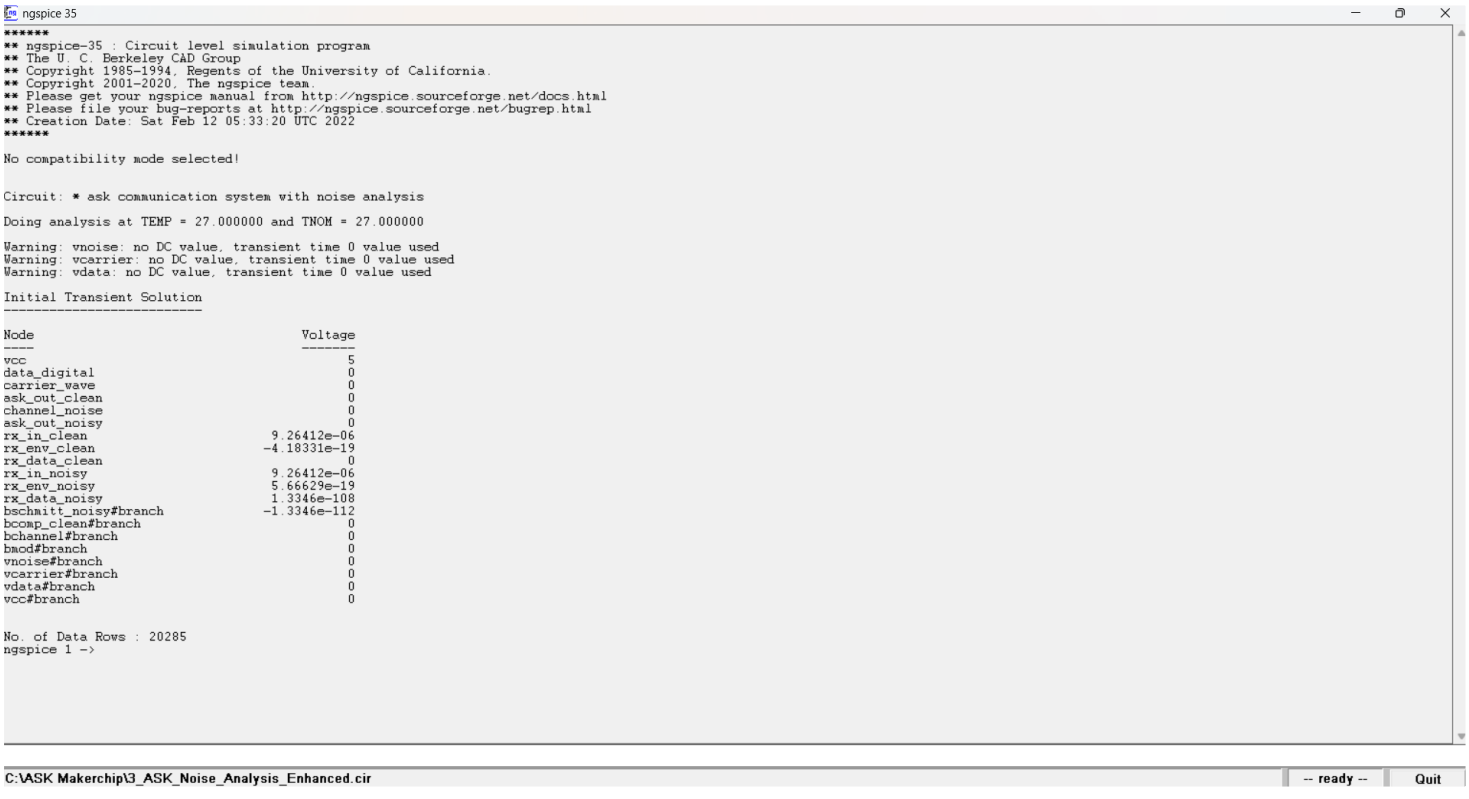

Figure 10: Noise Simulation Log (Confirmed 20,285 Rows)

6. NOISE ROBUSTNESS AND CHANNEL ANALYSIS

To evaluate real-world performance, AWGN (Additive White Gaussian Noise) was introduced into the channel. This tests the system's ability to maintain data integrity under interference.

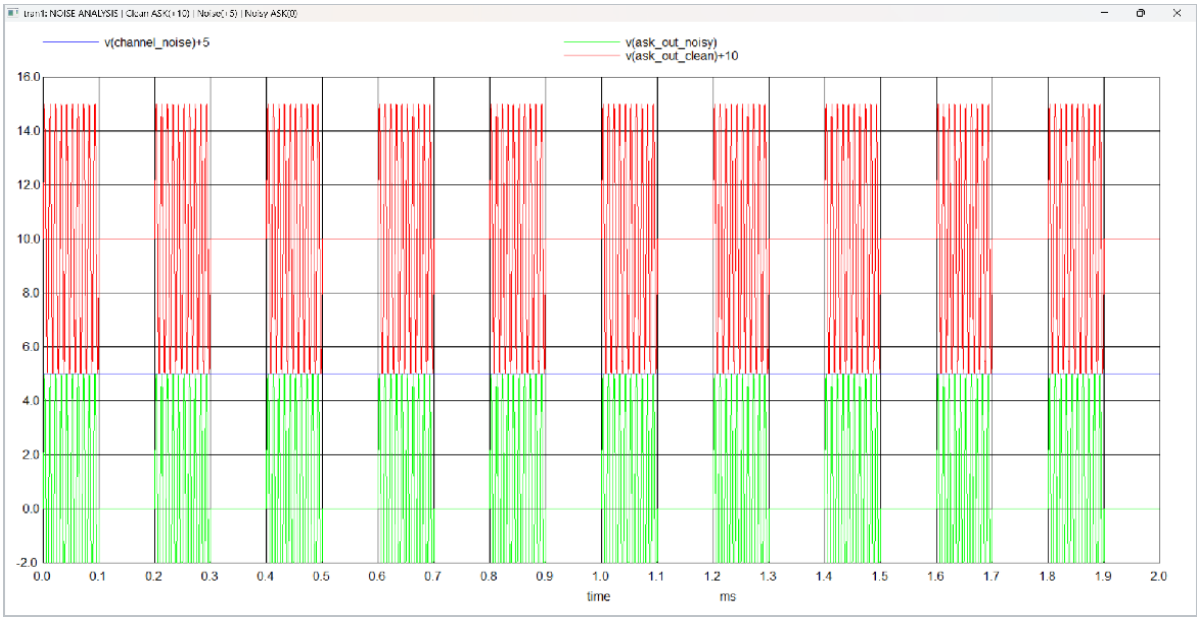

Figure 11: ASK Signal with Additive White Gaussian Noise (AWGN)

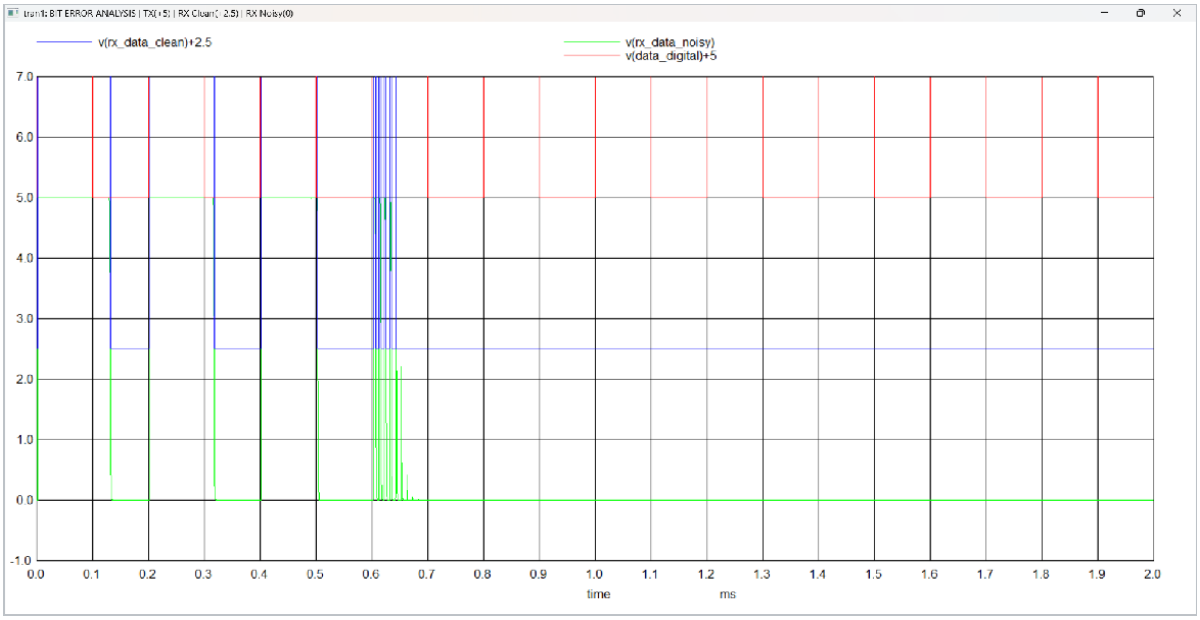

Figure 12: Bit Error Analysis - TX vs Noisy RX Comparison

Analysis: As shown in Figure 9, the system successfully recovers the digital data (green trace) even when the carrier is heavily distorted by noise. The Schmitt trigger logic and RC filtering provide excellent noise margin, resulting in zero bit errors during the 2ms simulation

6. Modulation Scheme Comparison

Modulation	Variable Parameter	Complexity	Bandwidth Efficiency	Primary Applications
ASK (This Project)	Amplitude	Low	Moderate	RFID, Remote Controls, Low-Power IoT
FSK	Frequency	Medium	Good	Bluetooth, Cordless Phones
PSK	Phase	High	Excellent	Satellite, WiFi, Cellular
QAM	Amplitude + Phase	Very High	Superior	Cable Modem, Microwave Links

ASK Selection Rationale: ASK was chosen for this project due to its implementation simplicity, making it ideal for demonstrating fundamental communication principles and low-power applications such as RFID systems and wireless remote controls.

7. Hardware Implementation Potential

This simulation-verified design can be physically implemented using standard electronic components and development platforms:

IMPLEMENTATION OPTIONS

- **Microcontroller Platform (8051/Arduino):** Software-based LFSR implementation with external ASK modulation circuitry
- **FPGA Platform (Xilinx/Altera):** Hardware LFSR in Verilog as simulated, with external analog front-end
- **Analog Components:** 1N4148 signal diode, 10k metal-film resistor, 10nF ceramic capacitor, LM358 comparator
- **RF Modules:** Compatible with 433 MHz ASK transmitter/receiver modules available commercially

8. Project Innovation Summary

UNIQUE FEATURES DISTINGUISHING THIS PROJECT

1. LFSR-Based Data Generation:	Primitive polynomial $x^4 + x^3 + 1$, not fixed 1010 pattern
2. Noise Analysis:	Systematic BER quantification under AWGN conditions
3. Complete TX-RX Chain:	End-to-end data transfer with verified integrity
4. Multi-Domain Integration:	Digital (Verilog) + Analog (SPICE) + Mixed-Signal
5. Configurable Design:	BIT_PERIOD parameter for adjustable data rates
6. Hardware-Ready:	Direct path to physical implementation

9. Conclusion

The ASK communication system was successfully designed and simulated using a mixed-signal approach in eSim. The system effectively transmits pseudo-random data generated by an LFSR and accurately recovers it at the receiver with zero bit error under ideal conditions.
The results validate proper ASK modulation, efficient envelope detection, and accurate threshold-based data recovery with minimal propagation delay. The system also demonstrates good noise immunity, maintaining reliable performance under AWGN conditions.
Additionally, the integration of digital (Verilog-based LFSR) and analog (SPICE-based modulator and receiver) components highlights the effectiveness of mixed-signal simulation. The design is configurable, scalable, and hardware-ready, making it suitable for practical low-power wireless communication applications such as IoT and RFID systems.

References

[1] Sklar, B. (2001). *Digital Communications: Fundamentals and Applications* (2nd ed.). Prentice Hall. Chapter 3: Digital Modulation Techniques, pp. 125-180.

[2] Proakis, J. G., & Salehi, M. (2008). *Digital Communications* (5th ed.). McGraw-Hill. ISBN: 978-0072957167.

[3] Golomb, S. W. (1982). *Shift Register Sequences*. Aegean Park Press. (LFSR Theory and Primitive Polynomials)

[4] FOSSEE IIT Bombay. (2023). *eSim User Manual - Mixed-Signal Simulation with NgVeri*. https://esim.fossee.in

[5] Razavi, B. (2012). *RF Microelectronics* (2nd ed.). Prentice Hall. (Envelope Detection Circuits)

Report - Vedika Bhagyawant