Title of the experiment:

Mixed-Signal Fault Detection and Automated Recovery System

Theory:

In critical electronic architectures, relying on software interrupts for fault protection introduces severe vulnerability. If a microcontroller stalls during an over-current event, software fail-safes are ineffective. This project proposes a hardware deterministic protection paradigm. By utilizing discrete analog components, the system achieves near-instantaneous load isolation, operating entirely independently of code execution. The sensing topology employs operational amplifiers configured as open loop comparators in an analog domain. A stable DC reference establishes the maximum safe operating threshold. When a dynamically scaled sensor voltage breaches this reference, the amplifier instantaneously drives its output to the positive saturation rail, generating a fault vector. Physical isolation relies on the state-switching characteristics of high-power MOSFETs. Upon receiving this saturation signal, the MOSFET gate is abruptly driven into deep cutoff. This completely halts current flow, electrically isolating the downstream load to prevent damage. Modeling this hybrid architecture within the eSim SPICE engine requires specialized nodal translation. To prevent convergence failures between continuous analog signals and discrete digital logic, the project implements ADC and DAC bridges. Finally, the circuit features an autonomous self healing paradigm governed by a closed loop watchdog timer. Rather than latching into a permanent fault state that requires manual intervention, this design continuously polls the analog comparator. Once the fault physically dissipates and the parameters normalize, the watchdog timer initiates a calibrated delay. Following this delay, it safely re biases the MOSFET gates, allowing seamless, autonomous system restoration.

Schematic Diagram:

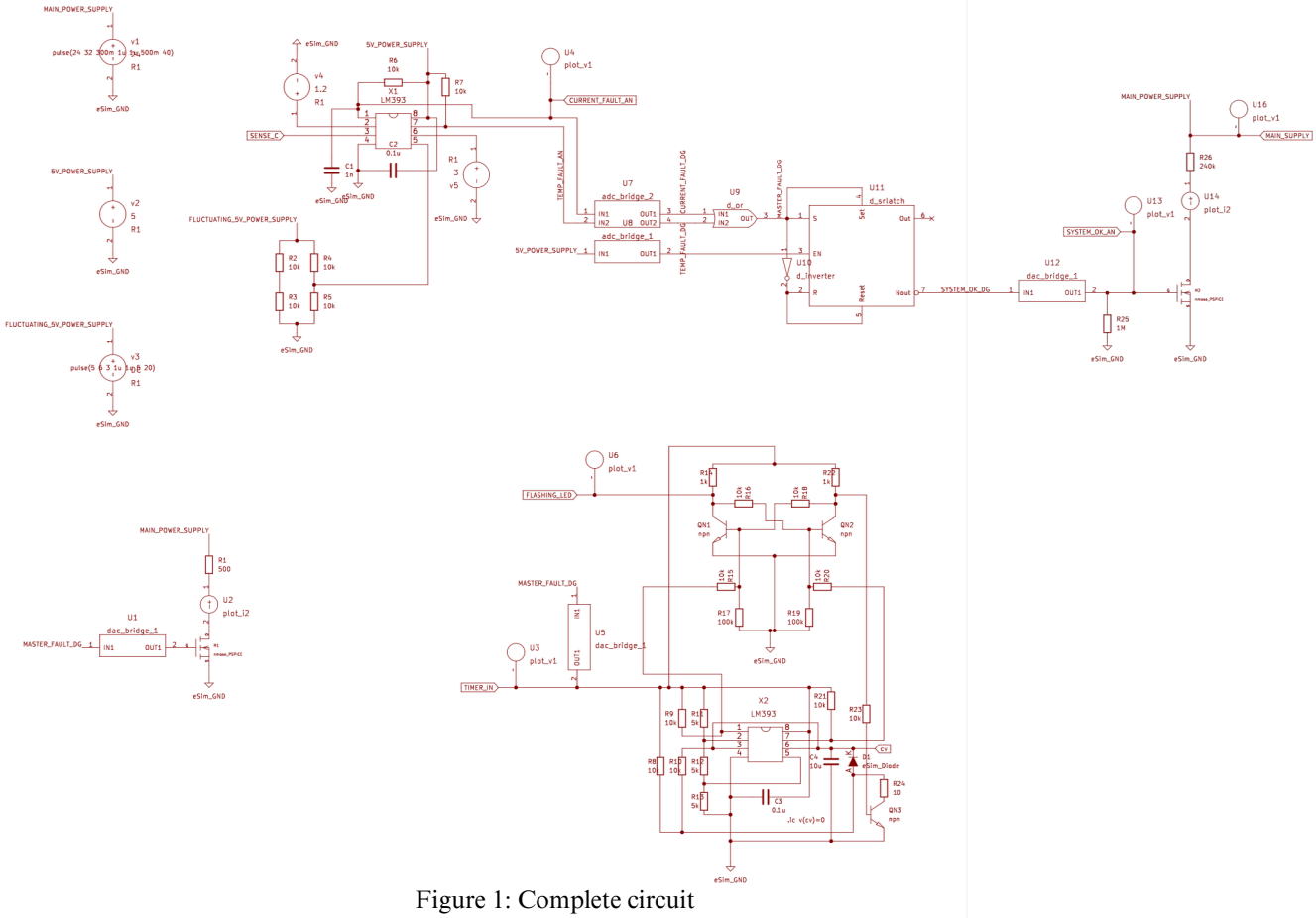

Figure 1: Complete circuit

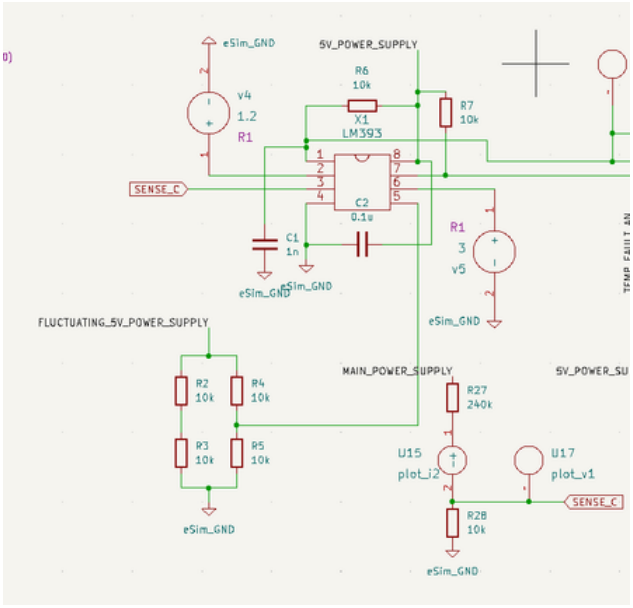

Figure 2: Sensors

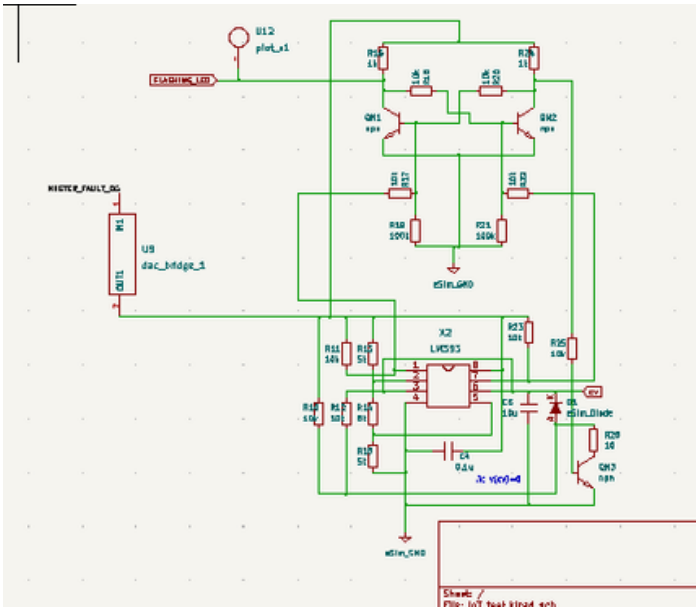

Figure 3: Custom astable multivibrator circuit for LED fault indication

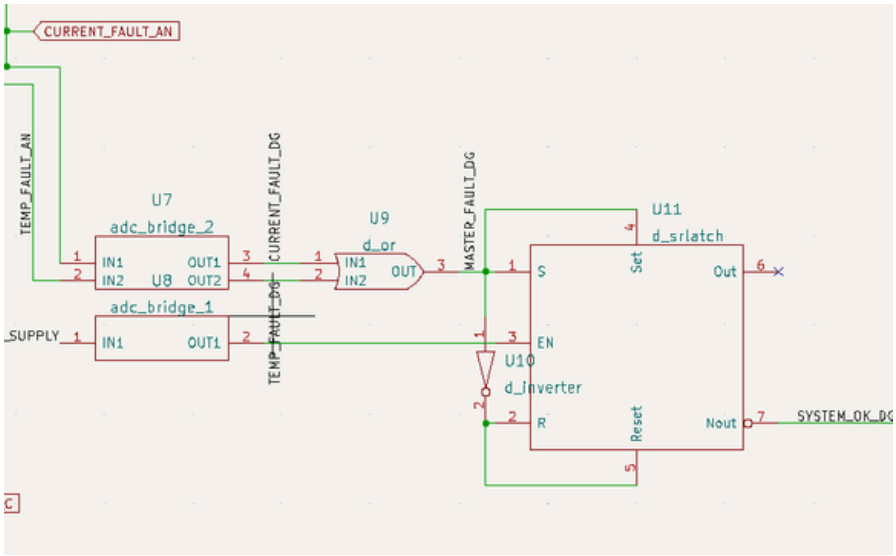

Figure 4: Digital decision making

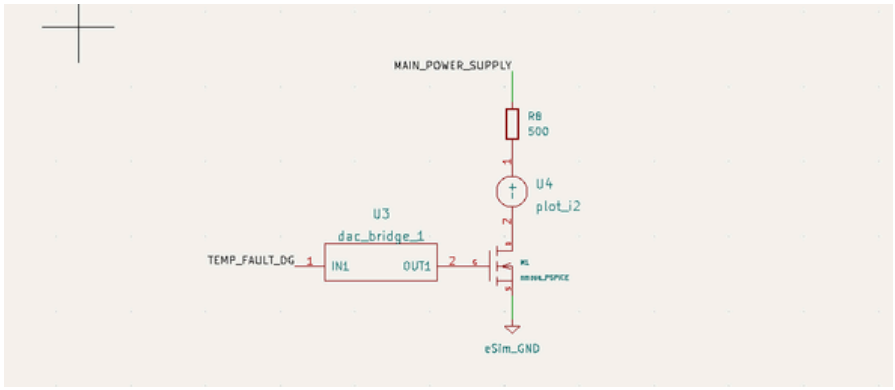

Figure 5: Auto-cooling circuit

Simulation Results :

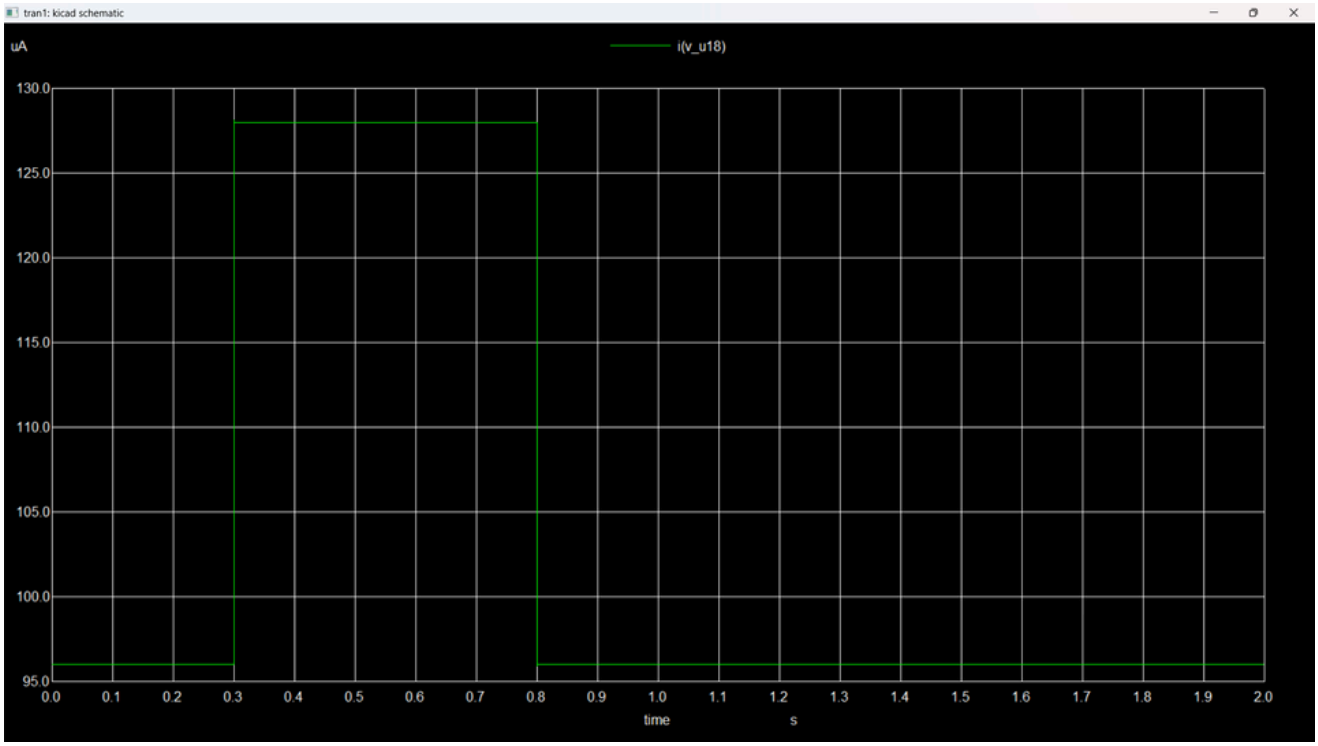

Figure 6: Overcurrent in the main supply

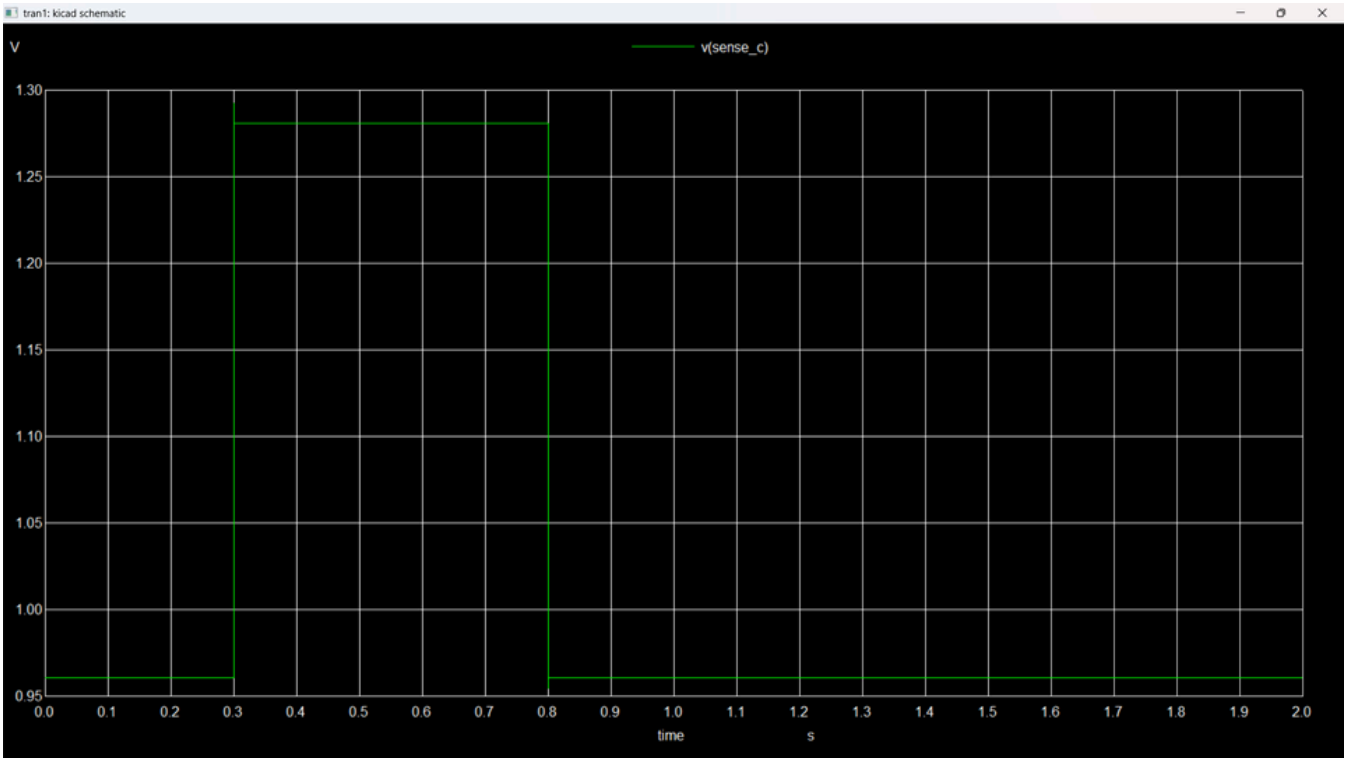

Figure 7: Current fault sensing

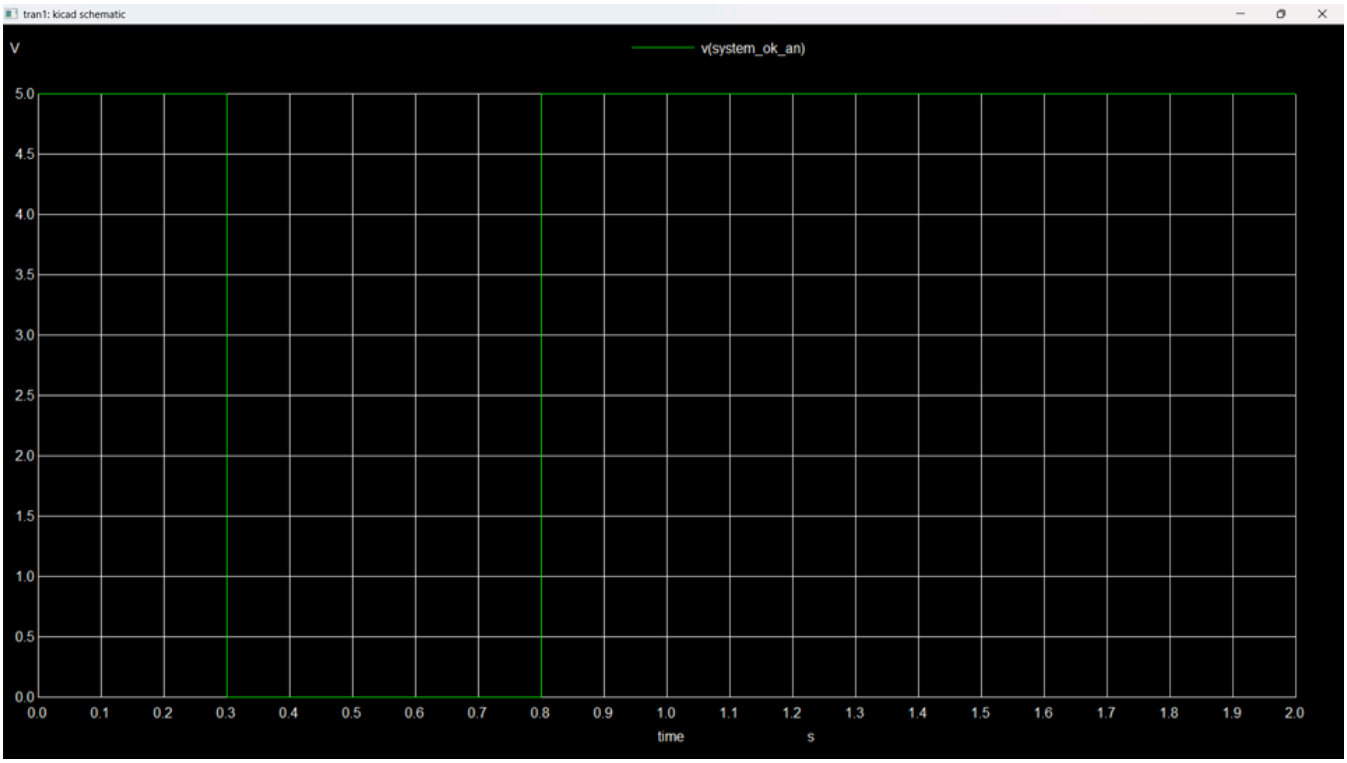

Figure 8: MOSFET Gate voltage goes low as fault is detected

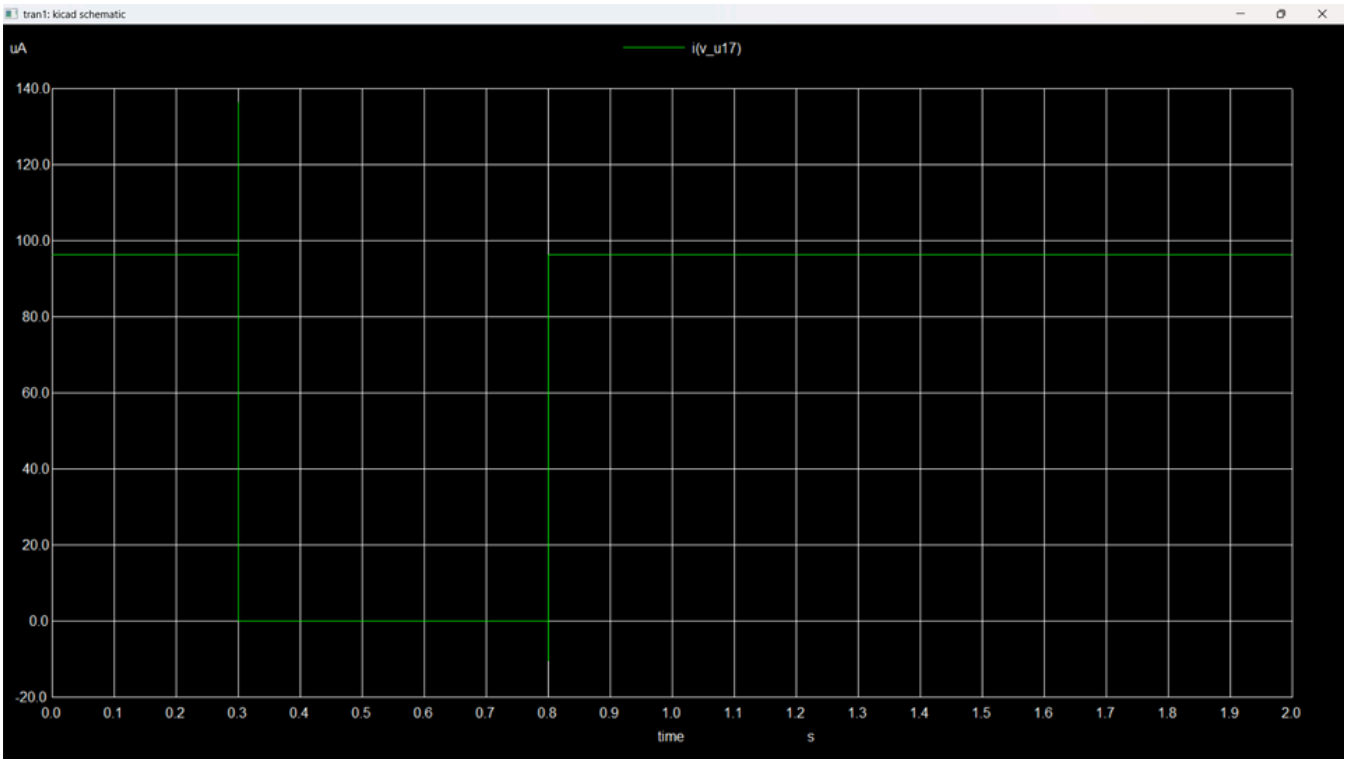

Figure 9: Main line getting OFF as fault is detected

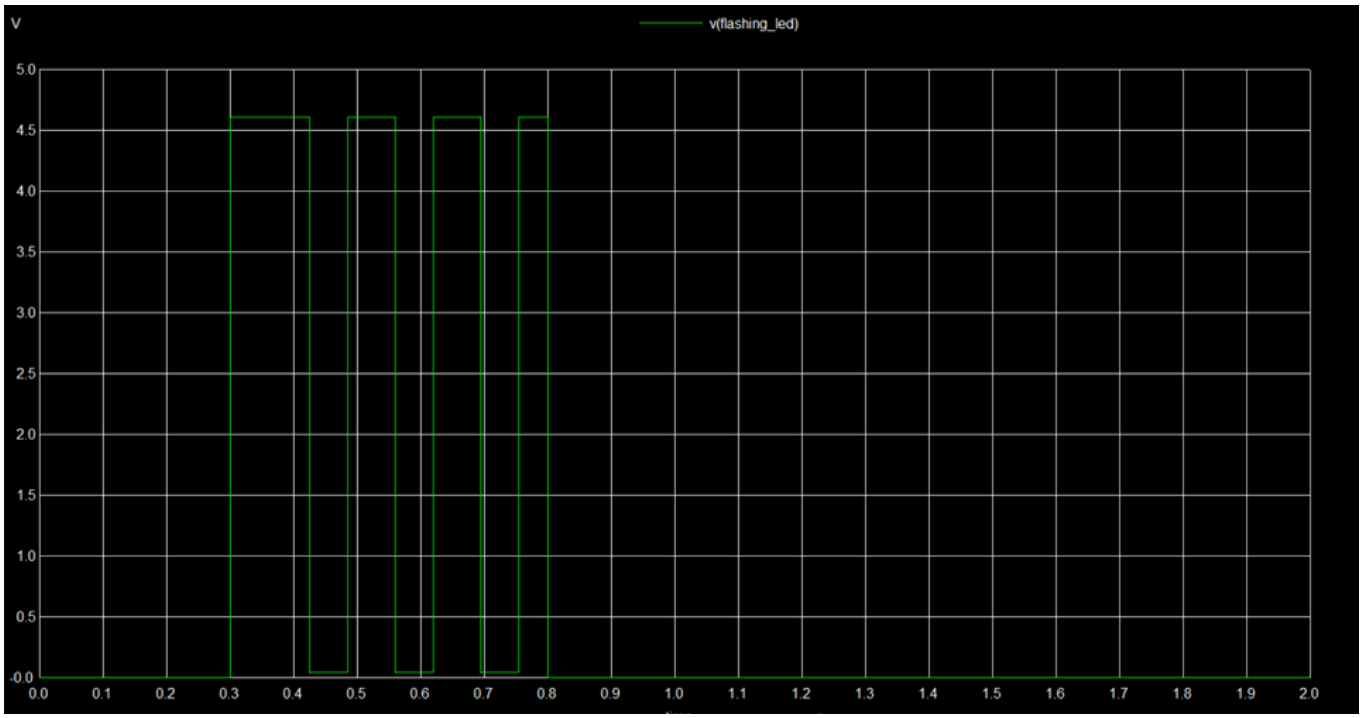

Figure 10: LED indication of fault detection

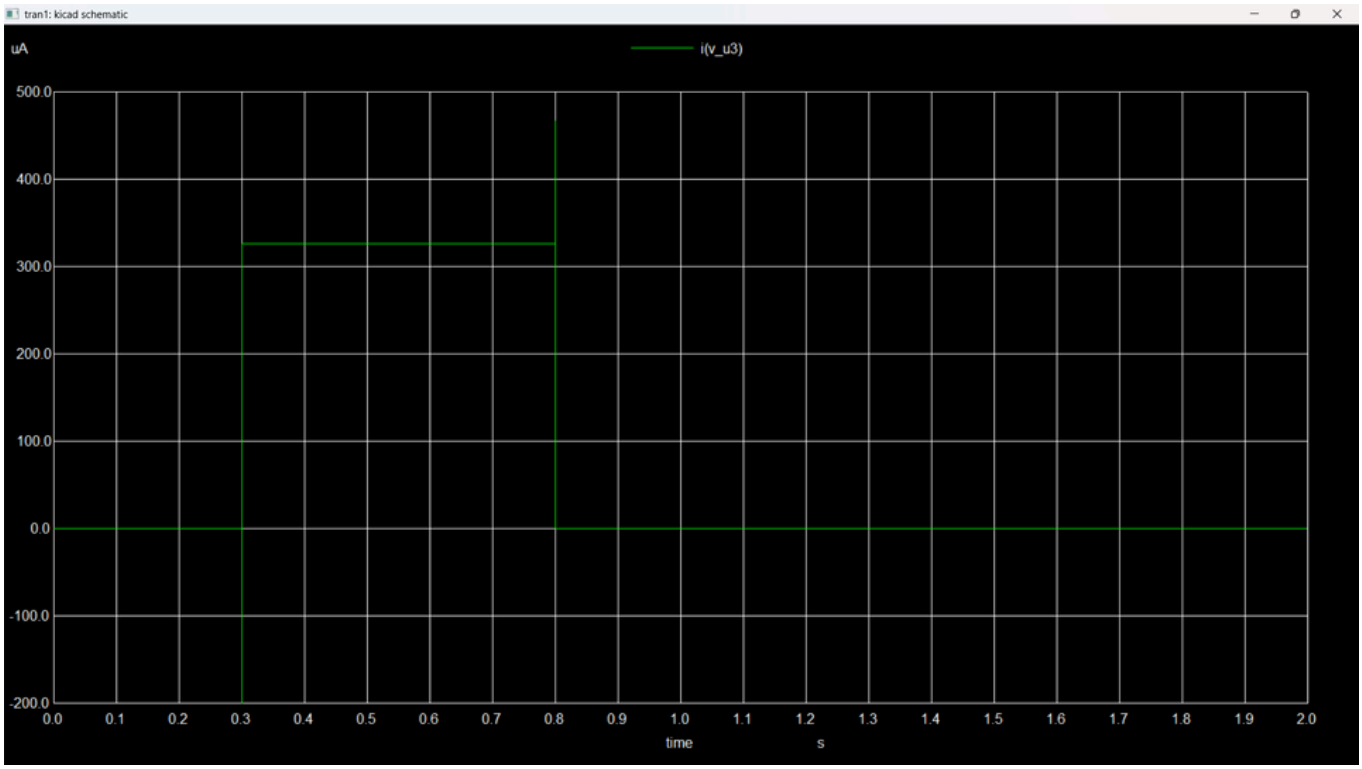

Figure 11: Supply to cooling fan getting turned ON as fault is detected

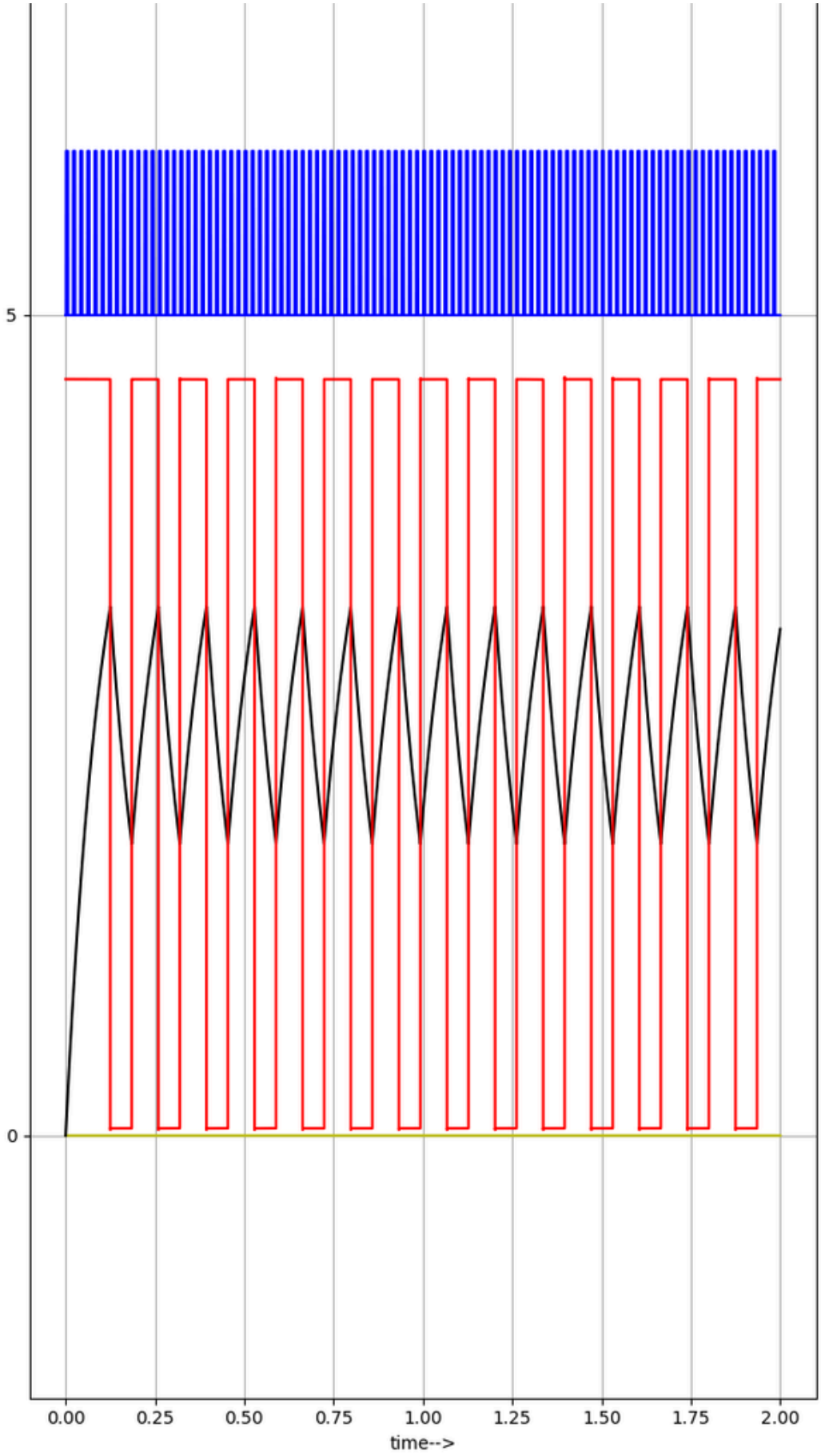

Figure 12: Overall python plots of the experiment

Conclusion :

The successful design and simulation of the hardware based fail safe circuit demonstrates the viability of utilizing deterministic, mixed signal architectures for critical system protection. By effectively integrating continuous time analog sensors with discrete digital logic through precise ADC and DAC nodal bridging in eSim, the project validated the core protection loop. The continuous threshold monitoring via precision operational amplifiers, combined with the rapid power isolation executed by high power MOSFETs, proved highly effective in mitigating simulated over current and thermal fault conditions. Additionally, the system successfully incorporated a custom astable multivibrator to drive localized alarm mechanism during these critical events without relying on software intervention.

Ultimately, this complete circuit architecture provides a robust, self-reliant framework for safeguarding sensitive downstream hardware from catastrophic electrical anomalies.

References :

https://esim.fossee.in/circuit-simulation-project/esim-circuit-simulation-run/746

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