ABSTRACT

Design and Verification of an ISO 14443-A Proximity Communication Link in eSim

1 Theory

This project simulates the data recovery front-end for a proximity integrated circuit card (PICC) operating under the ISO/IEC 14443 Type A standard. According to this standard, contactless communication relies on a precise 13.56 MHz carrier frequency. When the reader (PCD) transmits data to the card, it utilizes 100% Amplitude Shift Keying (ASK) modulation combined with Modified Miller encoding. Modified Miller encoding is highly bandwidth-efficient and ensures reliable clock recovery by selectively suppressing transitions, specifically avoiding a transition at the start of a logic '0' if it immediately follows a logic '1'.

To recover the digital bitstream from the received RF signal, a multi-stage process is required. First, an RF envelope detector demodulates the 13.56 MHz carrier. Because of the physical limitations and transient responses of the passive circuitry, the resulting baseband signal is not a perfect digital square wave. Instead, it presents as a continuous analog envelope with rounded peaks and transient dips (in this simulation, oscillating between bounds of 2.7V and 3.6V).

Because digital logic ICs cannot reliably interpret these gradual, "curvy" analog transitions, a discrete digitization stage is strictly required. To convert the analog envelope back into a precise 1001 binary sequence, a high-speed comparator or Schmitt Trigger circuit is utilized. By establishing a rigid reference voltage threshold (e.g., 3.1V) that sits perfectly within the bounded window of the analog signal, the comparator acts as a high-speed hardware switch. When the demodulated signal drops below this 3.1V threshold during a Modified Miller "dip," the output snaps violently to a high state (5V); when it recovers, it snaps to a low state (0V). Utilizing a high-speed comparator architecture bypasses the slew-rate limitations inherent in standard operational amplifiers, ensuring the recovered square wave edges align perfectly with the strict timing intervals dictated by the ISO 14443A standard.

2 Schematic Diagram

The circuit schematic of the Design and Verification of an ISO 14443-A Proximity Communication Link in eSim is as shown below:

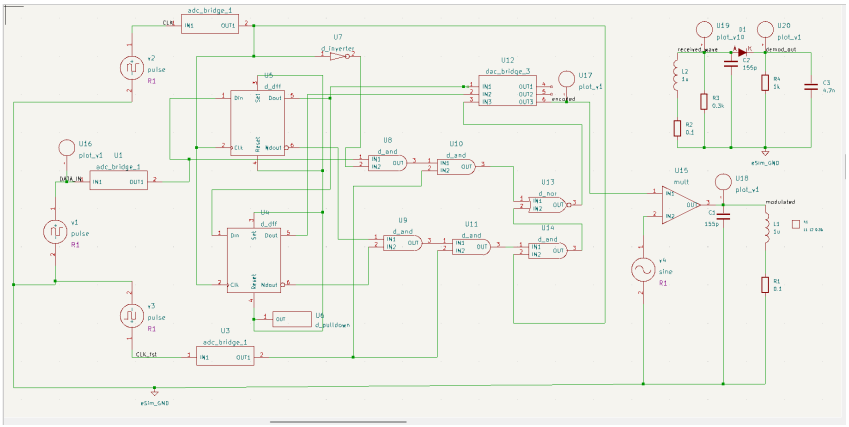

Figure 1: Frequency response of BJT

3 Simulation Results

3.1 Ngspice Plots

The following plots illustrate the input, intermediate and output characteristics as generated by the Ngspice engine within eSim:

- **Input Wave:** The graph represents the original, unencoded binary message (the raw 1s and 0s) generated by the system. It is a standard digital square wave, cleanly transitioning between logic low and logic high, serving as the baseline data sequence that needs to be transmitted. The input is 1001.

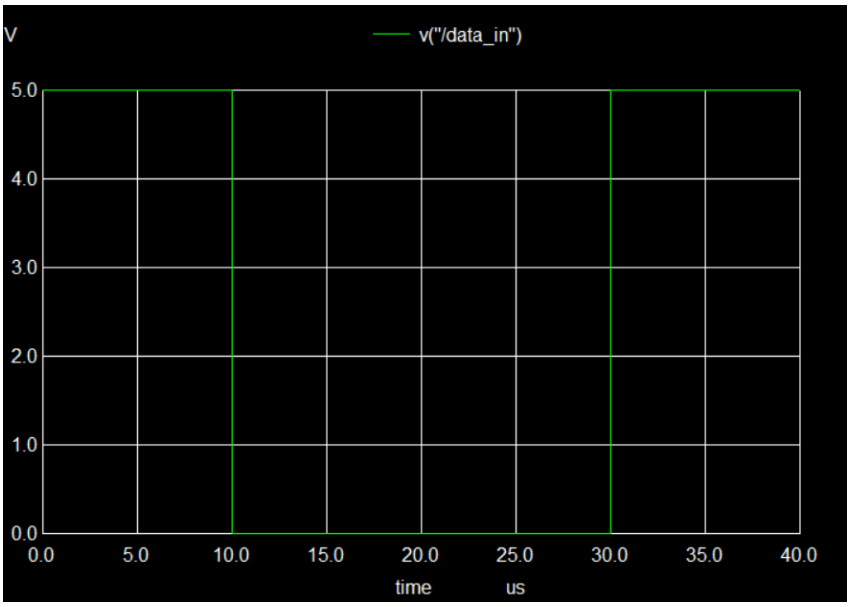

Figure 2: Ngspice Plot: Input Wave

- **Encoded Wave:** The graph displays the baseband signal after the raw digital input has been processed through the Modified Miller encoder. In Miller encoding, a logic '1' is represented by a voltage transition in the middle of the bit period,

while a logic '0' transitions at the start. However, to conserve bandwidth, if a '0' immediately follows a '1', that starting transition is deliberately suppressed. Notice that the waveform features these specific timed transitions and extended gaps in accordance with these rules. This encoded format ensures high bandwidth efficiency and allows for reliable clock recovery at the receiver. This is the final baseband signal that is fed into the RF modulator.

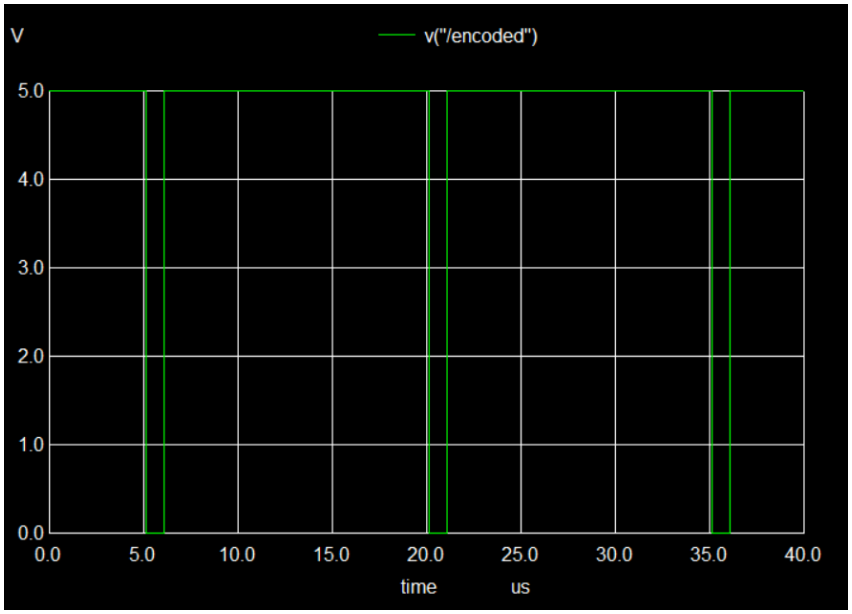

Figure 3: Ngspice Plot: Encoded Wave

- **Modulated or Transmitted Wave:** Because pure digital square waves cannot travel through the air, the data must be 'piggybacked' onto a very fast radio wave (a 13.56 MHz carrier frequency). The dense, solid-looking blocks represent the continuous radio wave, while the distinct vertical 'gaps' (where the voltage drops to zero) represent the digital data being embedded into the signal so it can be transmitted wirelessly.

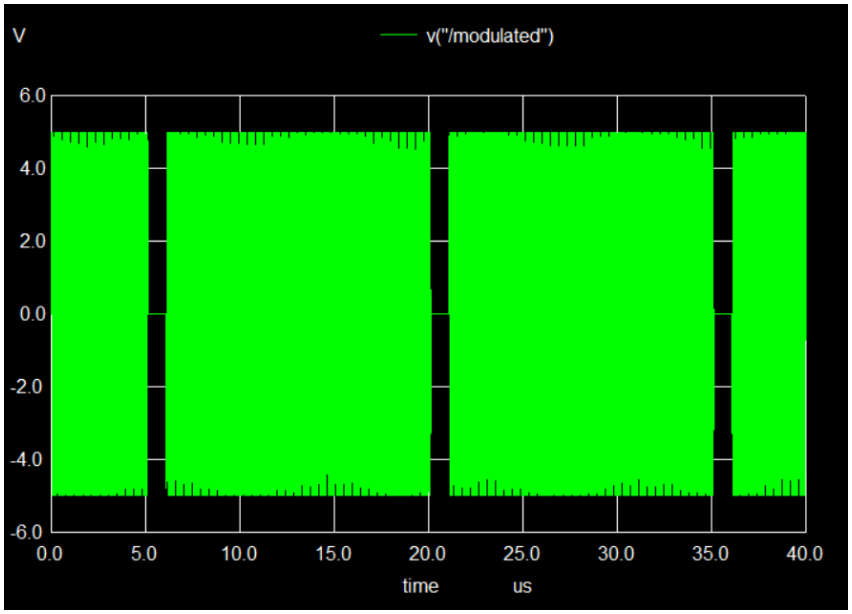

Figure 4: Ngspice Plot: Modulated or Transmitted Wave

- **Received Wave at Tag:** The graph shows the signal after it has been caught by the receiver's antenna and processed by the demodulator circuit. The circuit 'traces the outline' of the received radio wave to extract the hidden data. However, because real-world electrical components (like capacitors) take a brief moment to charge and discharge, the previously sharp digital edges become curved 'shark fins.' This oscillating analog wave is what the final comparator stage must digitize to fully recover the pure 1s and 0s.

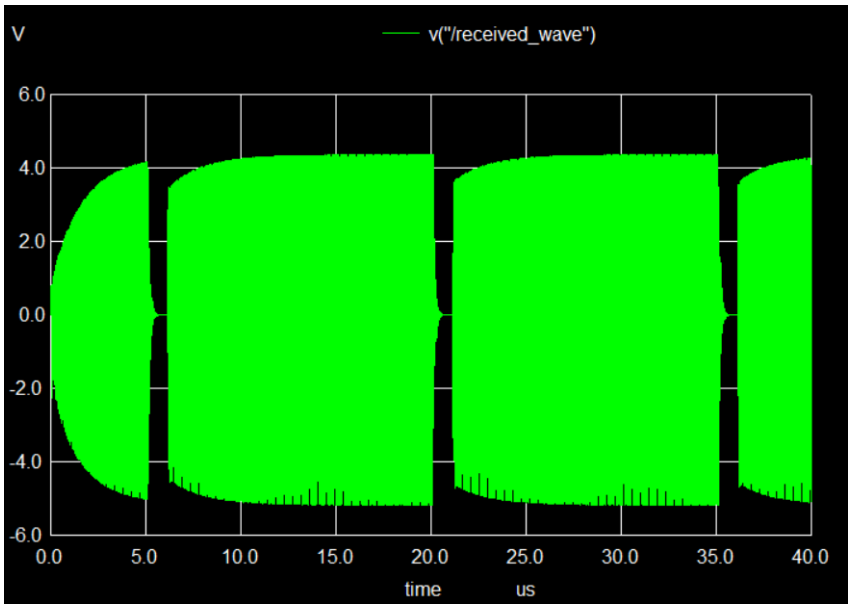

Figure 5: Ngspice Plot: Received Wave

- **Demodulated Wave:** The graph displays the raw Ngspice simulation output of the received signal after it has passed through the envelope detector. The high-frequency 13.56 MHz carrier wave has been successfully filtered out, leaving be-

hind this analog baseband waveform. The distinct curved shapes (the charge and discharge curves) are a direct physical result of the RC (resistor-capacitor) time constants in the passive demodulator circuit. This plot verifies that the envelope detector successfully extracted the Modified Miller sequence, oscillating smoothly between the 2.7V and 3.6V boundaries.

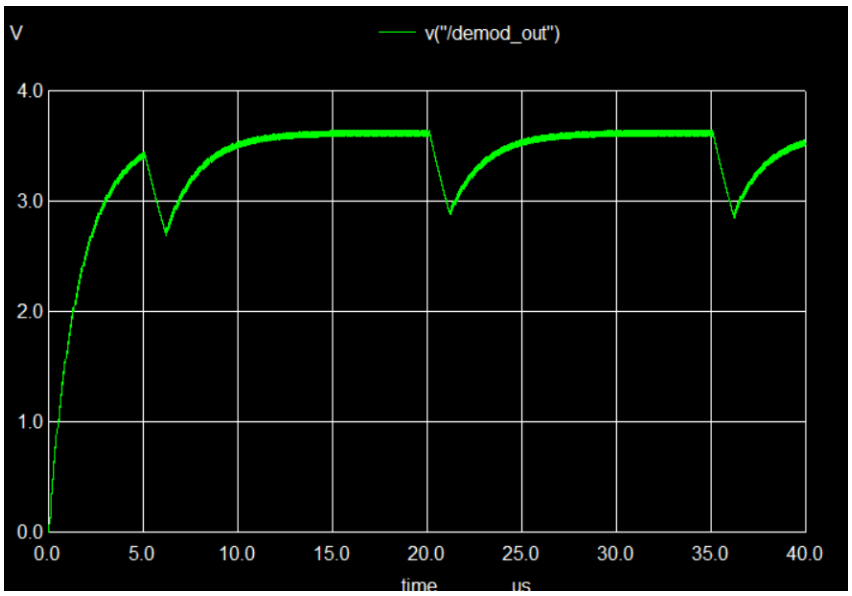

Figure 6: Ngspice Plot: Demodulated Wave

4 Conclusion

This project successfully simulated and verified the front-end data recovery architecture for an ISO/IEC 14443 Type A proximity integrated circuit card. By utilizing eSim, KiCad, and the Ngspice simulation engine, the complete signal path was modeled: from the raw binary input, through Modified Miller encoding, onto a 13.56 MHz ASK-modulated carrier, and finally through an analog envelope detector to recover the baseband signal.

While the theoretical concepts of RFID communication are straightforward, implementing and simulating the circuit presented several practical challenges and initial failures that provided valuable engineering insights:

Software and Netlist Complexities: A major challenge involved bridging the gap between KiCad's schematic capture and the Ngspice simulation engine. Initial simulations failed silently or produced syntax errors due to auto-generated net labels (such as the addition of forward slashes to node names) and misconfigured voltage sources. Debugging the raw Ngspice terminal commands was required to successfully force the transient analysis to plot the data.

Tuning the RC Time Constant: Designing the envelope detector was not a trivial task. Initial component values resulted in a failure to accurately track the envelope. If the capacitor was too large, the discharge rate was too slow, completely missing the fast Modified Miller "dips." If it was too small, excessive 13.56 MHz ripple bled into the baseband signal. Finding the exact balance to create the smooth "shark fin" waveforms (oscillating cleanly between 2.7V and 3.6V) required careful iterative tuning.

Strict Threshold Tolerances: The project highlighted the fragility of the analog-to-digital recovery boundary. Because the demodulated envelope did not return to 0V

(floating instead at a 2.7V minimum), standard logic gates would fail to read the signal. Implementing a comparator was necessary, but it required an extremely precise reference threshold (e.g., 3.1V). Even minor deviations in this threshold would cause the final digital output to fail entirely, proving how sensitive RF receiver design is to component tolerances.

5 References

1. https://esim.fossee.in/
2. ngspice.sourceforge.io/docs.html
3. https://www.wiley.com/en-us/RFID+Handbook