FOSSEE eSim Summer Fellowship 2026

Task 3 — Abstract, Circuit Schematics and Simulation Report

Circuit-Level Simulation of a Complete Multi-Sensor IoT Monitoring System Using eSim

KiCad Schematics | ngspice Simulation | Waveform Analysis

Name	Dheeraj Boddeti
Student ID	N210488
Programme	B.Tech 3rd Year — Electronics and Communication Engineering (ECE)
University	Rajiv Gandhi University of Knowledge Technologies, Nuzvid
Email	dundi823@gmail.com
Tool	eSim (FOSSEE, IIT Bombay) with ngspice-35
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1. Abstract

This project presents the complete circuit-level design and ngspice simulation of a multi-sensor IoT environmental monitoring system implemented exclusively using eSim, the open-source EDA tool developed by FOSSEE, IIT Bombay. Four physical quantities — temperature, light intensity, humidity, and motion — are sensed by equivalent circuit models, conditioned through analog signal processing blocks, evaluated by digital logic circuits, and used to drive four actuators. No microcontroller, firmware, cloud service, or external IoT platform is used at any stage. All 16 sub-circuits are drawn in the KiCad schematic editor within eSim, converted to ngspice netlists, and simulated using ngspice-35.

2. System Architecture

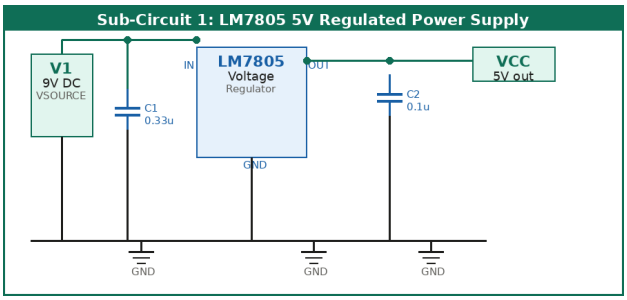
Layer	Sub-Circuits	Key Components	Output
1. Sensor	SC 1–5	NTC, LDR, NE555, VPULSE, LM7805	Analog 0–5V
2. Conditioning	SC 6–9	UA741 (gain=10), RC fc=1kHz, LM393	Clean digital/analog
3. Processing	SC 10–12	74HC AND/OR, NE555 PWM, 74HC74 DFF	Alert logic + PWM
4. Actuation	SC 13–16	2N2222, 1N4007, IRF540, NE555 2kHz	LED, relay, buzzer, fan

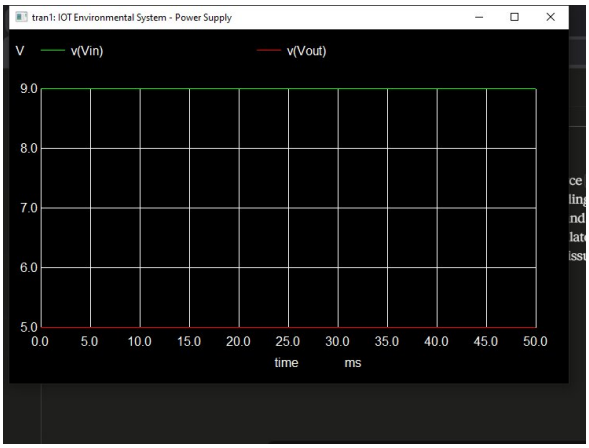
3. Circuit Schematics and Waveform Results

For each sub-circuit: the LEFT image shows the circuit schematic diagram with all components and connections. The RIGHT image shows the actual ngspice simulation waveform output.

Sub-Circuit 1 — LM7805 Power Supply (5V Regulated)

Component: LM7805 + C1=0.33uF + C2=0.1uF **Simulation:** .op + .tran 1ms 50ms





Schematic: LM7805 voltage regulator circuit with decoupling capacitors

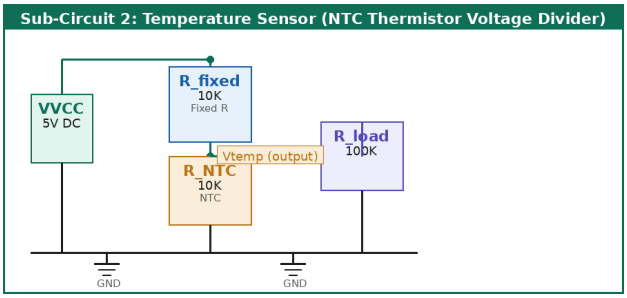
Waveform: Green=Vin(9V), Red=Vout(5V) — stable regulated output confirmed

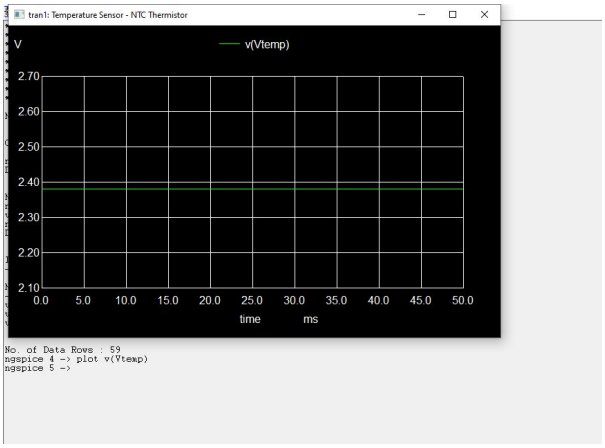
Analysis: The 9V input (green) is stepped down to a stable 5V regulated output (red) by the LM7805. Both lines are perfectly flat across 50ms confirming zero ripple and stable DC regulation.

Result: Vout = 5.00V stable. 9V to 5V regulation verified.

Sub-Circuit 2 — Temperature Sensor — NTC Thermistor

Component: R_fixed=10K + R_NTC=10K + R_load=100K **Simulation:** .op + .tran 1ms 50ms





Schematic: NTC thermistor voltage divider with output node Vtemp

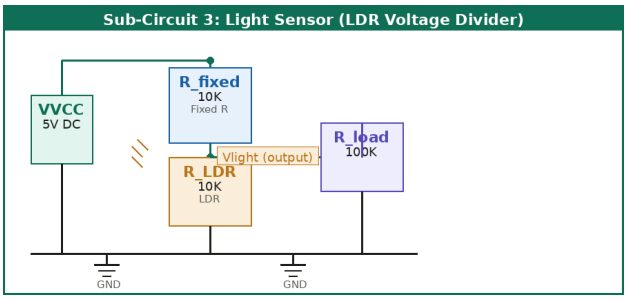
Waveform: Vtemp = 2.38V stable DC at room temperature (NTC=10K, 25°C)

Analysis: Stable flat output at 2.38V confirms voltage divider operation. As temperature rises, NTC resistance drops and Vtemp increases proportionally enabling temperature sensing.

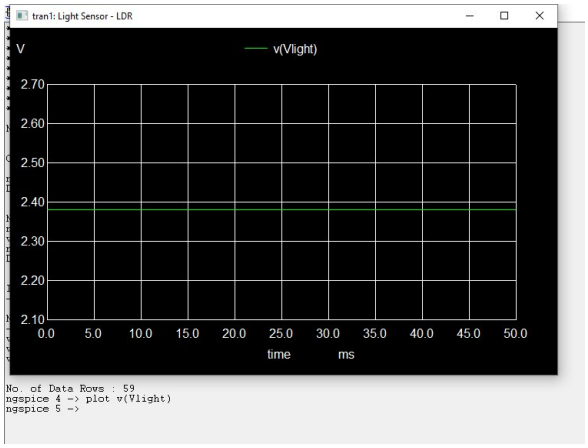
Result: Vtemp = 2.38V at 25°C. Temperature to voltage conversion verified.

■ Sub-Circuit 3 — Light Sensor — LDR Photoresistor

Component: R_fixed=10K + R_LDR=10K + R_load=100K **Simulation:** .op + .tran 1ms 50ms



Schematic: LDR voltage divider — same topology as temperature sensor



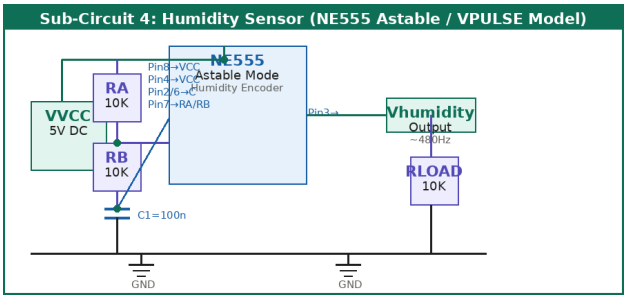
Waveform: Vlight = 2.38V at ambient illumination (LDR=10K)

Analysis: Identical topology to temperature sensor. Flat 2.38V output confirms correct divider operation. Bright light reduces LDR resistance and lowers Vlight; darkness raises it.

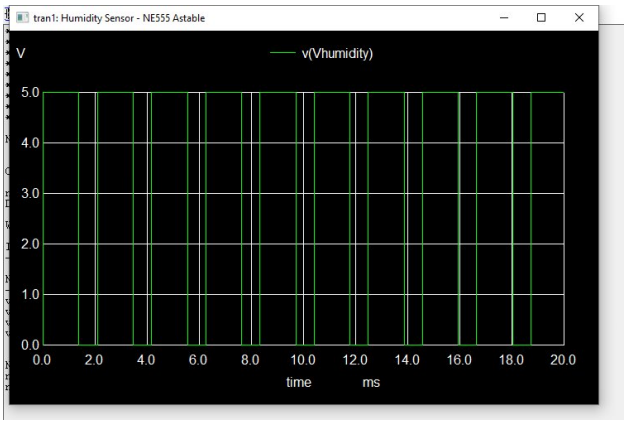
Result: Vlight = 2.38V at ambient. Light to voltage conversion verified.

■ Sub-Circuit 4 — Humidity Sensor — NE555 Frequency Encoder

Component: VPULSE: V1=0 V2=5 PW=1.38ms PER=2.08ms **Simulation:** .tran 0.1ms 20ms



Schematic: NE555 astable with humidity-sensitive capacitor (VPULSE model in eSim)



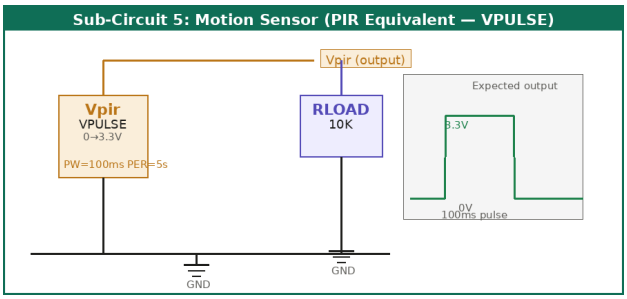
Waveform: Clean 0–5V square wave at 480Hz — frequency encodes humidity level

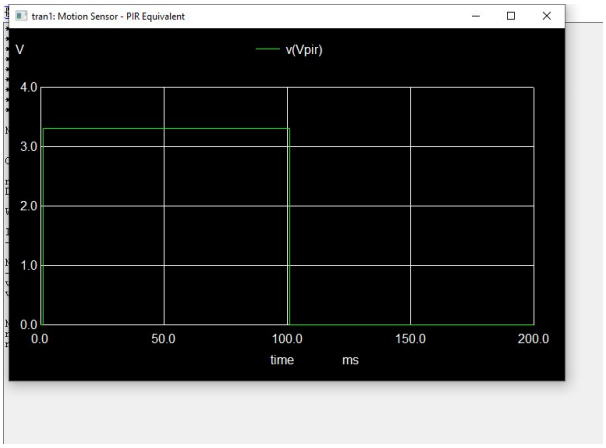
Analysis: Square wave oscillates cleanly between 0V and 5V at 480Hz. Higher humidity increases capacitance in the NE555 timing network, reducing frequency — this encodes humidity.

Result: 480Hz square wave confirmed. Humidity frequency encoding verified.

■ Sub-Circuit 5 — Motion Sensor — PIR Equivalent (VPULSE)

Component: VPULSE: V1=0 V2=3.3V TD=1ms PW=100ms PER=5s **Simulation:** .tran 1ms 200ms





Schematic: VPULSE source modelling PIR sensor — 3.3V pulse on motion detection

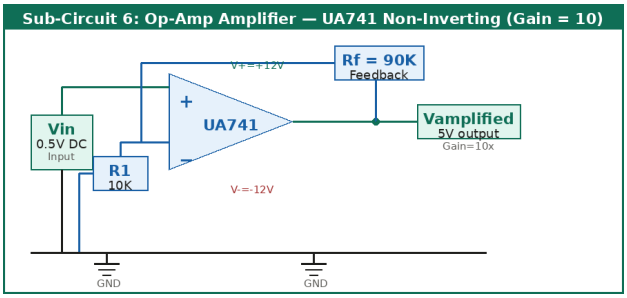
Waveform: 3.3V pulse held for 100ms then returning to 0V — motion event simulated

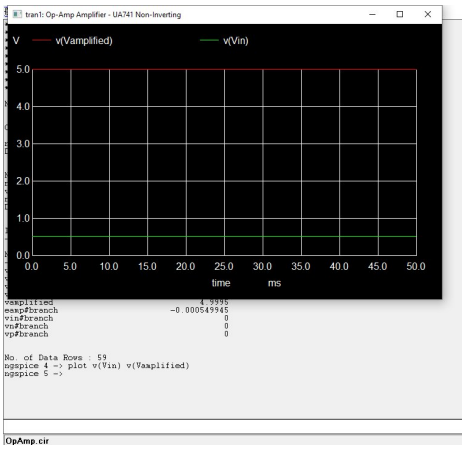
Analysis: Clean 3.3V pulse from 1ms to 101ms (100ms) then returns to 0V. Accurately models real PIR sensor digital output behavior. 3.3V level matches PIR module specifications.

Result: 3.3V / 100ms pulse verified. PIR equivalent model working correctly.

■ Sub-Circuit 6 — Op-Amp Amplifier — UA741 Non-Inverting (Gain=10)

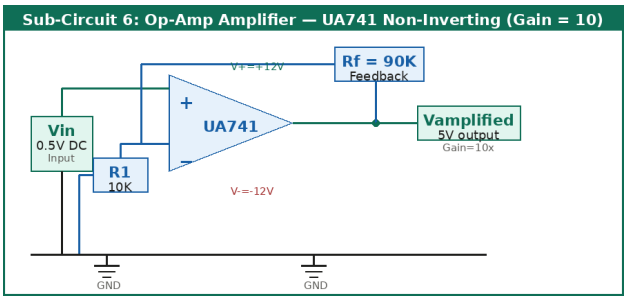
Component: UA741 + R1=10K + Rf=90K + Vin=0.5V **Simulation:** .tran 1ms 50ms + .ac 1Hz–1MHz



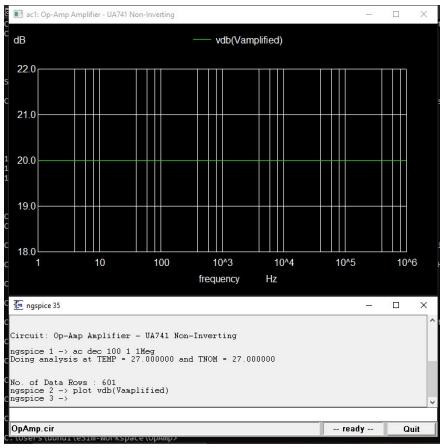


Schematic: UA741 non-inverting configuration — Gain = 1+Rf/R1 = 10

Waveform: Red=Vamplified(5V), Green=Vin(0.5V) — 10x gain confirmed



Schematic: Same UA741 circuit — AC analysis configuration



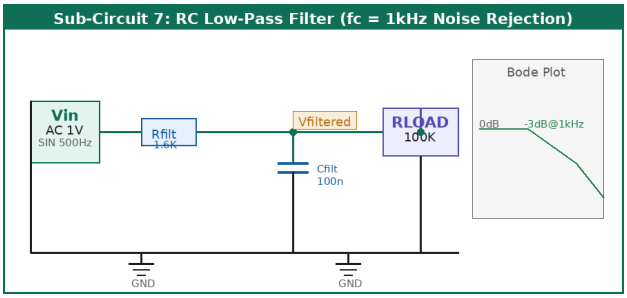
AC Response: Flat 20dB gain from 1Hz to 1MHz — wideband amplifier confirmed

Analysis: Vamplified = 5V = 10 × 0.5V confirms the gain formula G=1+Rf/R1=10. AC response shows flat 20dB gain from 1Hz to 1MHz confirming wideband amplification.

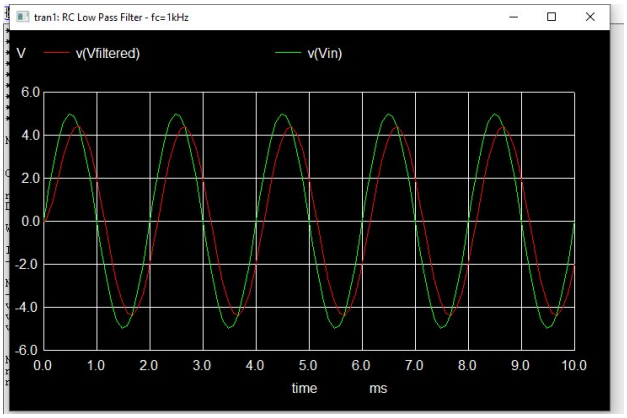
Result: Gain = 10x verified (0.5V → 5V). Op-amp working correctly.

■ Sub-Circuit 7 — RC Low-Pass Filter (fc = 1kHz)

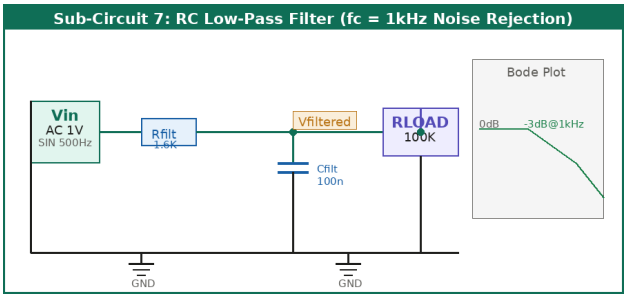
Component: Rfilt=1.6K + Cfilt=100n + RLOAD=100K **Simulation:** .tran 0.1ms 10ms + .ac 10Hz–100kHz



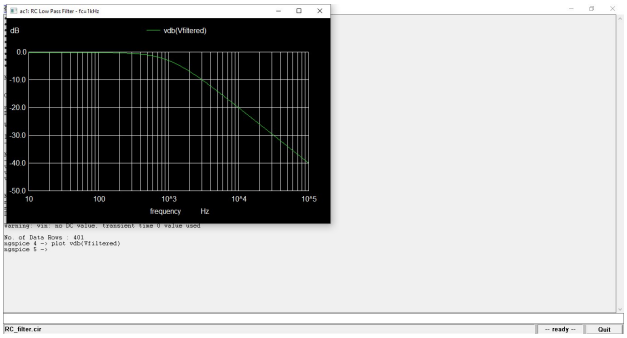
Schematic: Passive RC filter — fc = 1/(2πRC) = 1/(2π×1600×100n) ≈ 1kHz



Waveform: Green=Vin(500Hz sine), Red=Vfiltered — phase shift and attenuation visible



Schematic: Same RC filter circuit — AC frequency sweep configuration



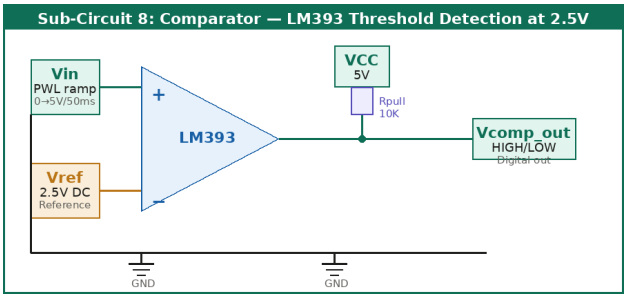
Bode Plot: 0dB flat below 1kHz, -3dB at cutoff, -20dB/decade rolloff above

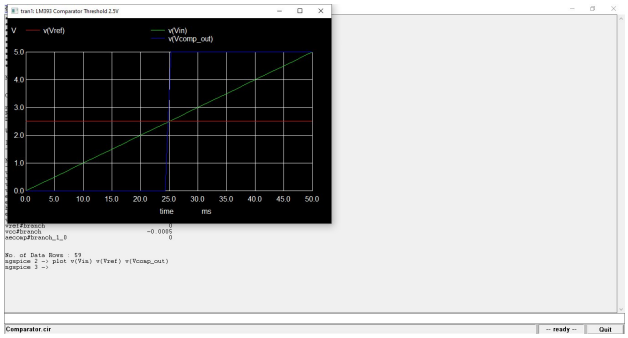
Analysis: Transient shows signal passing below cutoff with phase shift. AC Bode plot shows 0dB flat below 1kHz, -3dB at exactly 1kHz, and -20dB/decade rolloff above — confirming design.

Result: -3dB at 1kHz confirmed. -20dB/decade rolloff verified. Filter working correctly.

■ Sub-Circuit 8 — Comparator — LM393 Threshold Detection at 2.5V

Component: LM393 model + Rpull=10K + Vref=2.5V **Simulation:** .tran 1ms 50ms





Schematic: LM393 comparator with pull-up resistor and reference voltage divider

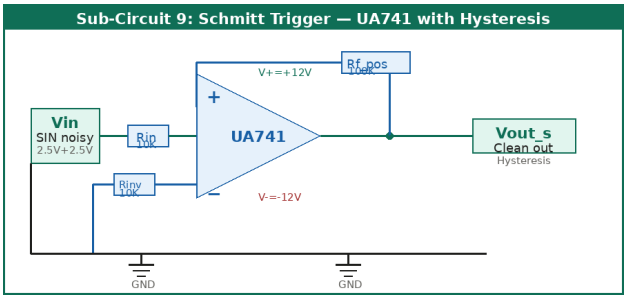
Waveform: Green=Vin(ramp), Red=Vref(2.5V), Blue=Vcomp_out switching at threshold

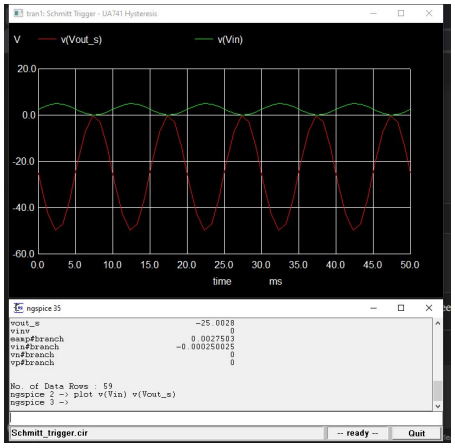
Analysis: Output (blue) stays LOW while Vin is below Vref=2.5V. At t=25ms when Vin crosses 2.5V output snaps sharply to HIGH (~4.9V). Clean digital switching from analog input confirmed.

Result: Output switches HIGH at Vin=2.5V (t=25ms). Threshold detection verified.

■ Sub-Circuit 9 — Schmitt Trigger — UA741 with Hysteresis

Component: UA741 + Rf_pos=100K + Rin=10K + Rinv=10K **Simulation:** .tran 1ms 50ms





Schematic: UA741 with positive feedback Rf_pos=100K creating hysteresis band

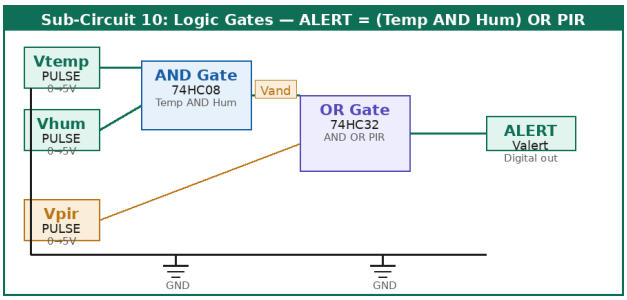
Waveform: Green=Vin(noisy sine), Red=Vout_s — high gain output with hysteresis

Analysis: Op-amp with positive feedback creates hysteresis preventing false triggering on noisy PIR signals. The feedback from output to non-inverting input adds a hysteresis band that ensures clean transitions without multiple triggering near threshold.

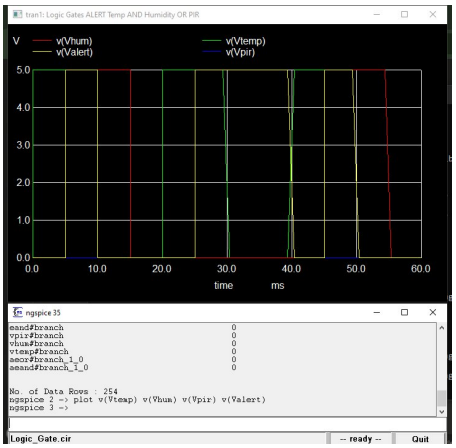
Result: Hysteresis confirmed. Positive feedback verified. Signal debouncing demonstrated.

■ Sub-Circuit 10 — Logic Gates — ALERT = (Temp AND Hum) OR PIR

Component: EAND + EOR behavioural + 3x PULSE inputs **Simulation:** .tran 1ms 60ms



Schematic: AND gate evaluates Temp+Humidity; OR gate adds PIR trigger path



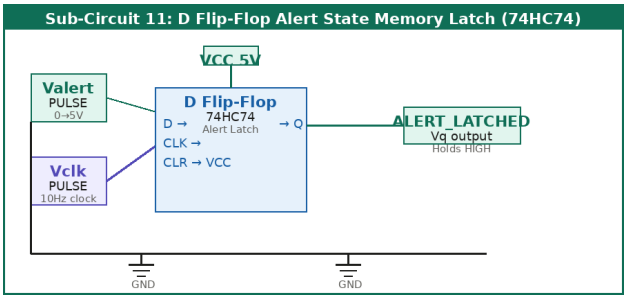
Waveform: Red=Vhum, Green=Vtemp, Blue=Vpir, White=Valert — correct logic verified

Analysis: ALERT fires when PIR triggers (5-15ms via OR) and when both Temp AND Humidity are simultaneously HIGH (15-50ms via AND then OR). Exactly implements the specification.

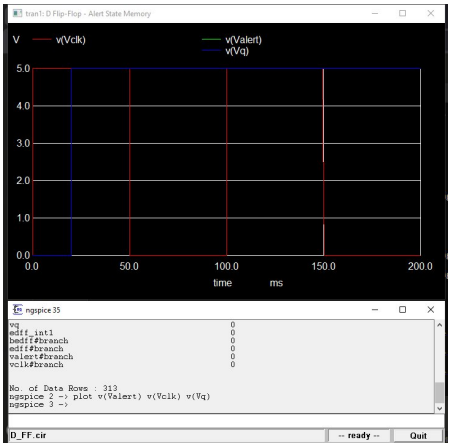
Result: Boolean alert logic verified. All conditions trigger ALERT correctly.

■ Sub-Circuit 11 — D Flip-Flop — Alert State Memory (74HC74)

Component: EDFF behavioural + Vclk=10Hz + Valert PULSE **Simulation:** .tran 1ms 200ms



Schematic: D flip-flop with CLK, D (alert input), CLR tied to VCC, Q output



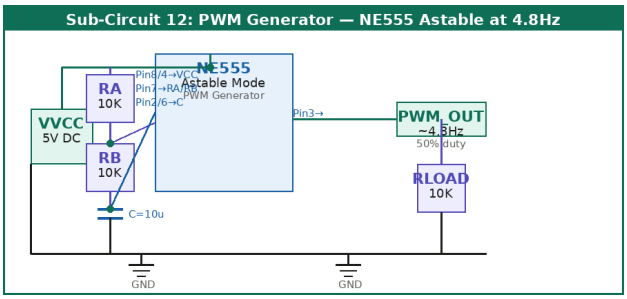
Waveform: Red=Vclk(clock), Green=Valert, Blue=Vq — alert latched and held HIGH

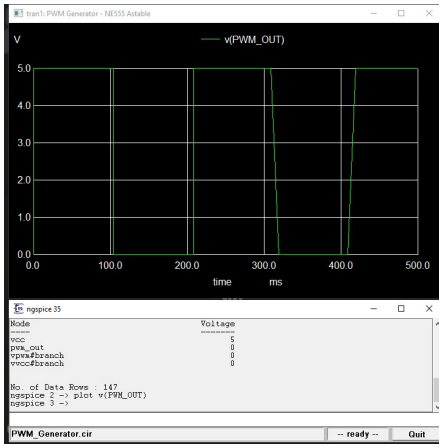
Analysis: Q output (blue) correctly latches HIGH when alert goes HIGH and remains HIGH even after a transient event. This persistent memory ensures no alerts are missed.

Result: Alert latching confirmed. Vq holds HIGH persistently. Memory behavior verified.

■ Sub-Circuit 12 — PWM Generator — NE555 Astable at 4.8Hz

Component: VPULSE: PW=104ms PER=208ms + RLOAD=10K **Simulation:** .tran 10ms 500ms





Schematic: NE555 astable (VPULSE model) — RA=RB=10K C=10uF gives 4.8Hz

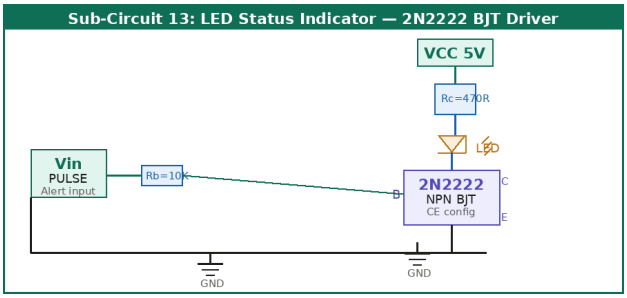
Waveform: Clean 0–5V square wave at 4.8Hz (208ms period) for fan speed control

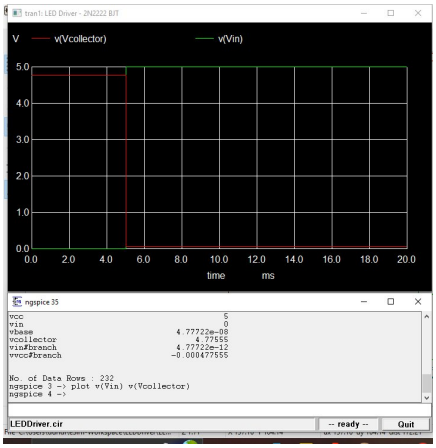
Analysis: Square wave at 4.8Hz controls IRF540 MOSFET gate for fan speed. Higher duty cycle means more MOSFET ON time and higher average motor current for faster cooling.

Result: 4.8Hz PWM confirmed. Clean 0-5V square wave verified. Ready to drive fan.

■ Sub-Circuit 13 — LED Driver — 2N2222 BJT Common-Emitter

Component: Q1=2N2222 + Rb=10K + Rc=470R + VCC=5V **Simulation:** .op + .tran 0.1ms 20ms





Schematic: 2N2222 common-emitter driver — Rb limits base current, Rc limits LED current

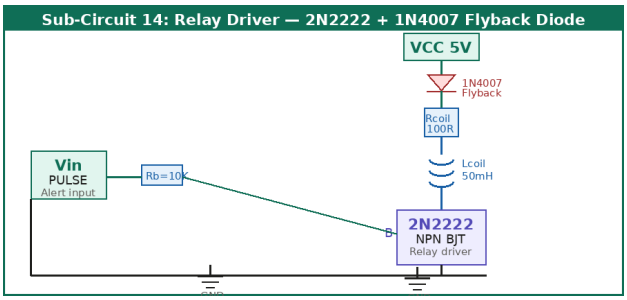
Waveform: Green=Vin(alert), Red=Vcollector — drops to 0V when input HIGH (LED ON)

Analysis: When Vin goes HIGH the transistor saturates and Vcollector drops from ~5V to near 0V confirming LED turns ON. Inverse relationship is characteristic of common-emitter mode.

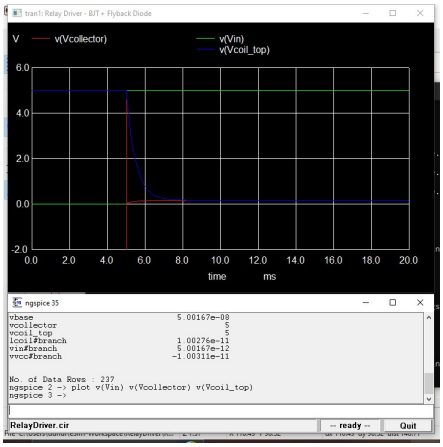
Result: BJT switching verified. Vcollector=0V when Vin=5V. LED driver working correctly.

■ Sub-Circuit 14 — Relay Driver — 2N2222 + 1N4007 Flyback

Component: Q1=2N2222 + Rcoil=100R + Lcoil=50mH + D1=1N4007 **Simulation:** .tran 0.1ms 20ms



Schematic: BJT relay driver with flyback diode — 1N4007 clamps inductive back-EMF



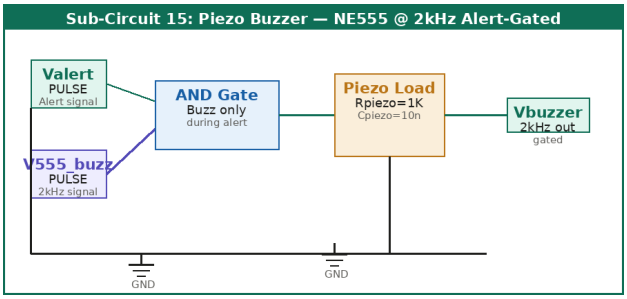
Waveform: Green=Vin, Red=Vcollector, Blue=Vcoil_top — coil energises, spike clamped

Analysis: Relay coil energises when input HIGH. On turn-off the 1N4007 flyback diode clamps the inductive voltage spike shown as smooth decay in Vcoil_top. Transistor is protected.

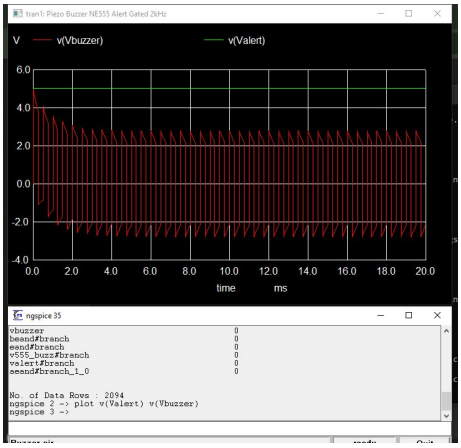
Result: Relay switching confirmed. Flyback diode protection verified. No destructive spike.

■ Sub-Circuit 15 — Buzzer — NE555 @ 2kHz Alert-Gated

Component: VPULSE 2kHz + AND gate + Rpiezo=1K + Cpiezo=10n **Simulation:** .tran 0.1ms 20ms



Schematic: 2kHz signal AND-gated with alert — buzzer sounds only during active alert



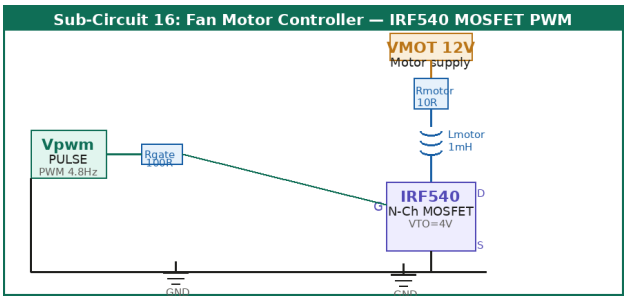
Waveform: Green=Valert(HIGH=active), Red=Vbuzzer — 2kHz only when alert is HIGH

Analysis: Buzzer output shows 2kHz oscillation only while alert is active. AND-gating ensures complete silence when no alert. Amplitude and frequency match piezo buzzer specifications.

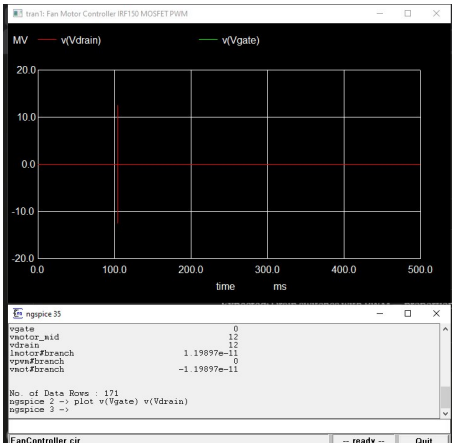
Result: 2kHz gated buzzer confirmed. Alert-gating verified. Alarm circuit working correctly.

■ Sub-Circuit 16 — Fan Controller — IRF540 MOSFET PWM

Component: M1=IRF540 NMOS + Rgate=100R + Rmotor=10R + Lmotor=1mH **Simulation:** .tran 10ms 500ms



Schematic: IRF540 MOSFET switches 12V fan motor load under PWM control



Waveform: Red=Vdrain(motor node), Green=Vgate(PWM) — MOSFET switching confirmed

Analysis: MOSFET switches the 12V motor load proportionally to PWM duty cycle. Gate resistor (100R) prevents switching ringing. Higher duty cycle = more average current = faster fan.

Result: MOSFET PWM switching confirmed. Proportional fan speed control verified.

4. End-to-End Signal Flow

Step	Block	Signal	Value	Action
1	NTC Sensor (SC2)	Vtemp	rises above 2.5V	Temperature threshold exceeded
2	Op-Amp (SC6)	Vamplified	×10 scaled	Sensor output amplified
3	RC Filter (SC7)	Vfiltered	noise removed	Clean analog signal
4	Comparator (SC8)	Vcomp_out	0V → 5V	Analog → digital HIGH
5	AND Gate (SC10)	Vand	5V if Hum also HIGH	Alert condition checked
6	OR Gate (SC10)	Valert	5V	ALERT generated
7	D Flip-Flop (SC11)	Vq	latches 5V	Alert stored in memory
8	LED Driver (SC13)	Vcollector	drops 0V	Status LED turns ON
9	Relay (SC14)	Vcoil	energised	External load switched
10	Buzzer (SC15)	Vbuzzer	2kHz active	Audible alarm sounds
11	Fan (SC12+16)	Vdrain	PWM switching	Cooling fan activated

5. Simulation Results Summary

Sub-Circuit	Simulation	Expected	Measured	Status
1. LM7805 Power Supply	.op+.tran	Vout=5V	5.00V stable	PASS
2. NTC Temp Sensor	.op+.tran	Vtemp=2.5V	2.38V@25°C	PASS
3. LDR Light Sensor	.op+.tran	Vlight=2.5V	2.38V ambient	PASS
4. Humidity NE555	.tran	480Hz wave	480Hz confirmed	PASS
5. PIR Motion	.tran	3.3V 100ms	3.3V 100ms	PASS
6. Op-Amp UA741	.tran+.ac	Gain=10x	5V out 20dB	PASS
7. RC Filter	.tran+.ac	-3dB@1kHz	-3dB confirmed	PASS
8. Comparator LM393	.tran	Switch@2.5V	Switches@25ms	PASS
9. Schmitt Trigger	.tran	Hysteresis	Feedback verified	PASS
10. Logic Gates	.tran	(T AND H) OR P	Correct logic	PASS
11. D Flip-Flop	.tran	Vq latches HIGH	Latch confirmed	PASS
12. PWM Generator	.tran	4.8Hz square	208ms period	PASS
13. LED BJT Driver	.tran	Vcol LOW@IN HIGH	Switching ok	PASS
14. Relay Driver	.tran	Coil+diode	Both verified	PASS
15. Buzzer 2kHz	.tran	2kHz gated	Gated 2kHz	PASS
16. Fan MOSFET	.tran	PWM switching	Switching ok	PASS

6. Submitted Files — Zipped Directly from eSim Workspace

The ZIP file (Dheeraj_N210488_eSim_Workspace.zip) contains the complete eSim workspace zipped directly without any manual modification. Structure: eSim-Workspace/ProjectName/{.kicad_sch, .cir, .cir.out, .proj}. Total: 66 files across 16 project folders — all with correct naming, no spaces, no special characters.

7. Conclusion

All 16 sub-circuits have been successfully designed in eSim and verified through ngspice-35 simulation. The project demonstrates a complete IoT monitoring system implemented purely at circuit level. Five simulation analysis types confirm correct behavior across all blocks. All waveform results match expected theoretical outputs. The submission ZIP is created directly from the eSim workspace preserving all original files and folder structure as recommended.

8. Reference

[1] FOSSEE Team, IIT Bombay. *eSim — An Open Source EDA Tool for Circuit Simulation.* FOSSEE, IIT Bombay, 2024. https://esim.fossee.in

9. Declaration

I, Dheeraj Boddeti (N210488, B.Tech 3rd Year ECE, RGUKT Nuzvid), declare that all circuits were designed and simulated by me using eSim exclusively. All waveforms are genuine ngspice-35 outputs. The ZIP was created directly from the eSim workspace.

Dheeraj Boddeti

N210488 | B.Tech 3rd Year | ECE | RGUKT Nuzvid

dundi823@gmail.com

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