Circuit Simulation Project

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Analog Implementation of PS/2 Communication Protocol Using Open-Drain NMOS

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Title of the Circuit : Analog Implementation of PS/2 Communication Protocol Using Open-Drain NMOS

Theory:

The PS/2 protocol is a synchronous serial communication standard originally developed by IBM for connecting keyboards and mice to personal computers. It operates over two dedicated signal lines — CLOCK and DATA — both of which follow an open-drain bus topology. This means any device on the bus can pull the line LOW, while external pull-up resistors passively maintain the HIGH state when no device is driving the line.

Data is transmitted in 11-bit frames consisting of a Start bit (logic 0), eight data bits sent LSB first, one odd parity bit, and a Stop bit (logic 1). The receiver samples the DATA line on every falling edge of the CLOCK signal, ensuring synchronization between the two lines. The clock frequency typically ranges between 10 kHz and 16.7 kHz, corresponding to a bit period of approximately 60 µs to 100 µs.

In this implementation, the PS/2 protocol is modeled entirely using analog components within the eSim environment. NMOS transistors operating in open-drain configuration serve as the bus drivers — they pull the respective lines LOW when their gate voltage is HIGH, and allow the pull-up resistors to restore the line to HIGH when the gate is LOW. The CLOCK signal is generated using a VPULSE source, while the DATA signal is produced using a PWL (Piecewise Linear) source that encodes the exact PS/2 frame for the byte 0x5A. The synchronization between these two signals is verified through Ngspice transient simulation.

Principle of Operation:

Open-Drain Bus Topology: Both the CLOCK and DATA lines operate in an open-drain configuration. NMOS transistors (MN1 for DATA, MN2 for CLOCK) pull the respective lines LOW when driven by a HIGH gate signal. Pull-up resistors Rdata and Rclk (each 4.7 kΩ) connected to VDD (5 V) restore the lines to HIGH when the NMOS transistors are OFF. This faithfully replicates the wired-AND behavior of a real PS/2 bus.
Clock Generation: A VPULSE source (Vclk) drives the gate of NMOS transistor MN2 through the Clock Generator subcircuit. The resulting CLOCK_LINE signal is the open-drain output — an inverted square wave at approximately 10 kHz (100 µs period, 0–5 V swing).
Data Generation: A PWL source (Vdata) drives the gate of NMOS transistor MN1 through the Data Generator subcircuit. The PWL waveform encodes the complete 11-bit PS/2 frame for the byte 0x5A (LSB first): Start=0, Data bits = 0,1,0,1,1,0,1,0, Parity=1 (odd), Stop=1. Each bit is held stable for one full clock period (100 µs).
Receiver (Waveform-Based Sampling): The receiver in this analog implementation consists of voltage probe nodes (plot_v1) placed directly on the CLK_LINE and DATA_LINE nets. The DATA_LINE is monitored at every falling edge of CLOCK_LINE to decode the transmitted PS/2 frame. This waveform-based sampling approach is well-suited for the eSim/Ngspice environment where analog waveforms can be visually inspected and decoded from the simulation output.
Frame Synchronization: DATA is stable and settled before each falling edge of CLOCK, satisfying the PS/2 setup and hold timing requirements. The idle state of both lines is HIGH (~5 V), maintained by the pull-up resistors.

Nomenclature:

Transmitter Side

- **Vclk (VPULSE):** Clock source — generates a 10 kHz square wave (0–5 V) to drive the CLOCK line through the open-drain NMOS MN2.
- **Vdata (PWL):** Data source — encodes the PS/2 frame for 0x5A as a piecewise linear voltage waveform driving NMOS MN1.
- **MN1 (nmos4):** Open-drain NMOS transistor for the DATA line.
- **MN2 (nmos4):** Open-drain NMOS transistor for the CLOCK line.
- **Rclk (4.7 kΩ):** Pull-up resistor for the CLOCK_LINE, connected to VDD.
- **Rdata (4.7 kΩ):** Pull-up resistor for the DATA_LINE, connected to VDD.
- **VDD (5 V DC):** Supply voltage — also sets the HIGH logic level for both bus lines.

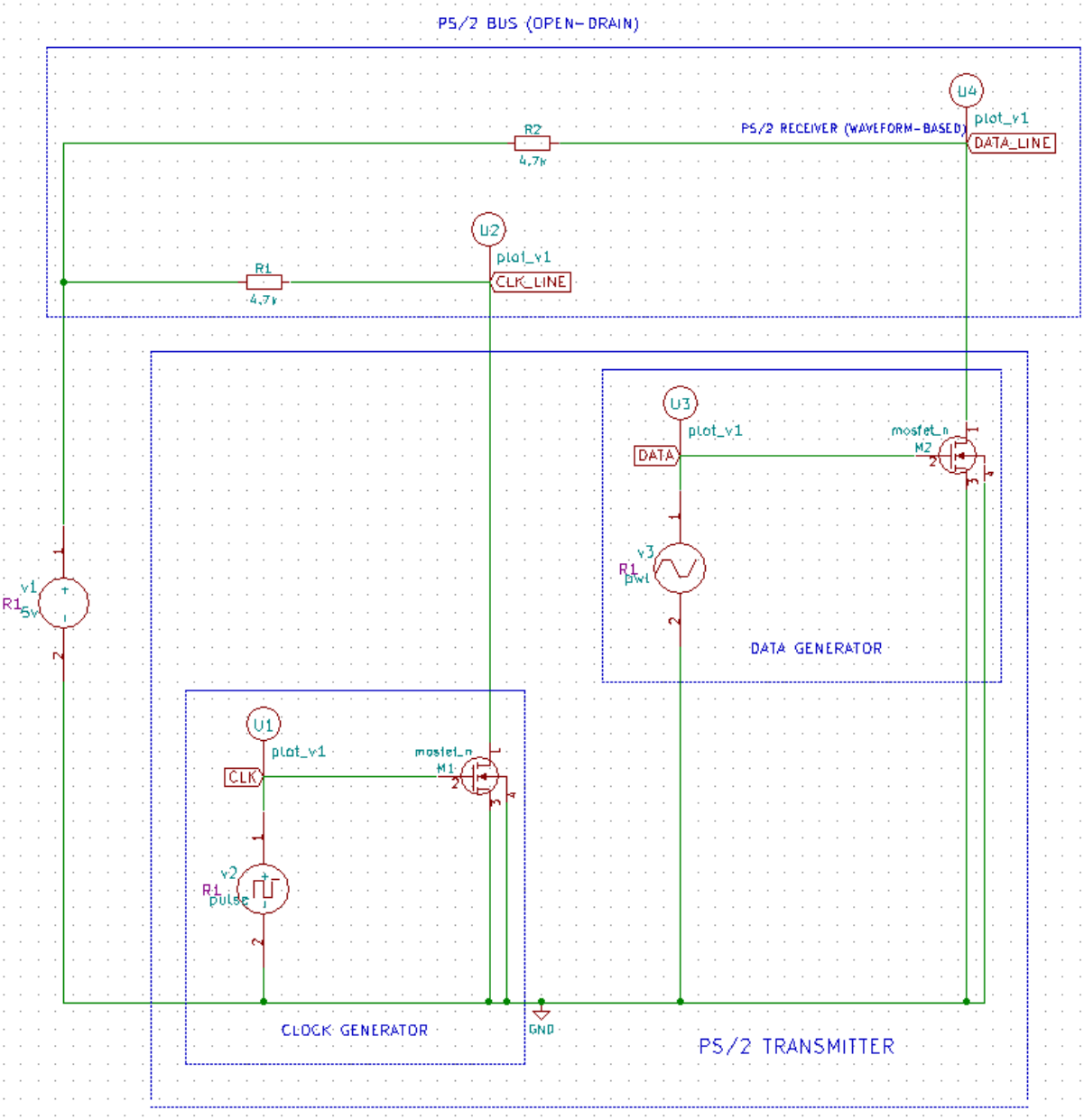
Bus Lines

- **CLOCK_LINE:** Open-drain clock output — square wave, ~10 kHz, 0 V (LOW) to ~5 V (HIGH).
- **DATA_LINE:** Open-drain data output — step waveform encoding the PS/2 frame, 0 V (LOW) to ~5 V (HIGH).

Receiver Side

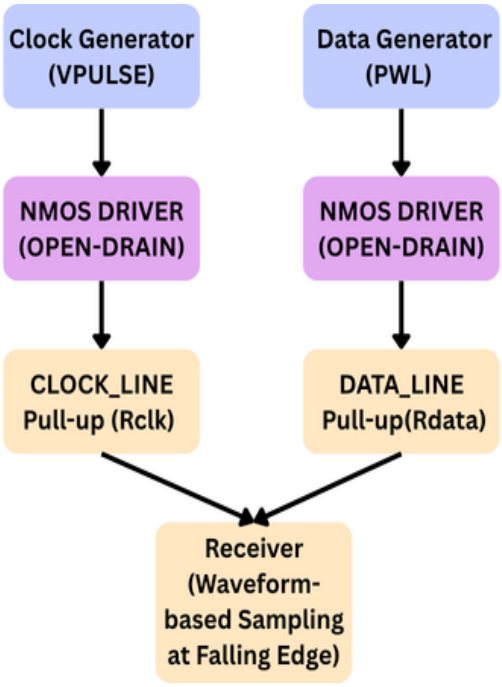
- **CLK_LINE probe (U2 plot_v1):** Voltage monitor on the CLOCK_LINE net for waveform observation.
- **DATA_LINE probe (U4 plot_v1):** Voltage monitor on the DATA_LINE net for waveform observation and bit decoding at falling clock edges.

Circuit Diagram:



PS/2 Transmitter — contains the Clock Generator subcircuit (Vclk VPULSE source + NMOS MN2) and the Data Generator subcircuit (Vdata PWL source + NMOS MN1), both sharing a common GND.
PS/2 Bus (Open-Drain) — the top-level bus with pull-up resistors Rclk and Rdata connected between VDD and the CLOCK_LINE and DATA_LINE nets respectively.
PS/2 Receiver (Waveform-Based) — voltage probe nodes U2, U3, U4 placed on CLK_LINE, DATA, and DATA_LINE for Ngspice output plotting.

Block Diagram:



PS/2 Frame Encoding for 0x5A:

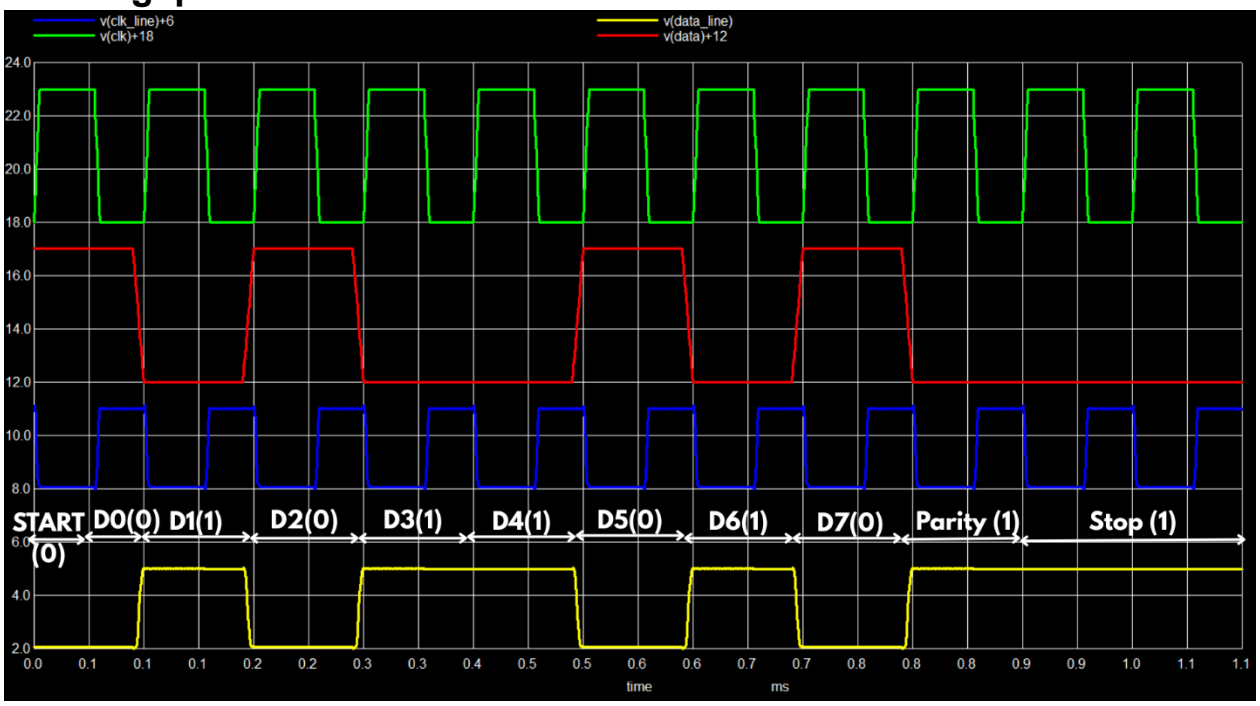
The byte 0x5A = 0101 1010 in binary. Transmitted LSB first over the PS/2 DATA line, the complete 11-bit frame is:

Bit Position	Bit Name	Value	Voltage on DATA_LINE
1	Start Bit	0	LOW (0 V)
2	D0 (LSB)	0	LOW (0 V)
3	D1	1	HIGH (~5 V)
4	D2	0	LOW (0 V)
5	D3	1	HIGH (~5 V)
6	D4	1	HIGH (~5 V)
7	D5	0	LOW (0 V)
8	D6	1	HIGH (~5 V)
9	D7 (MSB)	0	LOW (0 V)
10	Parity	1	HIGH (~5 V)
11	Stop Bit	1	HIGH (~5 V)

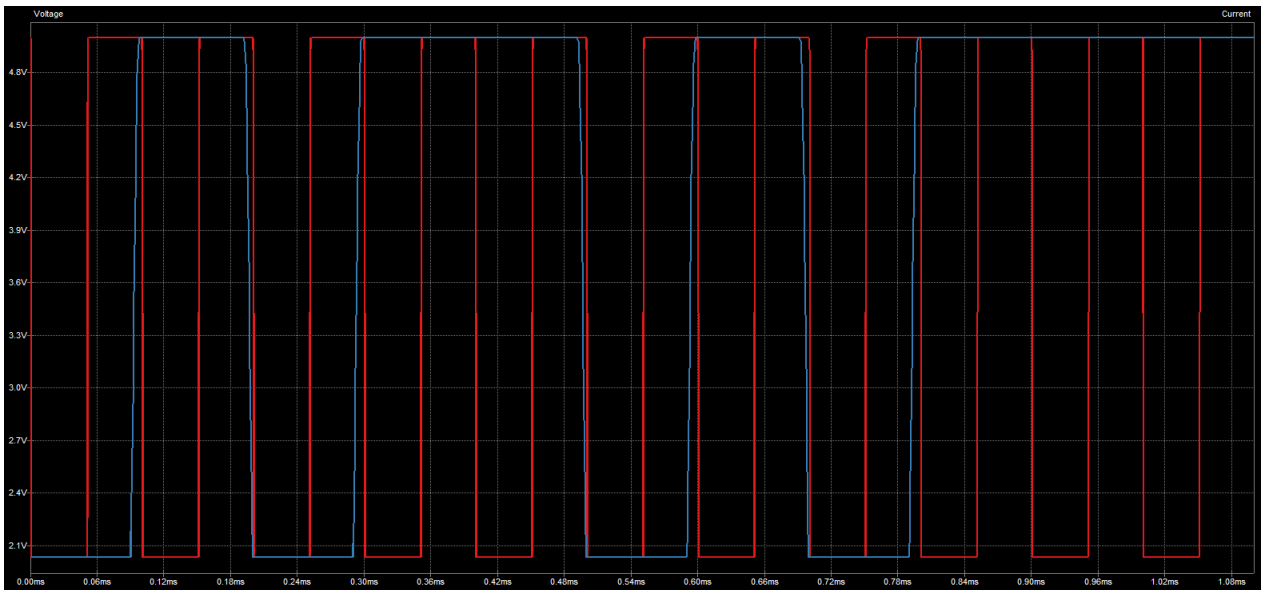
Odd parity verification:
Data bits contain 4 ones (D1, D3, D4, D6) → parity bit = 1 → total ones = 5 (odd)

Simulation Results :

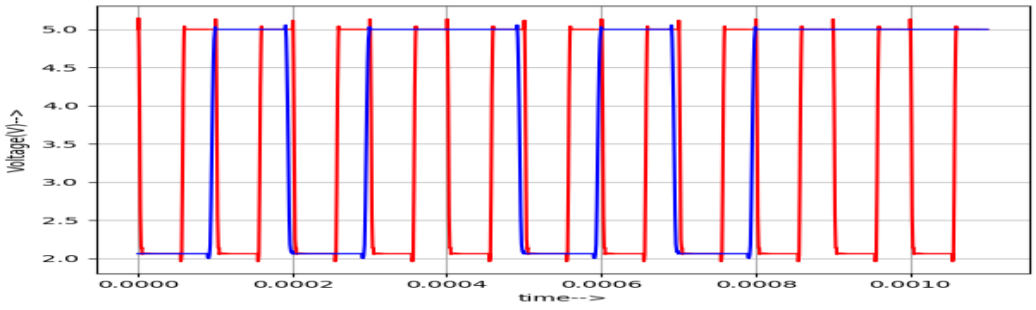
eSim Ngspice:



eSim Simulator:



eSim Python Plot:



Validation:

The simulation waveforms confirm the following:

- **Correct bit sequence:** Decoding DATA_LINE at each CLOCK_LINE falling edge yields the exact 11-bit sequence for 0x5A: Start=0, Data=01011010 (LSB first), Parity=1, Stop=1.
- **Timing alignment:** DATA_LINE is stable and settled before every falling edge of CLOCK_LINE, satisfying PS/2 protocol setup requirements.
- **Open-drain operation verified:** Both CLOCK_LINE and DATA_LINE exhibit correct open-drain behavior — NMOS transistors pull lines LOW, pull-up resistors restore HIGH.
- **Odd parity confirmed:** Four HIGH data bits (D1, D3, D4, D6) plus Parity=1 gives five total HIGH bits — odd parity is correctly implemented and verified.
- **Idle state correct:** Both lines rest at ~5 V (HIGH) before and after transmission, maintained by R1 and R2.
- **No floating nodes:** All nets are properly terminated; NMOS body pins connected to GND, no undefined voltage nodes observed in simulation.

Conclusion:

This project successfully demonstrates the analog implementation of the PS/2 communication protocol at the circuit level using eSim and Ngspice. The open-drain NMOS transmitter circuit accurately drives both the CLOCK and DATA lines of the PS/2 bus, and the Ngspice transient simulation confirms correct transmission of the byte 0x5A (0101 1010) as an 11-bit PS/2 frame with valid Start bit, correct data bits in LSB-first order, verified odd parity, and proper Stop bit. The waveform-based receiver decodes the data correctly by sampling DATA_LINE at each falling edge of CLOCK_LINE, consistent with the PS/2 protocol specification. The eSim tool proved highly effective for circuit-level modeling and verification of this analog communication protocol without requiring physical hardware.

References:

1.Adam Chapweske, "The PS/2 Mouse/Keyboard Protocol" — The most widely cited technical reference on PS/2 signal-level and protocol details.
URL: https://www.burtonsys.com/ps2_chapweske.htm
2.Wikipedia, "PS/2 Port" — Overview of PS/2 port history, electrical interface, and protocol behavior.
URL: https://en.wikipedia.org/wiki/PS/2_port