Design and Simulation of One-Wire Communication Protocol Transmitter–Receiver Circuit Using eSim

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Title of the circuit:

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Theory:

The One-Wire communication protocol, originally developed by Dallas Semiconductor (now Maxim Integrated/Analog Devices), provides a cost-effective and hardware-efficient means of serial communication between a master device and one or more slave devices over a single bidirectional data line (DQ) and a shared ground reference. Its minimalist bus architecture makes it particularly attractive in embedded systems, sensor interfacing, and IoT applications where pin count and wiring complexity must be kept to a minimum.

The protocol operates on an open-drain bus topology. In this configuration, no device actively drives the line HIGH; instead, devices are only capable of pulling the DQ line LOW through their open-drain or open-collector outputs. A passive pull-up resistor — typically in the range of 1 kΩ to 4.7 kΩ — connected between the DQ line and the supply voltage (VCC) restores the bus to a logic HIGH state whenever no device is asserting a LOW. This eliminates bus contention and allows multiple devices to coexist on the same wire without requiring explicit arbitration logic.

Communication in the One-Wire protocol is entirely timing-driven. The master device governs all transactions and begins every communication session with a reset pulse — holding the DQ line LOW for a minimum of 480 µs. This resets all slave devices on the bus. Following the reset, the master releases the line, and any present slave device responds within 15–60 µs by asserting its own presence pulse — pulling DQ LOW for 60–240 µs. This handshake confirms the slave's availability before any data transfer begins.

Data transmission follows a time-slot encoding scheme. Each bit occupies a precisely defined time slot of approximately 60–120 µs. A logic '1' is encoded by pulling the line LOW for a very short duration (1–15 µs) and then releasing it HIGH for the remainder of the slot. A logic '0' is encoded by holding the line LOW for the entire slot duration (approximately 60 µs or more). The receiving device samples the DQ line approximately 15–30 µs after the start of each time slot, well within the low-pulse window for a '1', to correctly interpret the transmitted bit value.

This simulation models the complete One-Wire communication pipeline — comprising the transmitter (master), the shared open-drain DQ bus, and the receiver (slave) — to validate the protocol's correct functional implementation using discrete analog components in the eSim/Ngspice mixed-signal environment.

Principle of Operation

Open-Drain Bus Architecture All devices on the One-Wire bus interface through open-drain transistor outputs. No device actively sources current to the line; they only sink current to pull the line LOW. The pull-up resistor passively maintains the bus at logic HIGH in the absence of any active pull-down, ensuring clean idle states and preventing electrical conflicts between devices.

Reset and Presence Detection Every communication session is initiated by the master, which asserts a reset pulse by holding DQ LOW for a minimum of 480 µs. Upon release, the master briefly switches to input mode. A slave device, detecting the rising edge of the line, waits 15–60 µs before asserting a presence pulse — pulling DQ LOW for 60–240 µs — to signal its readiness. This bidirectional handshake is fundamental to reliable One-Wire communication and ensures synchronization between master and slave before data exchange begins.

Time-Slot Based Bit Encoding Data is transmitted one bit per time slot. The master initiates each slot by pulling DQ LOW. The duration of the LOW phase encodes the bit value: a short pulse (1–15 µs) represents logic '1', while a sustained LOW (≥60 µs) represents logic '0'. The

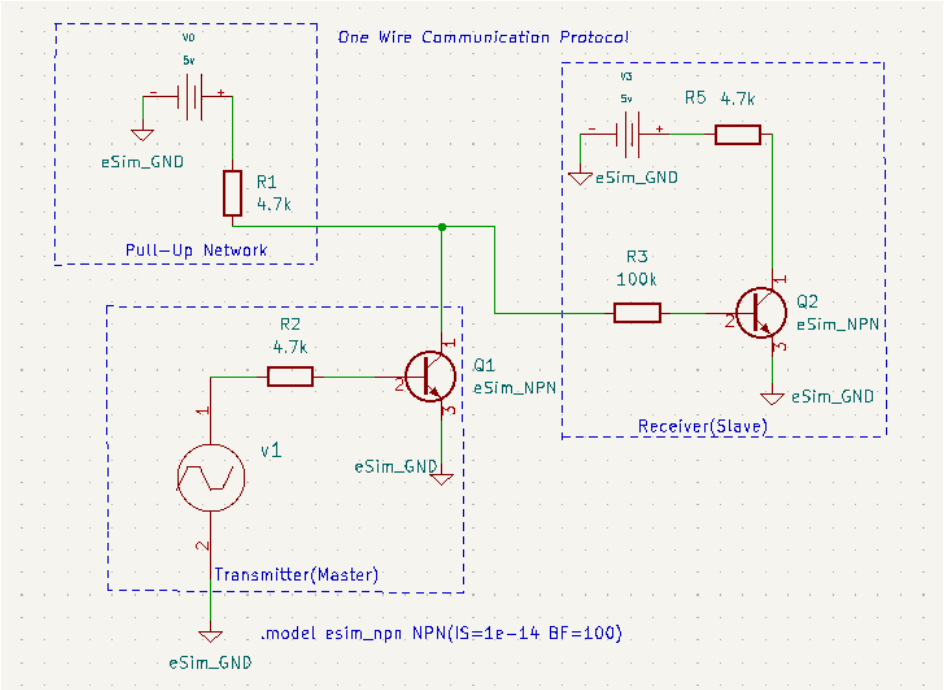
slave samples the line midway through the slot (~30 µs after the falling edge) to determine the bit value accurately, independent of minor timing variations.

High-Impedance Idle State When the bus is not actively being driven, all connected devices present a high-impedance state to the DQ line. The pull-up resistor holds the bus at VCC during this idle period. This prevents spurious switching, reduces power dissipation, and maintains bus integrity between transactions.

Receiver Reconstruction Logic The receiver monitors the DQ line and distinguishes logic '1' from logic '0' based on the measured duration of each LOW pulse. Due to the open-drain topology and the inverting nature of the NPN transistor switch used in the receiver stage, the output signal at OUT_RX is the logical complement of the DQ bus signal — HIGH when DQ is LOW, and LOW when DQ is HIGH. This inversion is a predictable and well-documented characteristic of the circuit topology and is accounted for in the protocol's data recovery logic.

Single-Master Architecture The One-Wire protocol follows a strict master-initiated communication model. The slave device never transmits data unsolicited; it only responds when addressed and commanded by the master. This deterministic control structure eliminates collision risks on the shared data line and simplifies timing analysis, making the protocol highly reliable even without complex arbitration mechanisms.

Schematic Diagram (eSim)



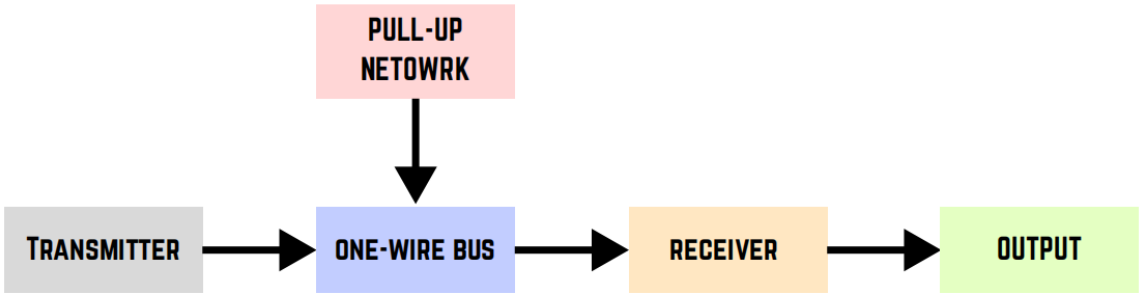
The circuit is implemented in eSim and is organized into three clearly delineated functional stages, all sharing a common DQ node that represents the One-Wire communication bus:

1. **Pull-Up Network** — A 5V supply (V0) and pull-up resistor R2 (4.7 kΩ) passively hold the DQ line at logic HIGH during idle and recovery intervals.

2. **Transmitter Stage (Master)** — An NPN transistor Q1 (eSim_NPN) driven through a base resistor R1 (4.7 kΩ) by a PWL voltage source V1, implementing open-drain bus driving behaviour.

3. **Receiver Stage (Slave)** — An NPN transistor Q2 (eSim_NPN) with its base connected to the DQ line through a high-value resistor R3 (100 kΩ), and a collector pull-up resistor R5 (4.7 kΩ) connected to a 5V supply (V3), producing the reconstructed output at OUT_RX.

Block Diagram:



The transmitter generates timing pulses. The One-Wire bus carries communication signals. The receiver detects LOW pulse durations and reconstructs digital data at the output.

Circuit Description

Transmitter Section

The transmitter is built around a PWL (piecewise linear) voltage source V1, which generates the precise timing waveforms required by the One-Wire protocol — including the reset pulse, recovery period, and individual data bit slots. V1 drives the base of NPN transistor Q1 through base resistor R1 (4.7 kΩ), which limits base current and protects the transistor from excessive drive.

When V1 outputs a HIGH voltage, Q1 is driven into saturation, presenting a near-short circuit between its collector and emitter. This pulls the DQ node firmly to ground (logic LOW), asserting a bus LOW regardless of the pull-up network. When V1 returns to LOW, Q1 enters cutoff and its collector-emitter path becomes effectively open-circuit. The pull-up resistor R2 then restores DQ to VCC (logic HIGH). This interaction between Q1 (active pull-down) and the pull-up resistor R2 (passive pull-up) implements the open-drain behaviour that is fundamental to the One-Wire protocol.

The transistor model used is esim_npn with parameters IS = 1×10^{-14} and BF = 100, which provides realistic switching characteristics and ensures decisive saturation and cutoff transitions across the timing windows used in this simulation.

Receiver Section

The receiver stage employs NPN transistor Q2, whose base is connected to the DQ line through a high-value resistor R3 (100 kΩ). This resistor limits the base drive current and prevents Q2 from loading the DQ bus, which could distort the very timing characteristics that carry the encoded data.

When DQ is LOW (Q1 conducting), the base of Q2 receives insufficient forward bias and Q2 remains in cutoff. With Q2 off, its collector is pulled HIGH by R5 (4.7 kΩ), making OUT_RX HIGH. Conversely, when DQ is HIGH (idle or recovery state), Q2 is forward-biased into saturation through R3, pulling OUT_RX LOW. This produces the expected logical inversion at the receiver output — a natural consequence of the open-drain topology and NPN transistor switching.

The presence pulse detection stage (slave responding to master reset) is not explicitly implemented in this simulation but can be incorporated in a future extension by adding a timed pull-down circuit on the slave side triggered by the falling edge of the master's release. The presence pulse stage is not explicitly implemented in this simulation and can be incorporated as a future extension.

Simulation Results (eSim Ngspice)

A transient analysis was performed using the directive. tran 1u 800us, simulating an 800 µs window sufficient to capture the complete One-Wire communication sequence: initial idle state, reset pulse assertion, bus recovery, and multiple data bit transmissions.

Figure 1: DQ Bus Signal — Complete One-Wire Waveform

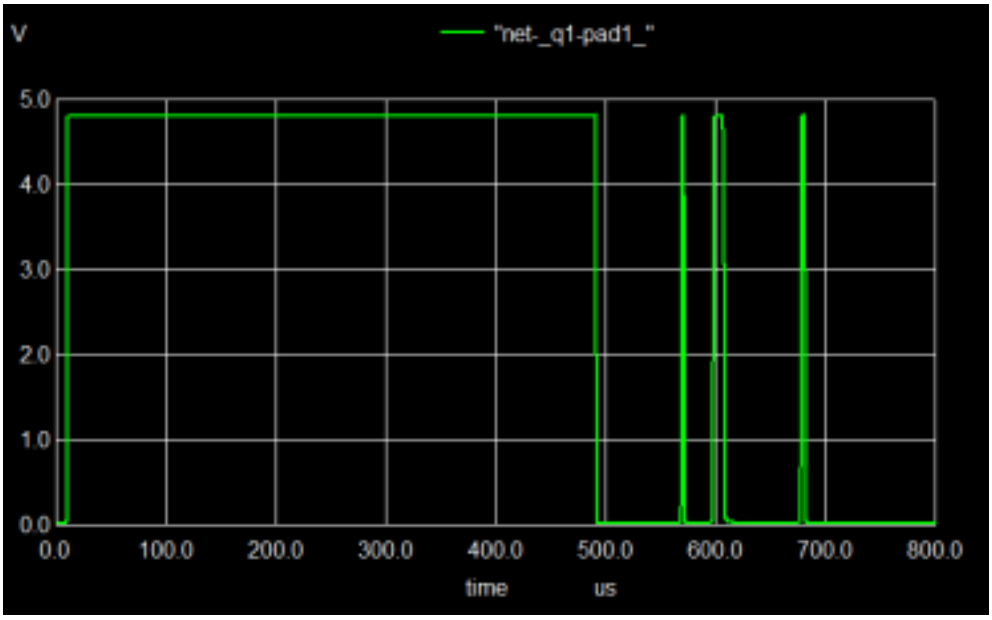


Figure 1: DQ line voltage — shows idle HIGH, reset pulse LOW (~500 µs), recovery HIGH (~580 µs), and data bit pulses

The following table compares expected protocol behaviour with observed simulation results:

Protocol State	Requirement	Observation in Simulation
Idle State	Line HIGH	Initial period
Reset Pulse	~480 µs LOW	~10µs–490µs
Recovery	Line returns HIGH	~500µs
Data Bit 1	Short LOW pulse	~570–580µs
Data Bit 0	Long LOW pulse	~600–660µs
Data Bit 1	Short LOW pulse	~680–690µs
Receiver Output	Correct reconstruction	Matches timing (inverted)

Figure 2: Receiver Output (OUT_RX at Collector of Q2)

The receiver successfully reconstructs transmitted data based on pulse duration.

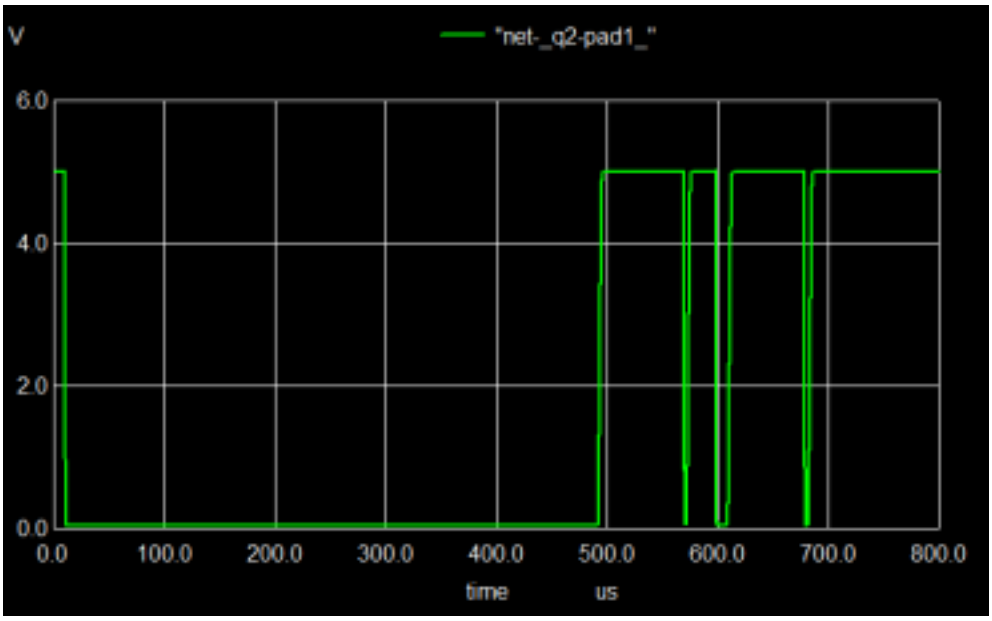


Figure 2: OUT_RX — receiver output, inverted relative to DQ bus; matches expected One-Wire output polarity

Figure 3: Transmitter Input and Receiver Output Waveforms Demonstrating One Wire Data Transmission (Without Reset)

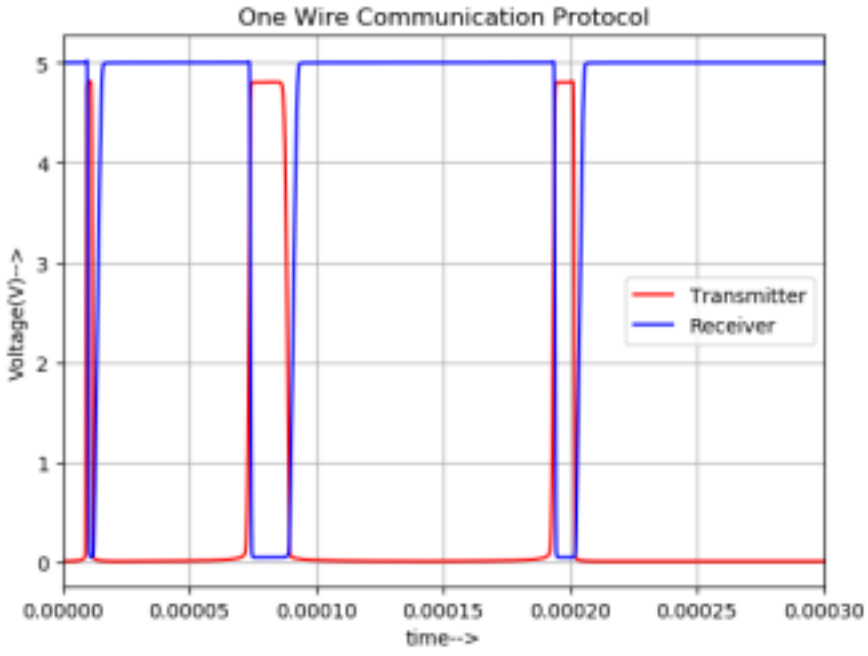


Figure 3: Transmitter Input and Receiver Output — OUT_RX is inverted relative to the input signal and demonstrates correct pulse-width based data reconstruction.

Conclusion:

This simulation successfully demonstrates the complete functional operation of the One-Wire communication protocol in a mixed-signal eSim/Ngspice environment using discrete analog components. The transmitter stage — built around an NPN transistor Q1 driven by a PWL voltage source — accurately generates all required protocol waveforms: the 480 µs reset pulse, bus recovery interval, and individually timed data bit slots. The pull-up resistor (R2 = 4.7 kΩ) reliably restores the DQ bus to logic HIGH during idle and inter-slot recovery periods, in full conformance with the One-Wire specification. The receiver stage (Q2) correctly reconstructs the transmitted bit stream at OUT_RX with the expected inverted polarity, and all simulated timing parameters — reset pulse width, recovery duration, and data bit slot widths align closely with the official One-Wire protocol requirements. The simulation validates the circuit concept for educational and proof-of-concept purposes, confirming that the One-Wire protocol can be faithfully modelled using a minimal set of passive components and NPN transistors in eSim, without requiring any digital logic ICs or microcontrollers. This makes the design particularly valuable as a teaching tool for understanding open-drain bus architectures, time-slot based encoding, and mixed-signal circuit simulation methodology.

Key Achievements:

- Successful open-drain bus implementation using NPN transistor Q1 and hardware pull-up resistor R2 (4.7 kΩ)
- Accurate reset pulse generation (~480 µs) and bus recovery (~500 µs) timing, meeting One-Wire specification
- Correct time-slot encoding demonstrated: short LOW pulse encodes logic ‘1'; long LOW pulse encodes logic '0'
- Functional receiver reconstruction with proper inverted-polarity output at OUT_RX
- All protocol states validated against One-Wire specification timing requirements
- Clean and interference-free DQ bus waveforms with sharp transitions, validating component selection and model parameters

References:

1. Guide to 1-Wire Communication — Analog Devices.

https://www.analog.com/en/resources/technical-articles/guide-to-1wire-communication.html

2. 1-Wire Protocol Overview — Quectel Developer Documentation.

https://developer.quectel.com/doc/quecpython/Application_guide/en/hardware/peripheral interfaces/GPIO_One_wire.html

3. Understanding 1-Wire Communication — Tutorial 1796 — Maxim Integrated.

https://www.maximintegrated.com/en/design/technical-documents/tutorials/1/1796.html

4. Spoken Tutorial Project — eSim: IIT Bombay (eSim installation, schematic entry, and Ngspice simulation tutorials). https://spoken-tutorial.org/