Design and Simulation of UART with Parity Protection and Automated Frame Synchronization.

Theory:

The Universal Asynchronous Receiver-Transmitter (UART) is a serial communication protocol that facilitates data exchange between two devices without the requirement of a shared global clock. In this specific implementation, the system is designed to operate at a **9600 baud rate** using a **7E1 frame format**—consisting of 7 data bits, 1 even parity bit, and 1 stop bit. The timing for each bit is precisely calculated at approximately **104µs**, ensuring that the asynchronous nature of the transmission remains stable and predictable across the mixed-signal simulation environment.

The theoretical foundation of this design relies on hardware-level error detection rather than software-based verification. By utilizing a dedicated XOR Tree Network, the circuit performs a real-time modulo-2 summation of the bitstream to calculate **Even Parity**.

Principle Of Operation:

- **Asynchronous Protocol:** The UART system transmits data serially without a shared global clock. The transmitter (Tx) and receiver (Rx) maintain synchronization by adhering to a pre-defined 9600 baud rate.
- **Frame Structure:** The design is tested for a 9-bit data frame consisting of 7 data bits, 1 even parity bit, and 1 stop bit. Both Tx and Rx lines remain in a logic high state (1) during idle periods.
- **Hardware Parity Protection:** A hardware-based XOR tree is incorporated to generate even parity in real-time. This ensures data integrity by verifying the bitstream during the idle gap between pulses.
- **Automated Start Bit Generation:** The transmitter includes circuitry to automatically generate a "Start Bit" (a high-to-low transition) to signal the beginning of a transmission burst.
- **Start Bit Detection & High Impedance:** The receiver remains in a high-impedance state until the start bit is detected. This "gated-clock" strategy prevents "phantom" bit detection caused by electrical line noise.
- **Error Detection Logic:** The receiver independently calculates the parity of the incoming data and compares it with the parity bit sent by the transmitter.
- **Parity Flagging:** If the calculated and received parity bits match, the Parity_Check flag is set to logic high; in the event of a mismatch (failure), the flag remains at zero

Nomenclature:

Transmitter (Tx) Side

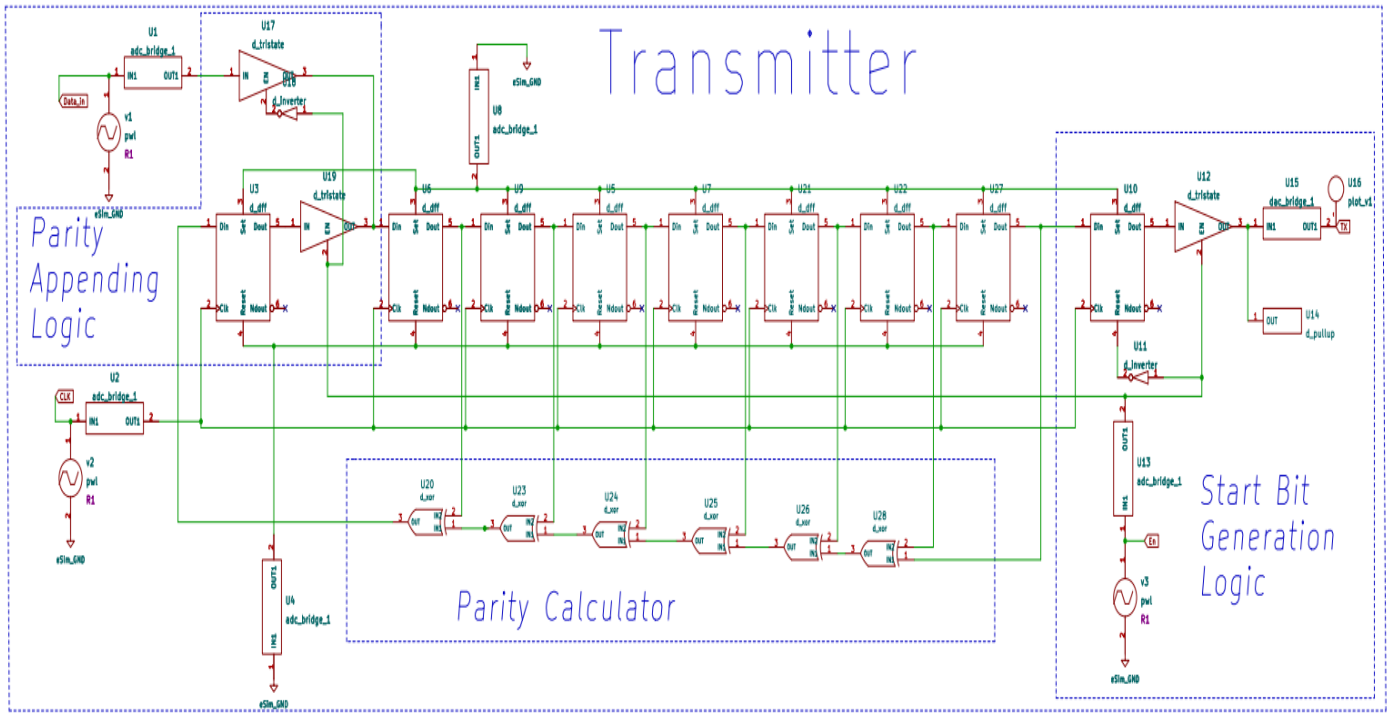
- ***Data_in*:** Parallel input data provided to the transmitter by the microcontroller or user.
- ***CLK*:** Transmitter system clock governing the 9600 baud rate timing (104 micro seconds period).
- ***En*:** Enable signal that initiates data transfer once the bitstream is correctly latched into the internal flip-flops.
- ***Tx*:** The final serial data stream transmitted over the communication line.

Receiver (Rx) Side

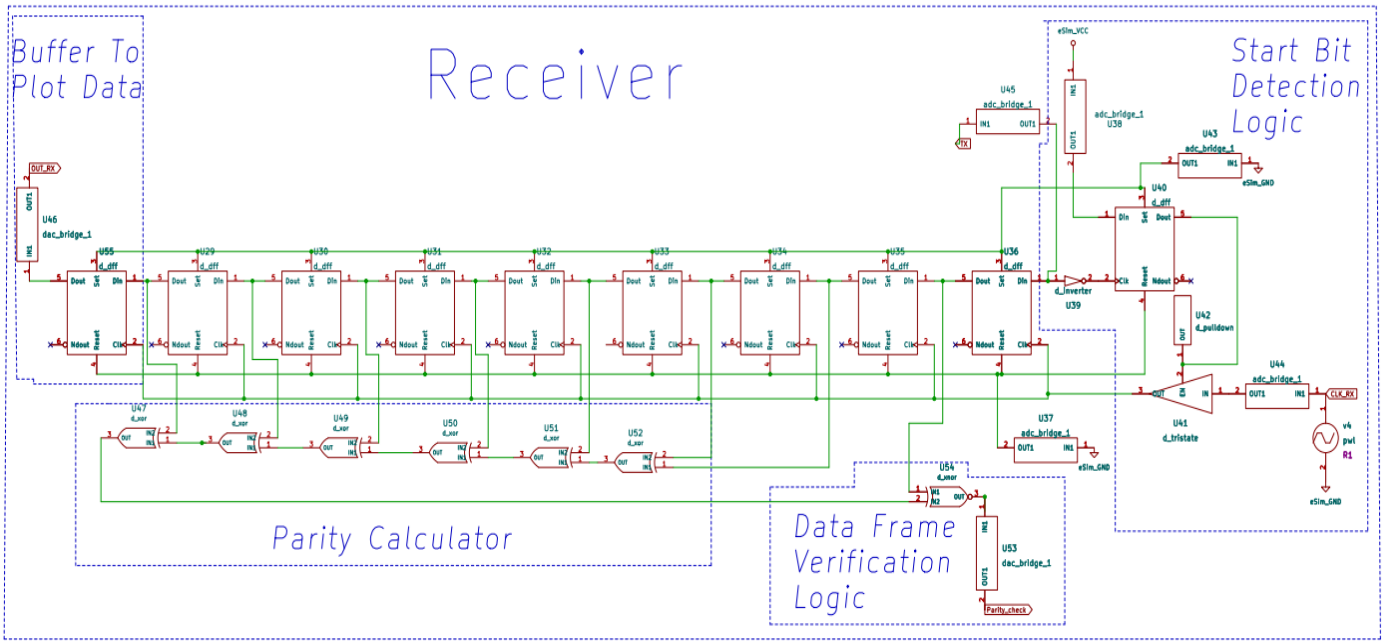
- ***CLK_RX*:** Local receiver clock used for sampling the incoming bitstream.
- ***Tx*:** The serial data received from the transmitter (input connection to the receiver logic).
- ***Out_Rx*:** Parallel output data produced by the receiver once all bits in the frame are successfully processed.
- ***Parity_Check*:** A status flag that validates data integrity by confirming if the receiver's calculated parity matches the transmitter's parity bit.

Schematic Diagram (eSim Kicad):

The circuit schematic of Transmitter is given below:



The circuit schematic of Receiver is given below:



Data Flow and Transmission Sequence:

i. User gives the 7 bit data at ***Data_in*** in transmitter and simultaneously gives 7 clock pulses (104us for 9600 baud rate) to ***CLK.***
ii. Now the parity is calculated at *Parity Calculator* and stored in U3 d-flip-flop.
iii. Once the transmitter receives the ***En*** signal (for plotting purpose it is generated 3 time period after taking input data from user):
    a. The *Parity Appending Logic* stops receiving data from user and appends the parity bit to the 7-bit data.
    b. The start bit is generated using *Start Bit Generation Logic*.
iv. The whole frame (1 start bit + 7 data bit + 1 parity bit) is transmitted at ***Tx***.
v. The receiver remains in high impedance state until it receives the start bit (transition from logic high to logic low) using *Start Bit Detection Logic*
vi. Once the start bit is received the ***CLK_RX*** is given to all the registers of receiver.
vii. The receiver simultaneously calculated the parity of the received data using *Parity Calculator.*
viii. After receiving the complete data packet the *Data Frame Verification Logic* generates ***Parity_check*** flag which is equal to logic high in case of parity matching.
ix. *Buffer To Plot Data* is used to for the sole purpose of plotting data and the data can be obtained ***OUT_Rx.***

Simulation Results (eSim Ngspice):

Figure 1: ***CLK*** Signal (first 7 pulses to populate D flip flops next 8 to transmit data)

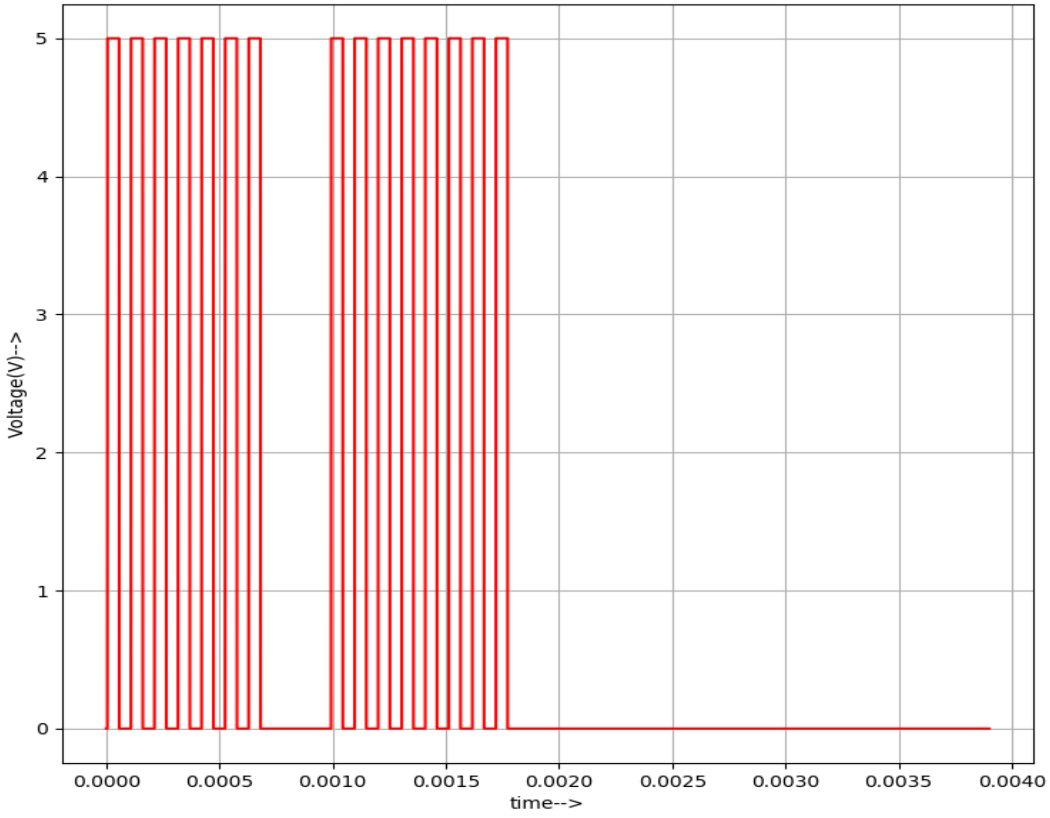


Figure 2: ***DATA_IN*** Signal (7-bit data = 1011010)

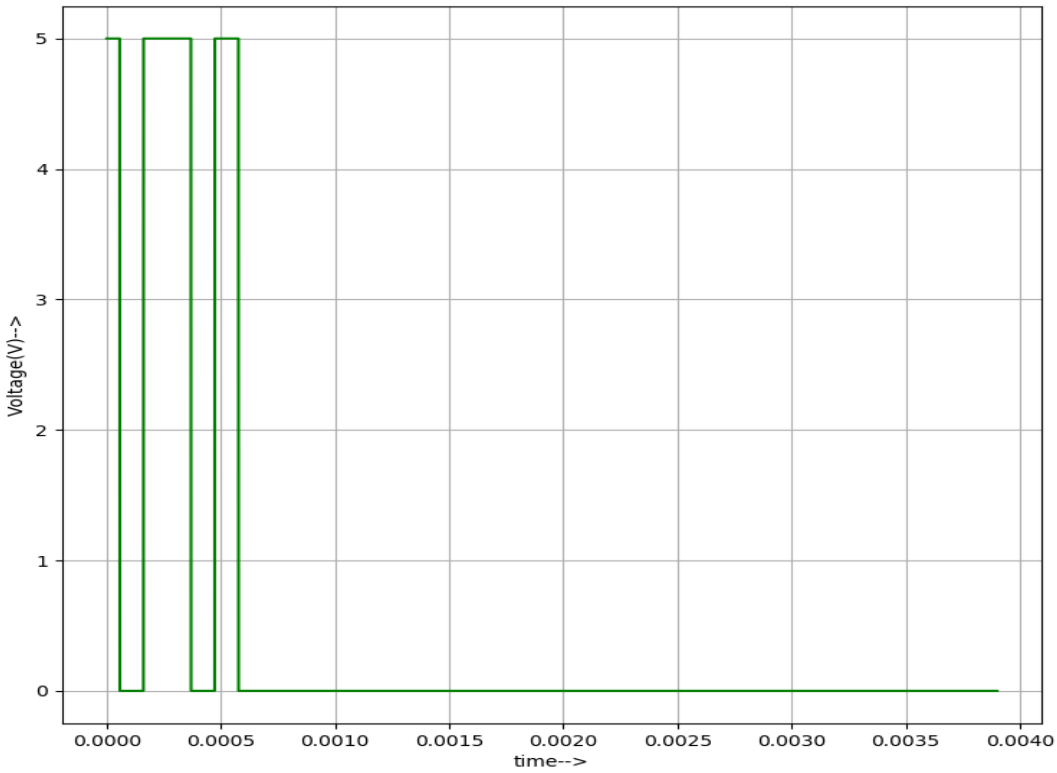


Figure 3: ***En*** Signal (Logic high for the period of data transmission)

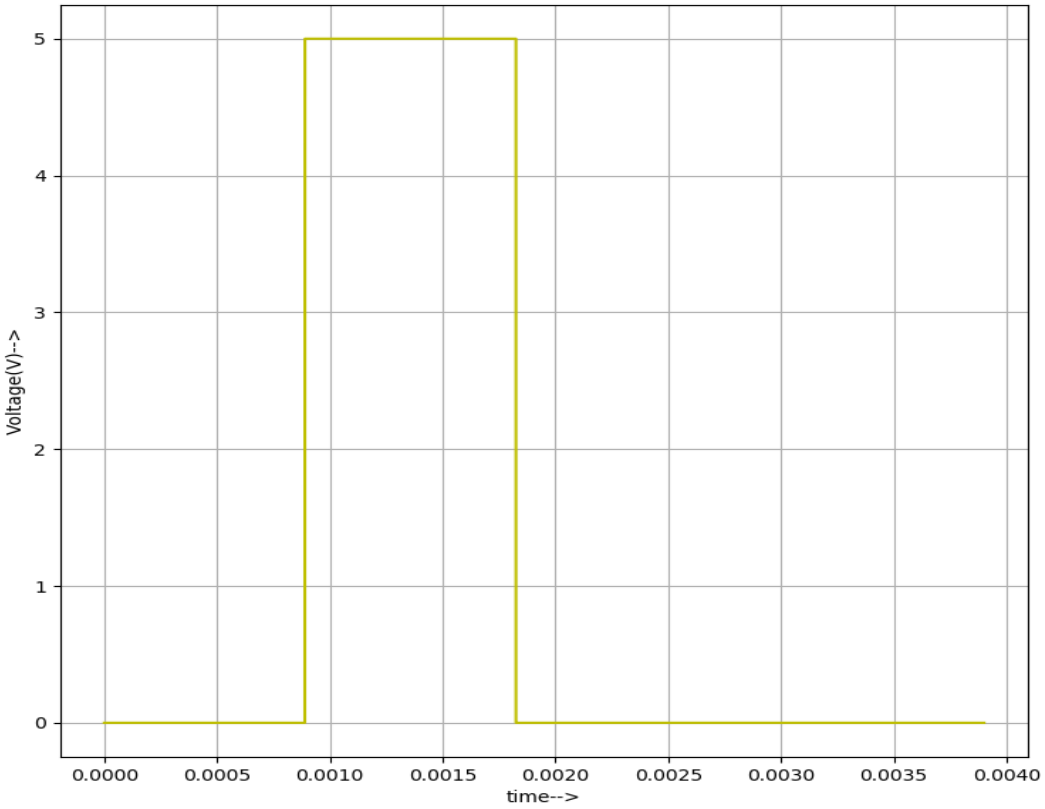


Figure 4: ***Tx*** Signal (Start condition + 7-bit data + Parity bit = 0 + 1011010 + 0)

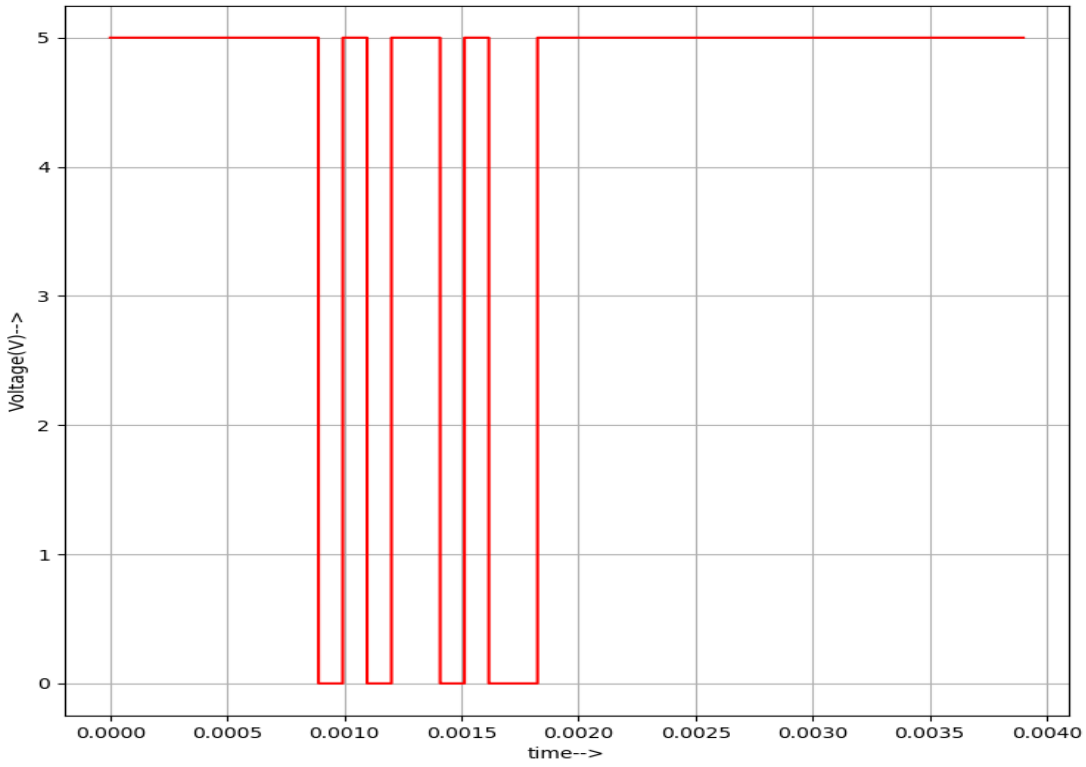


Figure 5: ***CLK_Rx*** Signal (first 8 pulses to populate receiver's D flip flops and next 8 to obtain data

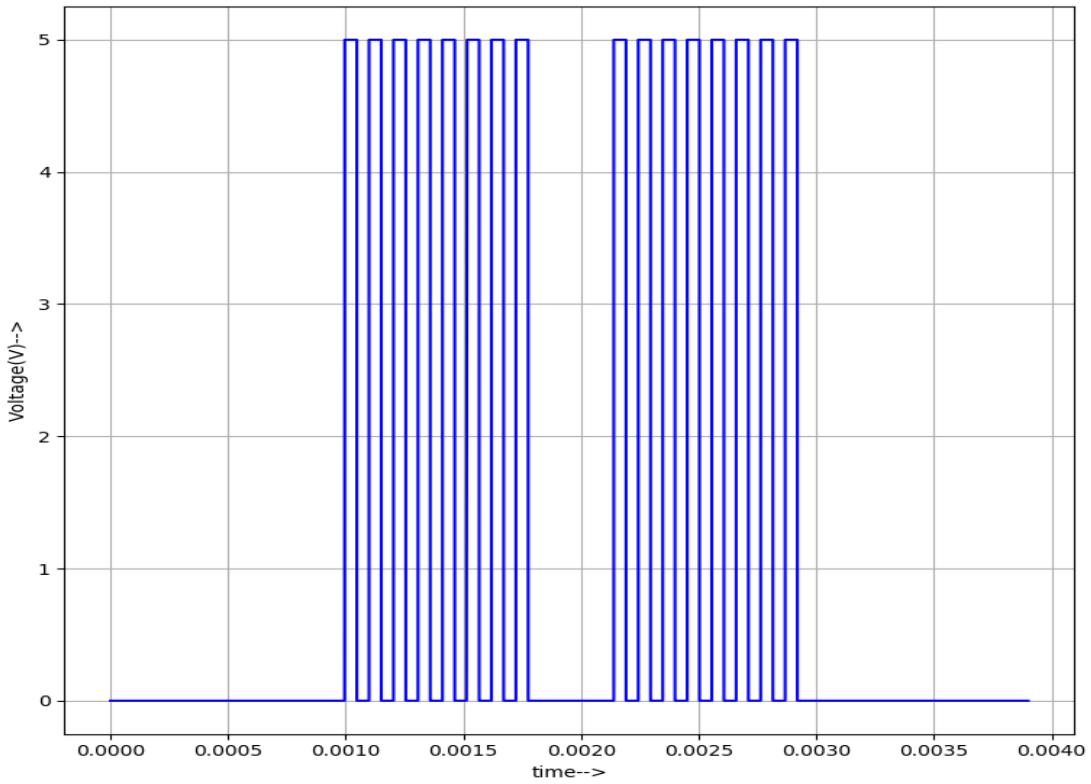


Figure 6: ***OUT_RX*** Signal (7-bit data + parity = 1011010 + 0)

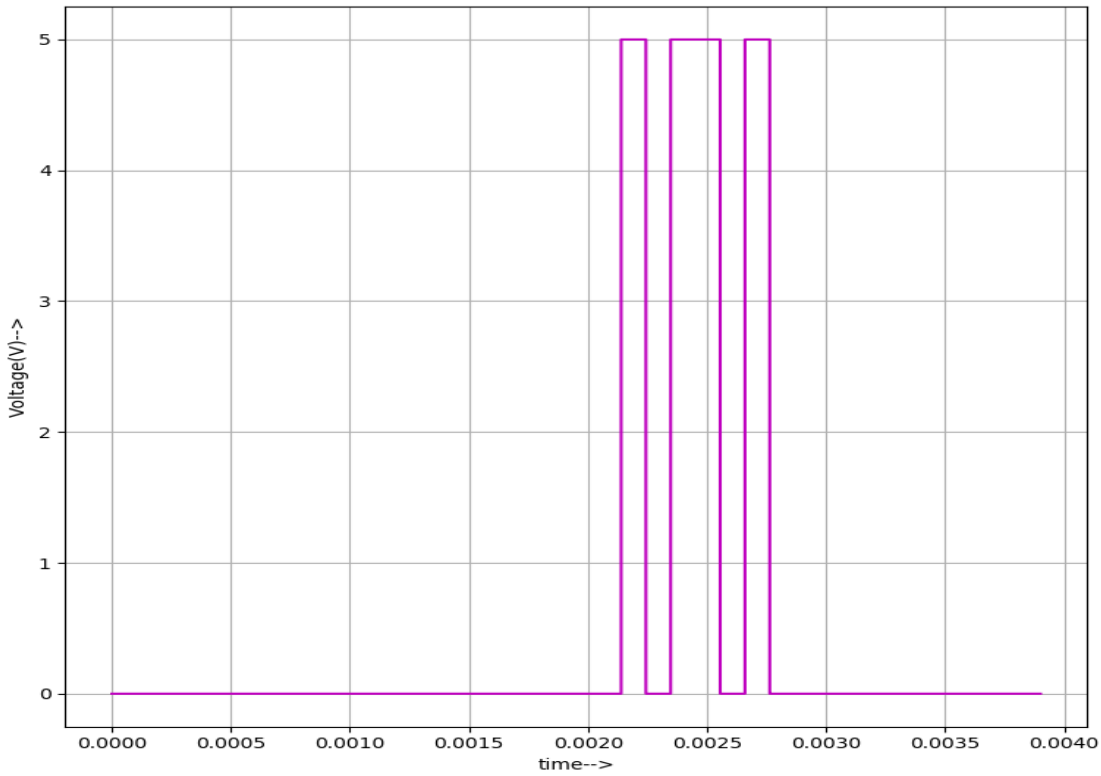
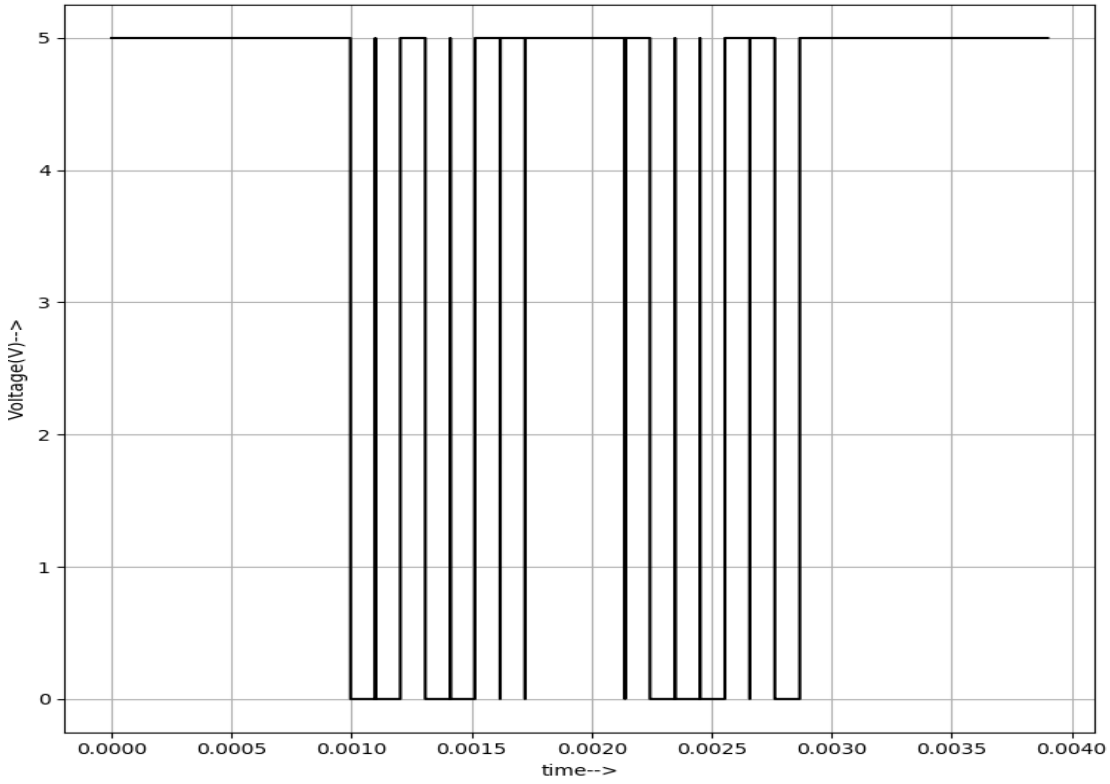


Figure 7: ***Parity_Check*** Signal (Final Value is one, means parity matches and data is valid).



Conclusion :

With this implementation of UART the 7E1 data frame (data = 1011010 + parity = 0) at 9600 baud rate is successfully transferred as well as received while ensuring frame synchronization as well as parity protection.

References :

- Texas Instruments (TI) User Guide (SPRUGP1): Universal Asynchronous Receiver/Transmitter (UART) User's Guide. https://www.ti.com/lit/ug/sprugp1/sprugp1.pdf?ts=1775224645292&ref_url=https%253A%252F%252Fwww.google.com%252F
- FOSSEE eSim User Manual: IIT Bombay (To get familiar with software).
- Ngspice Reference Manual: (Used for calculating precise Piecewise Linear (PWL) coordinates for the 7+8 pulse bursts and the 3-period idle gap).