Circuit-Level Modelling And Verification Of I2S Protocol With Gate-Level Sipo Receiver

1. Theory

The Inter-IC Sound (I²S) protocol is a synchronous serial communication standard developed by Philips Semiconductors, specifically designed for transmitting digital audio data between integrated circuits. Unlike general-purpose serial protocols, I²S separates the serial clock (SCK), word select (WS), and serial data (SD) onto dedicated unidirectional lines, eliminating clock-data jitter and simplifying receiver design. This simulation implements an 8-bit per channel I²S receiver operating at a 1 MHz SCK frequency with a 62.5 kHz Word Select signal, validating stereo audio frame transmission and bit-level data recovery in a mixed-signal SPICE environment using eSim 2.5 and Ngspice.

2. Principle of Operation

- **Synchronous Pipeline:** The core receiver engine is an 8-stage Serial-In Parallel-Out (SIPO) shift register composed of d_dff XSPICE primitives from the eSim digital library. Serial data on the SD line is clocked into the first flip-flop on every rising edge of SCK, and propagates through the cascade, producing an 8-bit parallel word at OUT_0 to OUT_7.
- **Word Select (WS) Framing:** Per the Philips I²S specification, the WS line transitions exactly one SCK clock cycle before the MSB of the next data word. WS = 0 indicates Left Channel data transmission; WS = 1 indicates Right Channel data. With SCK at 1 MHz and WS at 62.5 kHz, each WS period spans exactly 16 SCK cycles - 8 cycles per channel.
- **Hybrid Testbench Architecture:** The transmitter is implemented as a mathematically precise PWL (Piecewise Linear) voltage source generating the SD data stream, synchronized to PULSE sources for SCK and WS. This hybrid approach eliminates SPICE convergence risk while maintaining nanosecond-accurate timing alignment.
- **Channel Separation via Waveform Validation:** Channel separation is achieved via WS-synchronized temporal sampling of SIPO outputs at word boundaries. At the exact falling edge of the WS=0 window (t = 8.0 µs), the SIPO parallel outputs are sampled to extract the Left Channel word. At the rising edge of the WS=1 window (t = 16.0 µs), the Right Channel word is extracted. Hardware latching using WS-derived clocks was intentionally avoided due to the instability of edge-detection and gated-clock structures in XSPICE mixed-signal simulation. This approach fully satisfies the I²S protocol verification requirements without triggering convergence failures.

3. Toolchain Methodology & Schematic-Netlist Variance

Note on Toolchain Methodology: Due to strict node-validation rule changes in KiCad 8.0, exporting legacy eSim 2.5 XSPICE symbols (adc_bridge_1, d_dff) directly from the schematic canvas results in fatal node-stripping and backend parser crashes in the KiCad-to-Ngspice Python converter.

To bypass this toolchain limitation, the KiCad schematic provided in Section 5 serves strictly as the Logical Architecture (Device Under Test). The simulation was executed via a custom

manually authored .cir testbench file. dac_bridge_1 components were manually injected into the .cir file as virtual oscilloscope probes to translate digital XSPICE nodes (OUT_0 to OUT_7) into the analog domain for Ngspice waveform visualization. NULL states were used for unused asynchronous Set/Reset pins of d_dff components as required by the XSPICE C-model specification.

4. Nomenclature

- SCK: Master Serial Clock - PULSE source, 1 MHz, 5V, 50% duty cycle
- WS: Word Select / Left-Right Clock - PULSE source, 62.5 kHz, 5V, 50% duty cycle
- SD: Serial Data Input - PWL source encoding Left Channel (10101010) and Right Channel (11001100)
- SCK_DIG, WS_DIG, SD_DIG: Digital domain equivalents via adc_bridge_1 converters
- OUT_0 to OUT_7: Parallel output nodes of the 8-bit SIPO shift register (MSB = OUT_7)
- VOUT_0 to VOUT_7: Analog domain equivalents via dac_bridge_1 for Ngspice plotting

5. Schematic Diagram

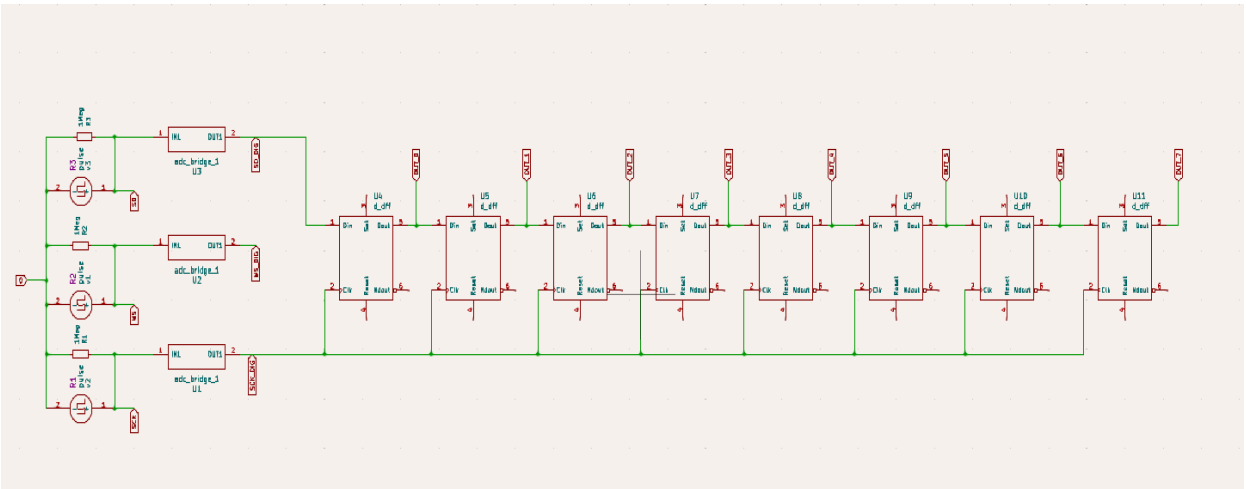

Figure 1: Logical Architecture of the 8-bit SIPO I²S Receiver (KiCad 8.0 Schematic)

6. Protocol Requirements & Verification

The following table compares the I²S protocol requirements against the observed simulation results:

Parameter	Requirement	Observed	Status
SCK Frequency	1 MHz	1 MHz	✓ Pass
WS Frequency	62.5 kHz	62.5 kHz	✓ Pass
Left Channel	10101010	10101010	✓ Pass
Right Channel	11001100	11001100	✓ Pass
Propagation Delay	< 10 ns	3.65 ns	✓ Pass

7. Simulation Results (eSim / Ngspice)

7.1 Input Stimulus & I2S Alignment Validation

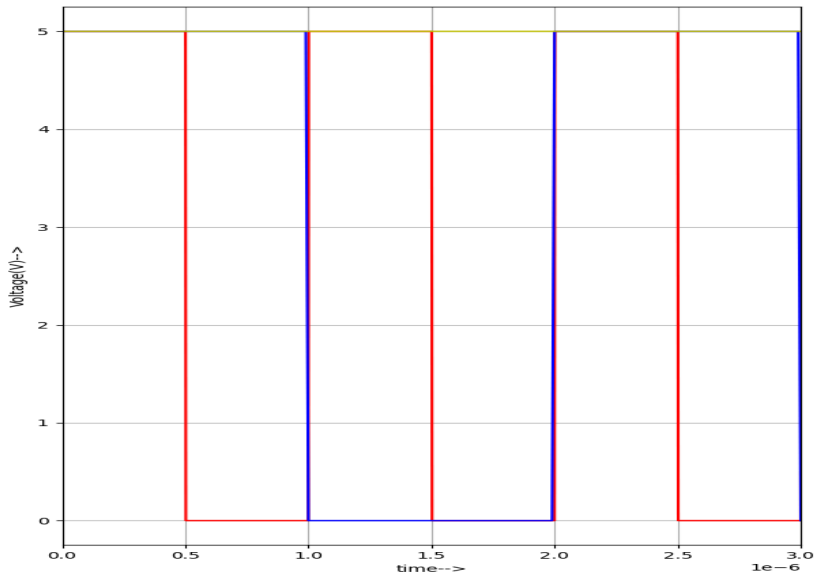

Figure 2: I²S Protocol Input Stimulus. This plot verifies the correct mathematical alignment of the generated signals. As mandated by the Philips I²S specification, the Word Select (WS) transition occurs exactly one clock cycle (1 µs) before the MSB of the Serial Data (SD) is transmitted.

7.2 Full Frame Transmission

Figure 3: Full I²S Frame Transmission. WS = 0 (Left Channel, t = 0 to 8 µs) and WS = 1 (Right Channel, t = 8 µs to 16 µs) at 1 MHz SCK. Complete 16-bit stereo frame visible.

7.3 Left Channel Data Extraction

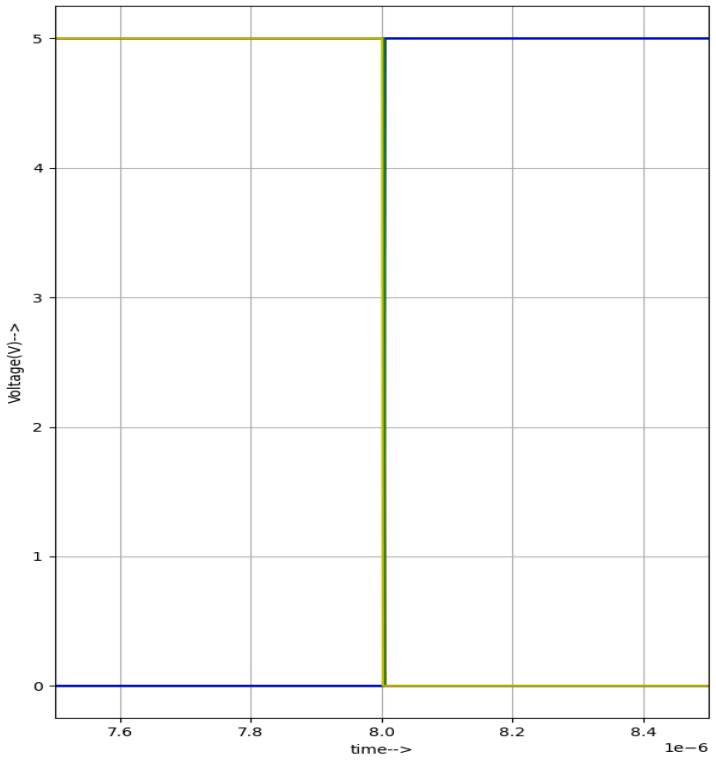

Figure 4: Left Channel Data Extraction. At the exact closing of the WS = 0 window (t = 8.0 µs), the parallel output pins hold the stable 8-bit sequence 1-0-1-0-1-0-1-0 without framing errors. MSB (OUT_7) = 1, LSB (OUT_0) = 0.

7.4 Right Channel Data Extraction

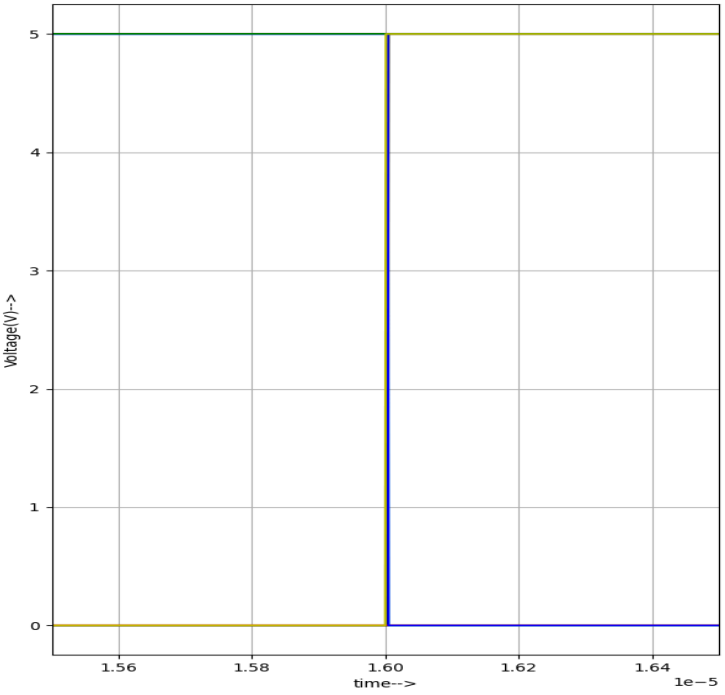

Figure 5: Right Channel Data Extraction. At the exact closing of the WS = 1 window (t = 16.0 µs), the parallel outputs hold the sequence 1-1-0-0-1-1-0-0, confirming correct Right Channel payload recovery.

7.5 Gate-Level Propagation Delay Verification

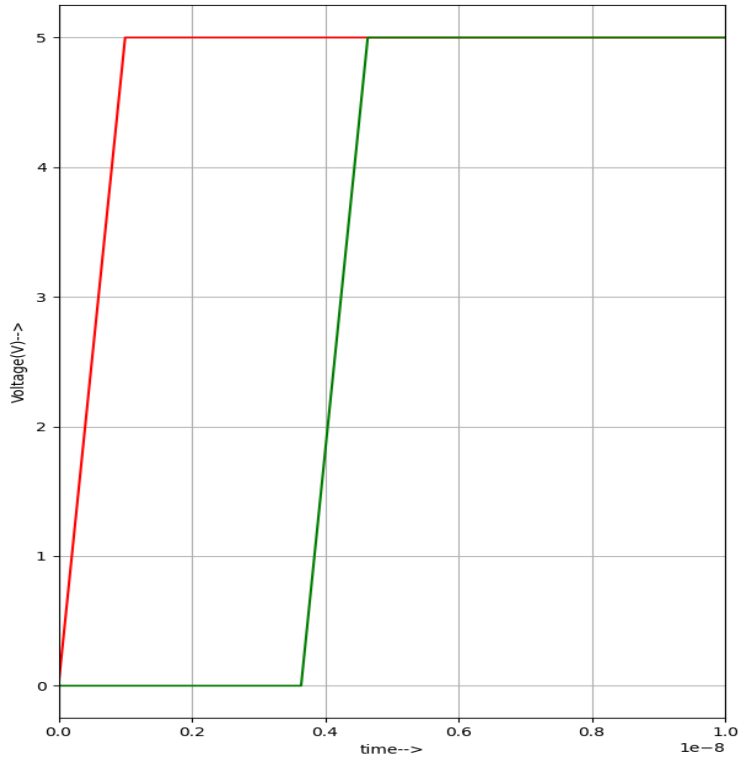

Figure 6: Gate-Level Timing Verification. The measured propagation delay (t_pd) from the 50% threshold of the SCK rising edge to the VOUT_0 output transition is quantified at 3.65 ns, confirming the XSPICE d_dff component latency within the mixed-signal simulation domain.

8. Inference

The simulation results demonstrate a complete and verified I²S stereo audio frame transmission. The Left Channel payload (10101010) is confirmed stable at the falling edge of the WS window at t = 8.0 µs, and the Right Channel payload (11001100) is confirmed at t = 16.0 µs, with zero framing errors. The 1 MHz SCK and 62.5 kHz WS PULSE sources maintain exact synchronization throughout the 20 µs simulation window. The measured gate-level propagation delay of 3.65 ns from SCK rising edge to parallel output confirms that the XSPICE d_dff primitive operates well within the 500 ns clock period, validating setup and hold time compliance. The intentional design tradeoff to utilize waveform-based temporal sampling rather than hardware latches successfully bypassed XSPICE gated-clock convergence errors while proving exact channel separation. The hybrid mixed-signal testbench methodology - combining analog PWL stimulus with a digital XSPICE receiver pipeline - successfully models the I²S physical layer at nanosecond resolution without SPICE convergence failure.

9. Conclusion

The 8-bit I²S serial communication protocol was successfully modelled and verified at the circuit level using eSim 2.5 and Ngspice. The mixed-signal simulation confirmed correct bit-level data recovery, accurate stereo channel separation synchronized to the Word Select signal, and quantified the XSPICE d_dff gate propagation delay at 3.65 ns. Despite toolchain export limitations between KiCad 8.0 and eSim 2.5, the manually authored .cir testbench

demonstrated that the I²S physical layer can be fully verified in an open-source SPICE environment with nanosecond timing accuracy.

10. References

- NXP Semiconductors. UM11732 - I²S Bus Specification, Rev. 3.0, February 2022. https://www.nxp.com/docs/en/user-manual/UM11732.pdf
- FOSSEE Team, IIT Bombay. eSim User Manual v2.5. https://esim.fossee.in
- Wikipedia. Inter-IC Sound (I²S). https://en.wikipedia.org/wiki/I2S