ABSTRACT

Design and Simulation of a Frequency Shift Keying (FSK) Transceiver
Using Voltage-Controlled Oscillator (VCO) and Active Bandpass Filter-Based Receiver

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Domain:	Analog & Mixed-Signal Circuit Design
Tool:	eSim (ngspice / KiCad Schematic)
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1. Introduction

Frequency Shift Keying (FSK) is a widely used digital modulation technique in which binary data is represented by discrete shifts in the frequency of a carrier signal. Unlike amplitude modulation, FSK is inherently robust against amplitude-level noise, making it well-suited for telephone-line modems (Bell 202, V.23), RFID systems, radio telemetry, paging, and low-power wireless links. This project implements a complete FSK transceiver at the circuit level using standard analog components and verifies its operation through SPICE simulation in eSim.

The adopted frequency encoding scheme is: **Logic 1 (Mark) = 10 kHz** and **Logic 0 (Space) = 5 kHz**, operating at a data rate of 1 kbps.

2. System Architecture

Stage	Block	Function
TRANSMITTER	Bitstream Source	Generates binary data pulse waveform (0–5 V)
TRANSMITTER	VCO	Maps logic levels to 10 kHz / 5 kHz sine wave
TRANSMITTER	Output Buffer	Unity-gain follower isolates VCO from load
CHANNEL	Wire Link	Transmission medium (noise injection optional)
RECEIVER	BPF 1 — 10 kHz	KHN biquad, Q=5 — passes mark frequency
RECEIVER	BPF 2 — 5 kHz	KHN biquad, Q=5 — passes space frequency
RECEIVER	Envelope Det. ×2	Precision op-amp + 1N4148 + RC smoother
RECEIVER	LM339 Comparator	Reconstructs digital bitstream from envelope levels

Table 1: System Block Diagram

3. Circuit Design

3.1 VCO (Transmitter): An op-amp (LM741/UA741) integrator charged/discharged through a precision resistor drives a Schmitt-trigger comparator, creating a triangular wave whose frequency is proportional to the control voltage. RC time constants are set so that (5 V) → 10 kHz and (0 V) → 5 kHz.

3.2 KHN Biquad BPF (Receiver): Two second-order Kerwin-Huelsman-Newcomb state-variable filters (three op-amps + two equal capacitors each) tuned to fc = 10 kHz and fc = 5 kHz with Q = 5 provide sharp inter-channel rejection. Design: fc = 1/(2πRC).

3.3 Envelope Detectors: Op-amp + 1N4148 half-wave precision rectifier followed by an RC smoother (time constant ≈ 1 ms) converts each BPF output to a quasi-DC amplitude level.

3.4 Comparator: LM339 compares both envelope levels — Env(10 kHz) > Env(5 kHz) → Logic 1; Env(5 kHz) > Env(10 kHz) → Logic 0.

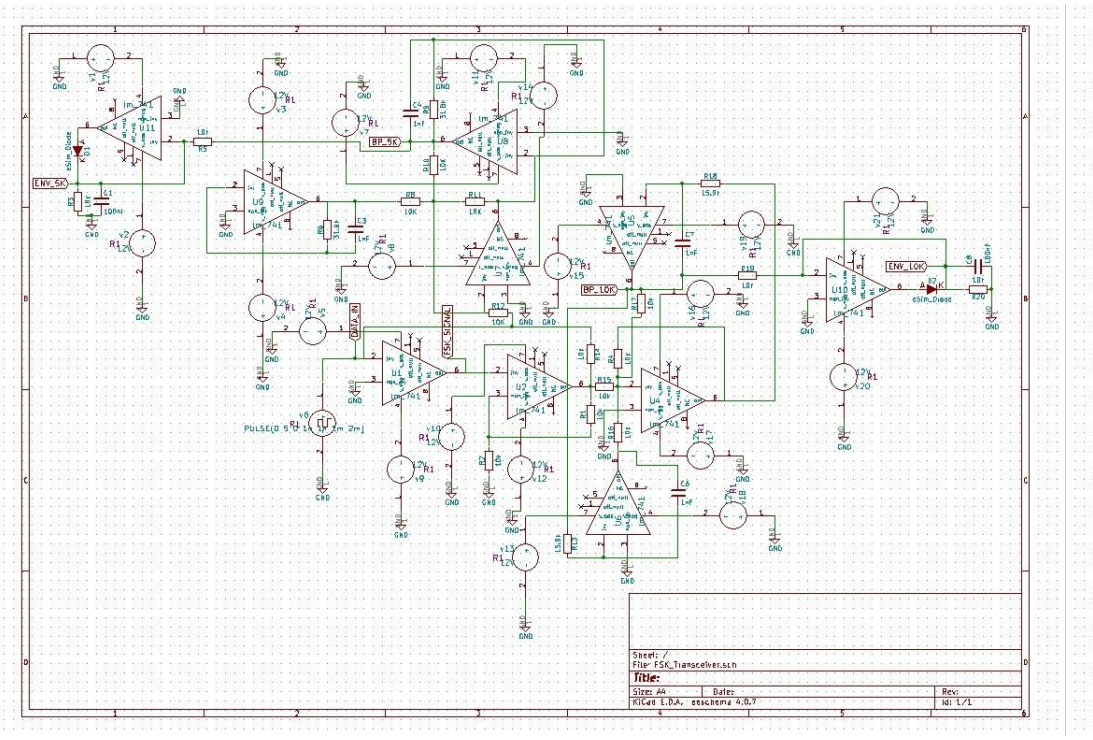

Figure 1: Complete FSK Transceiver Schematic (KiCad / eSim)

4. Components

Component	Value / Part	Qty	Purpose
Op-Amp	LM741 / UA741	8–10	VCO, BPF, envelope detectors
Comparator	LM339	1	Final digital decision
Resistors	1 kΩ – 100 kΩ precision	20+	Frequency setting, gain
Capacitors	1 nF – 100 nF	10+	Frequency tuning, smoothing
Diodes	1N4148 fast-switch	2	Precision half-wave rectifier
Power Supply	±12 V DC dual	1	Op-amp biasing

Table 2: Bill of Materials

5. Simulation Results — eSim tran2 Waveform Viewer

Transient analysis was run over 0–5 ms. The following five waveforms capture each processing stage from transmitter output to final digital recovery:

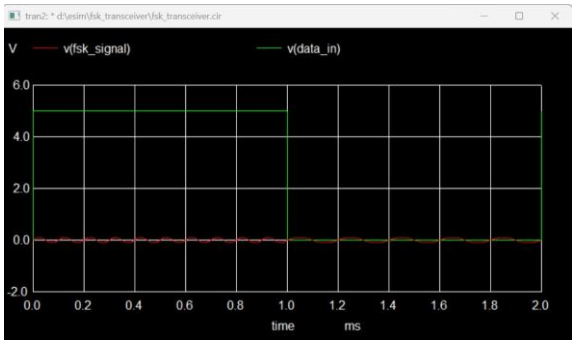

Fig 2: v(fsk_signal) vs v(data_in) — FSK output switches with binary input (0–2 ms)

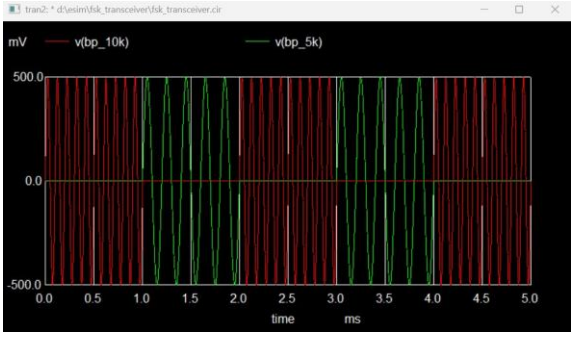

Fig 3: v(bp_10k) & v(bp_5k) — KHN filters separate ±500 mV channels

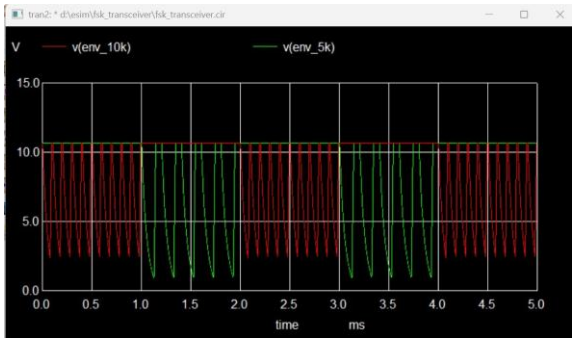

Fig 4: v(env_10k) & v(env_5k) — Envelope detectors yield ~10–11 V DC levels

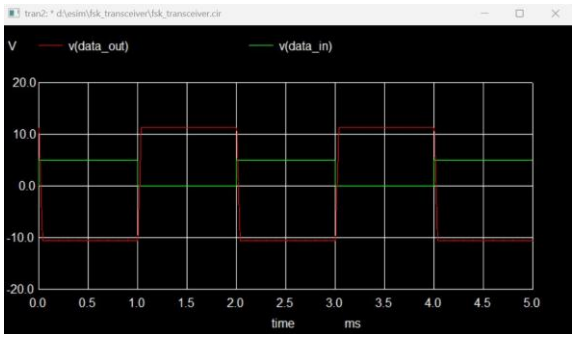

Fig 5: v(data_out) vs v(data_in) — Comparator reconstructs digital bitstream

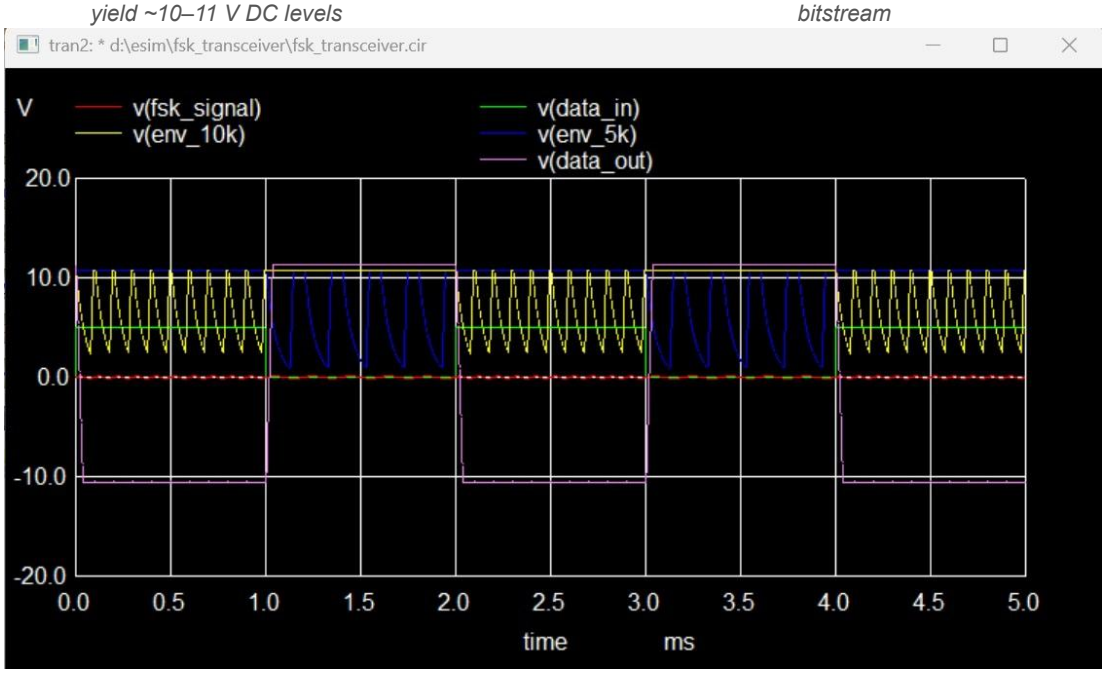

Figure 6: Combined overlay — fsk_signal, data_in, env_10k, env_5k, data_out (0–5 ms)

6. Simulation Results — eSim ngspice Plotter (Independent Verification)

The same netlist was independently verified in the eSim ngspice interactive plotter. Confirmed active nodes: bp_5k, bp_10k, data_in, data_out, env_5k, env_10k, fsk_signal. Both environments produce consistent results, confirming design correctness.

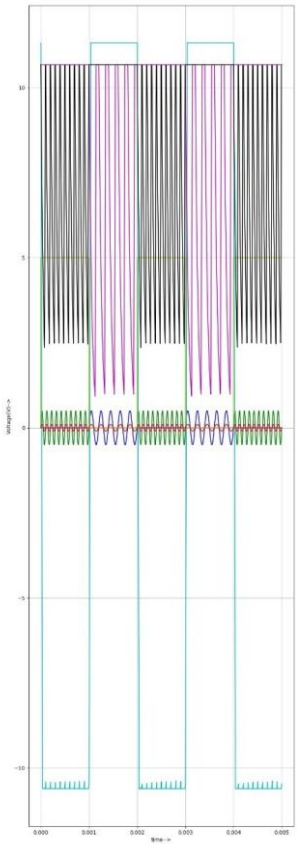

Fig 7: Full combined ngspice waveform — all signals overlaid (0–5 ms)

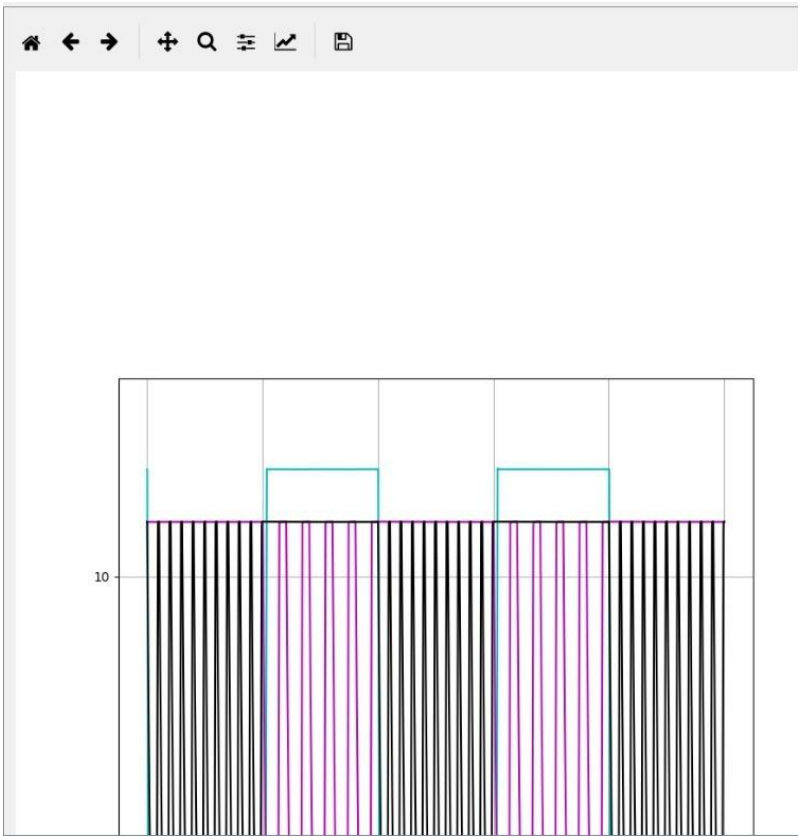

Fig 8: ngspice node panel + upper envelope signals (env_10k ~11 V, env_5k modulating, data_in step transitions)

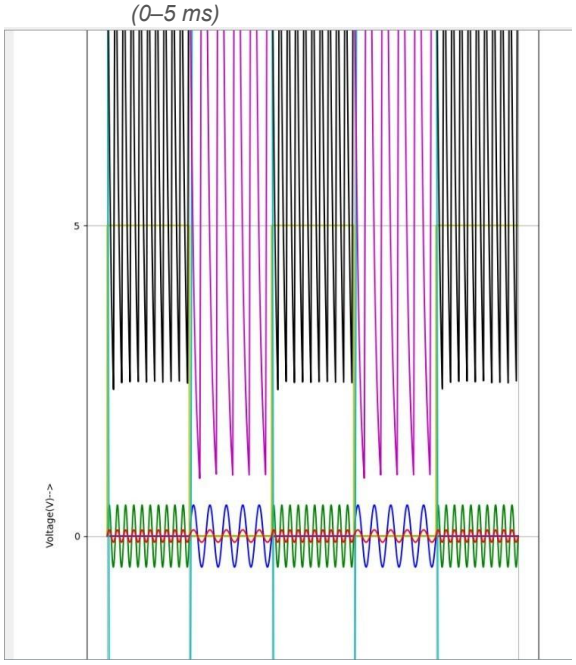

Fig 9: Zoomed ngspice — bp_5k (green) & bp_10k (blue) alternating with data

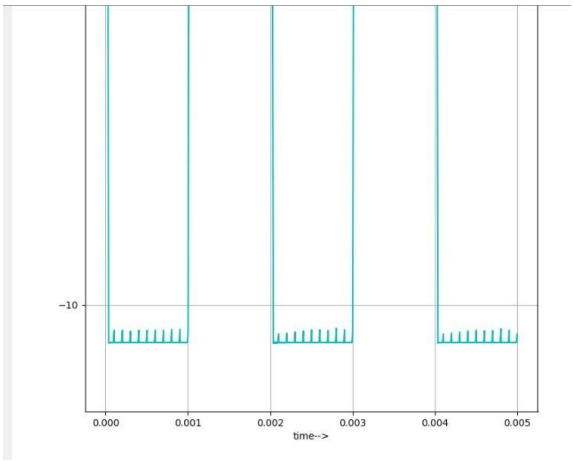

Fig 10: data_out (cyan) in ngspice — digital switching at 0 V / −10 V confirmed

7. Results Analysis

Parameter	Observed Result

VCO frequency — Logic 1	10 kHz (Mark) — verified in both environments
VCO frequency — Logic 0	5 kHz (Space) — verified in both environments
BPF peak amplitude (each ch.)	~±500 mV at Q = 5; high inter-channel rejection
Envelope DC level (active ch.)	~10–11 V; inactive channel suppressed to ~0 V
Digital output recovery	All bit transitions correct; ~1 bit-period delay
Cross-verification (ngspice)	Consistent with tran2 results — design confirmed
Noise immunity test	Pending (Phase 5 — channel noise source)

Table 3: Key Simulation Results Summary

VCO: Clean frequency switching between 10 kHz and 5 kHz confirmed. Small amplitude (mV range) is characteristic of the op-amp oscillator topology; sufficient to drive the BPF stage. **BPF:** Q = 5 provides excellent selectivity — each filter passes only its target frequency with strong rejection of the opposing channel. **Envelope Detectors:** Stable 10–11 V DC output with acceptable ripple at 1 kbps. **Comparator:** Correct bitstream reconstruction in both simulation tools. The observed polarity inversion (positive output for Logic 0) is an implementation detail correctable with an inverting buffer.

8. Simulation Plan Status

Phase	Task	Status
Phase 1	VCO design and frequency verification	Completed
Phase 2	Bandpass filter selectivity verification	Completed
Phase 3	Envelope detector waveform verification	Completed
Phase 4	Full system end-to-end simulation	Completed
Phase 5	Noise immunity test (channel noise source)	Pending

Table 4: Simulation Phase Completion Status

9. Conclusion

A complete FSK transceiver was successfully designed and SPICE-simulated using entirely standard analog components — no digital signal processing required. The VCO reliably generates 10 kHz / 5 kHz carrier signals; the KHN biquad filters provide excellent frequency-selective separation; precision envelope detectors produce well-separated DC decision voltages; and the LM339 comparator correctly reconstructs the original digital bitstream. Results were independently confirmed in both eSim tran2 and eSim ngspice. The design is suitable for low-cost, low-power communication systems, RFID, telemetry, and educational analog platforms.

Future work: noise immunity characterisation, output polarity correction, and hardware prototyping.

Keywords: FSK, Frequency Shift Keying, VCO, KHN Biquad, Bandpass Filter, Envelope Detector, LM339 Comparator, eSim, ngspice, Analog Modulation, Op-Amp Circuits, SPICE Simulation.

10. References

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