NOISE TOLERANT UART RECEIVER

This project presents the design and simulation of a robust UART (Universal Asynchronous Receiver-Transmitter) receiver developed in eSim. The design focuses on hardware-level reliability, utilizing a gated clock mechanism to minimize power consumption and a parity-check tree for data integrity. The system operates at a baud rate of 9600 bps, translating to a bit period of approximately 104.16µs.

Working Principle

The receiver remains in an idle state until a Start Bit (Logic 0) is detected at the Recovered_Tx line.

Signal Conditioning: The incoming signal passes through an LM741-based filter and comparator stage to mitigate noise.

Clock Synchronization: A Set-Reset (SR) Latch is triggered by the start bit, enabling a Tristate Buffer that releases the local clock.

Data Capture: A series of eight D-Flip Flops forms a Shift Register that populates the serial data into a parallel format (D_1 to D_8).

Stability Phase: To ensure signal integrity as per standard UART protocols, the system implements an "8+8" pulse logic. After the initial 8 bits are shifted, a delayed pulse counter maintains the clock for an additional 8 cycles to allow the Parity XOR Tree to stabilize and the data to be "obtained" before the clock is automatically disabled.

Schematic Components

The circuit is composed of mixed-signal blocks:

Analog Block: Pulse voltage sources for data simulation, LM741 operational amplifier for signal recovery, and RC filtering.

Digital Block: XSPICE-based d_dff (Flip Flops), d_srlatch, d_tristate, and logic gates (d_and, d_xor) for the parity tree and counter logic.

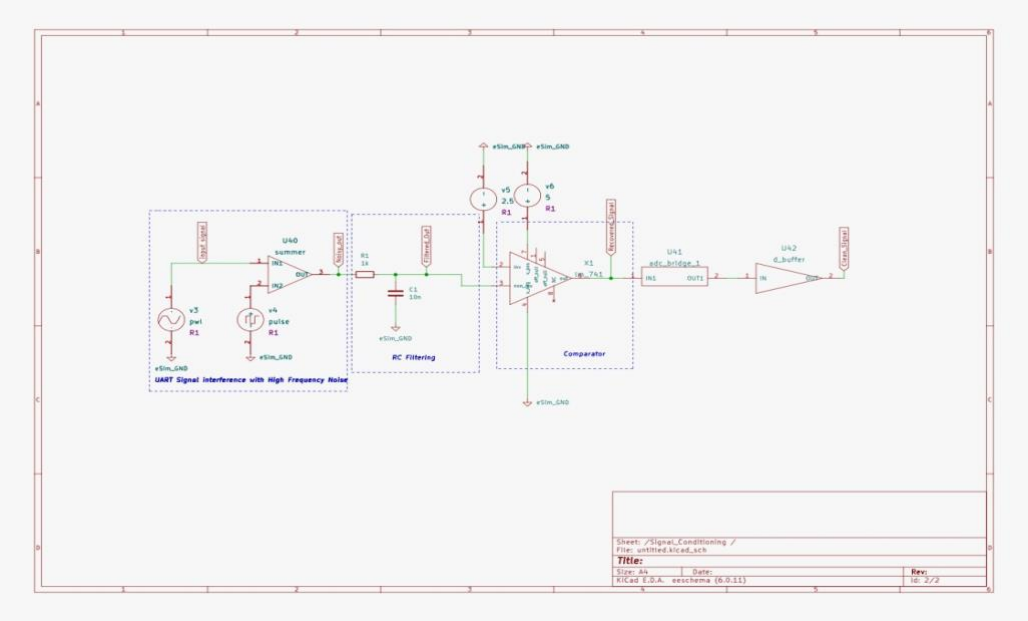
Bridging: adc_bridge and dac_bridge components are utilized to facilitate seamless communication between the analog signal path and the digital processing logic.

The simulation results verify the following:

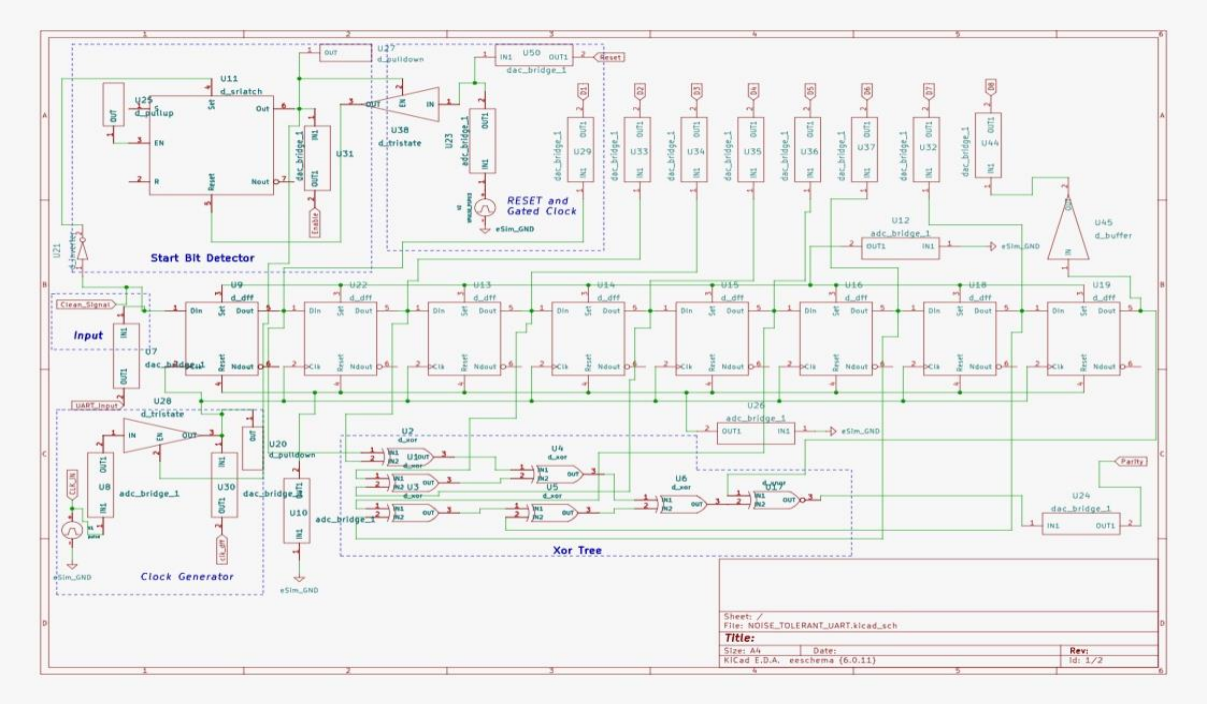
- **Gated Clock:** The clock pulses only during the active transmission window and shuts down precisely after the 16th pulse.

- **Data Fidelity:** The parallel outputs (D_1 through D_8) correctly reflect the serial input bits provided by the PWL source.
- **Error Detection:** The **Parity Output** successfully flags the odd/even bit count, providing a reliable error-detection mechanism for the received byte.

Signal Conditioning Schematic:

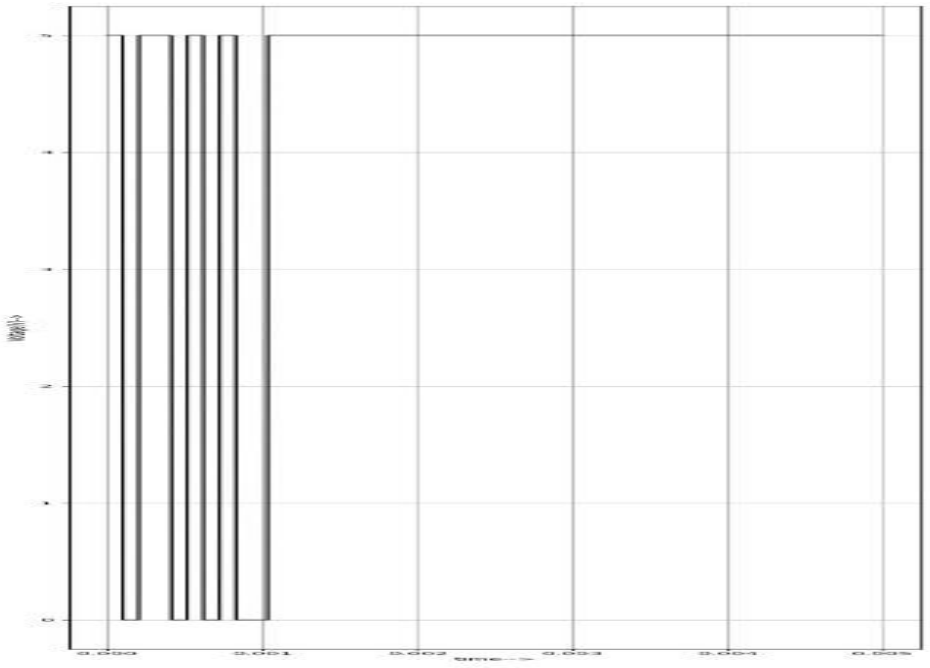


UART RECEIVER Schematic :

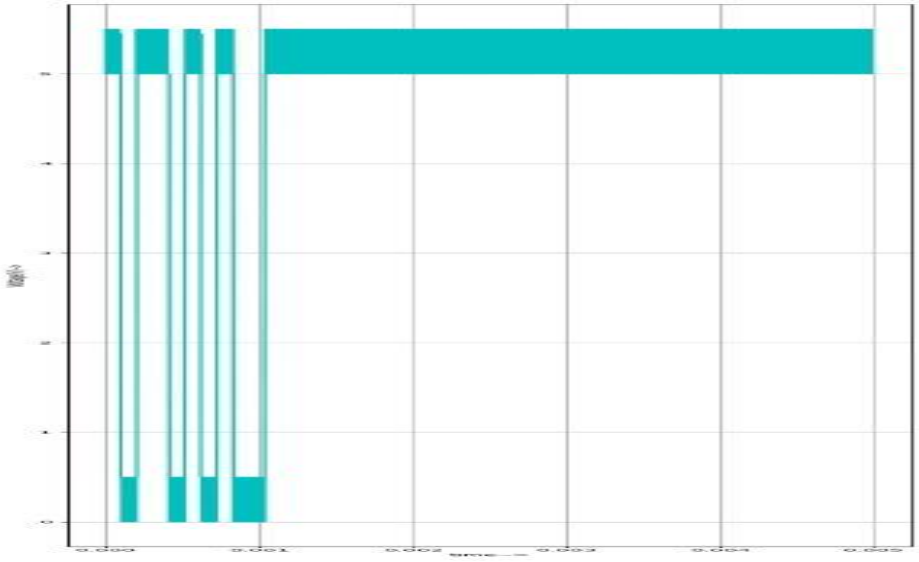


Output Waveforms :

The input Signal (1101010 + 0 Parity) Signal

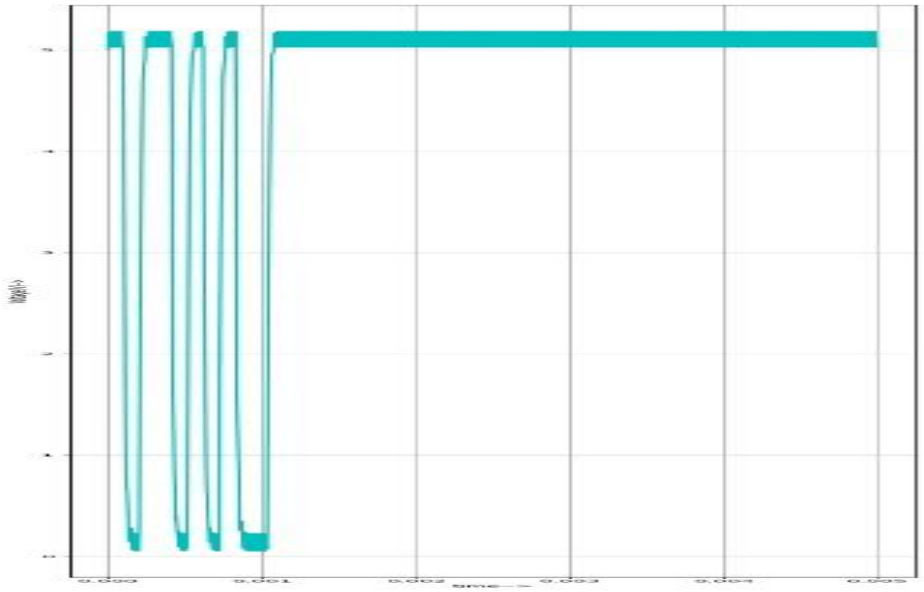


The input Signal that is corrupted by high frequency Signal :

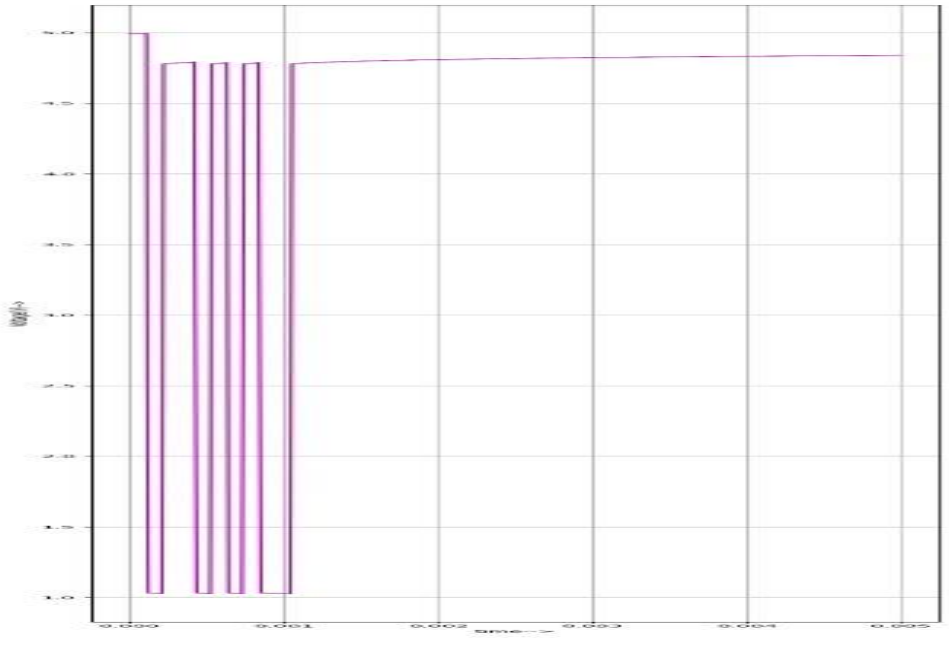


Recovering Signal by using RC Filter, Comparator and Buffer Circuits :

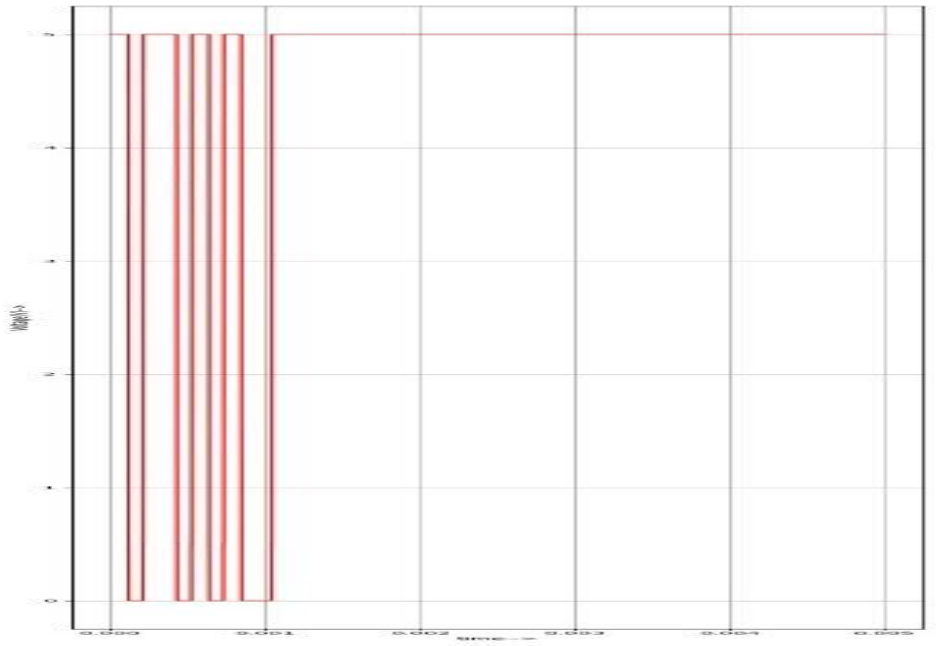
RC Filter Output :



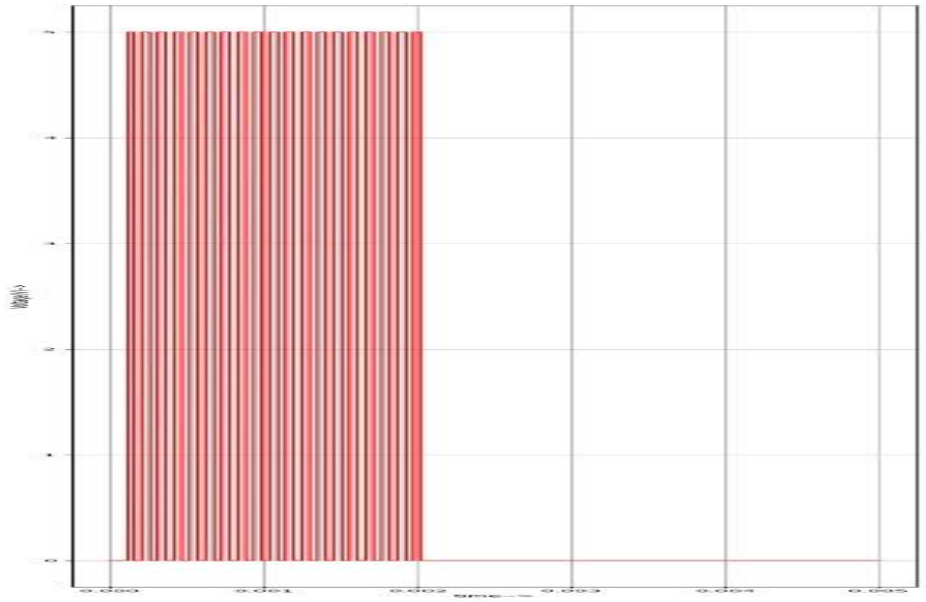
Comparator Circuits Output :



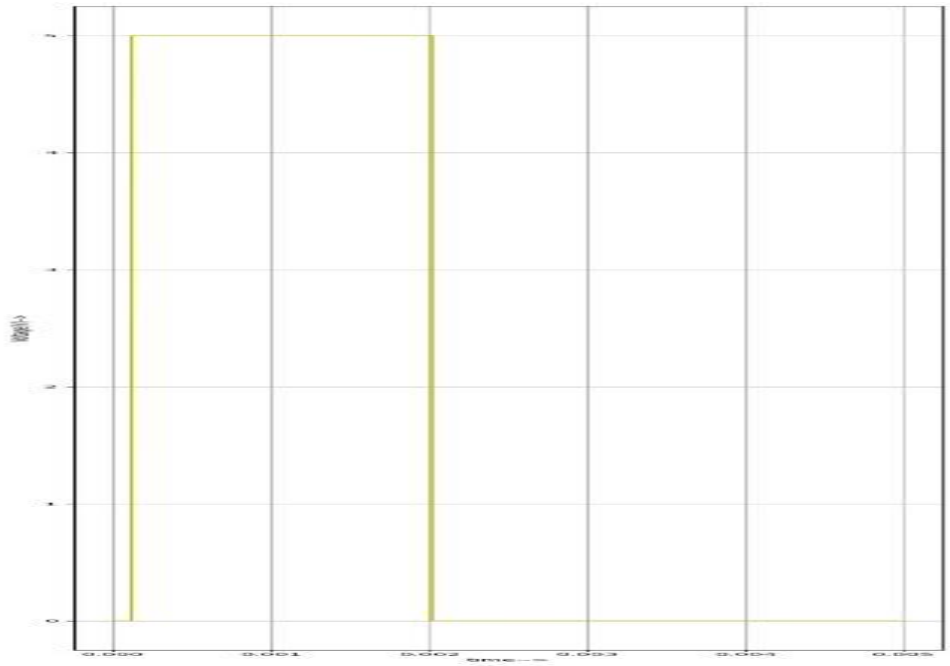
Recovered Original Signal after Buffer Circuit :



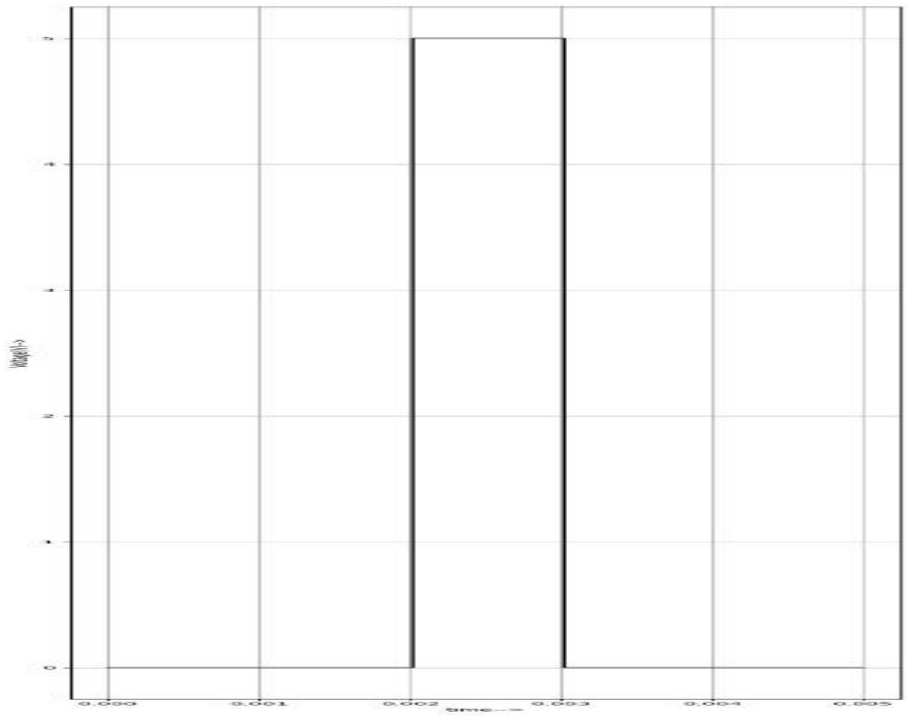
Gated Clock (Clock is Enabled only For Transmission, After Transmission Receiver enters into RESET Mode) :



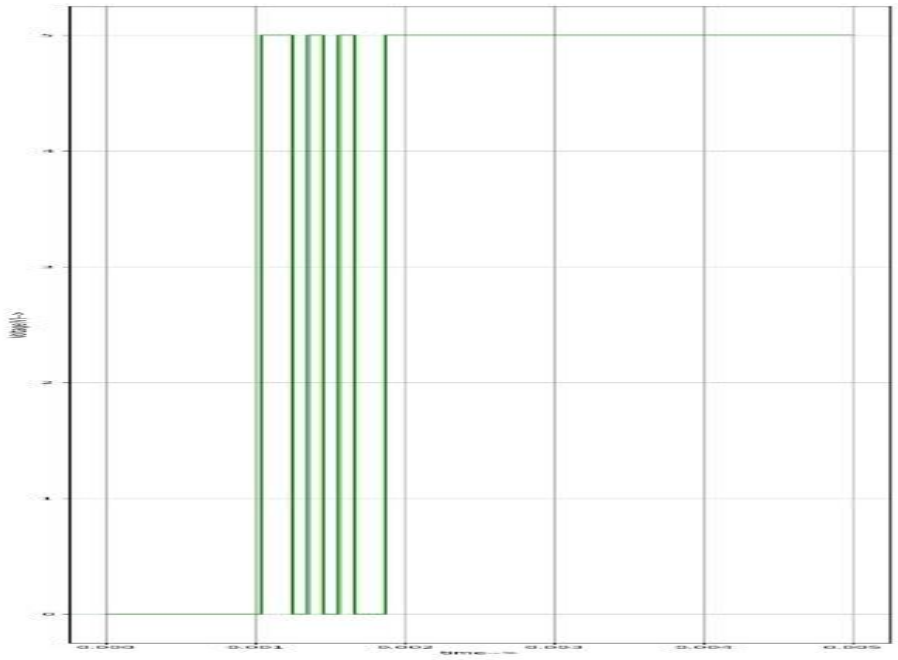
Enable Signal :



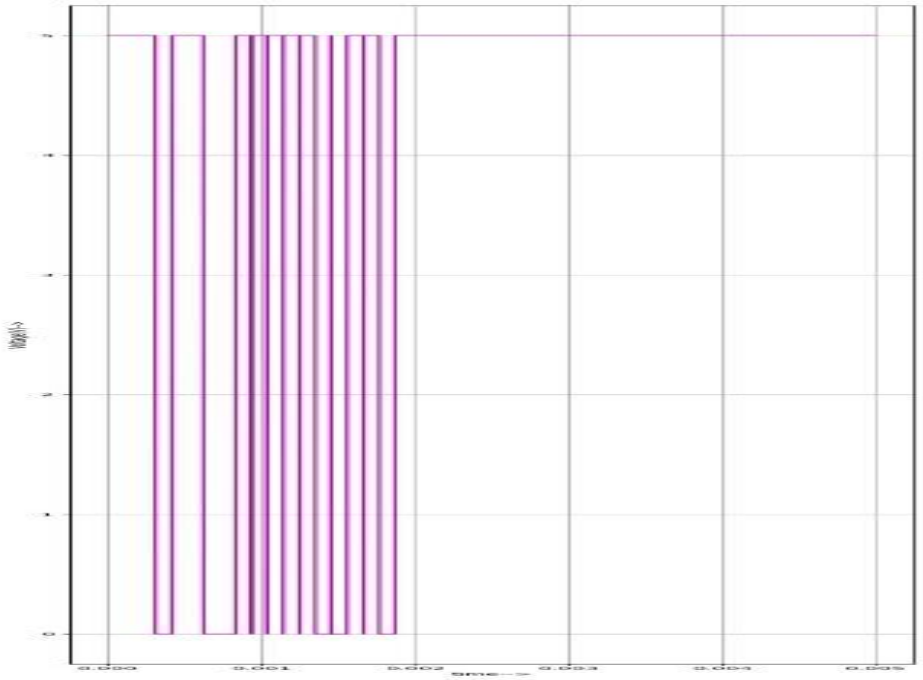
RESET Signal :



Recieved Output at the D8 Flipflop :



Parity Signal by XOR Tree :



References :

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  https://spoken-tutorial.org/tutorial-search/?search_foss=eSim&search_language=English
- **eSim and Ngspice Manual.**
  https://static.fossee.in/esim/manuals/eSim_Manual_2.4.pdf
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  https://en.wikipedia.org/wiki/Universal_asynchronous_receiver-transmitter