Title of the experiment:

Circuit-Level Event Detection And Wake-Up Decision System For Ultra-Low Power Iot Nodes

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Theory:

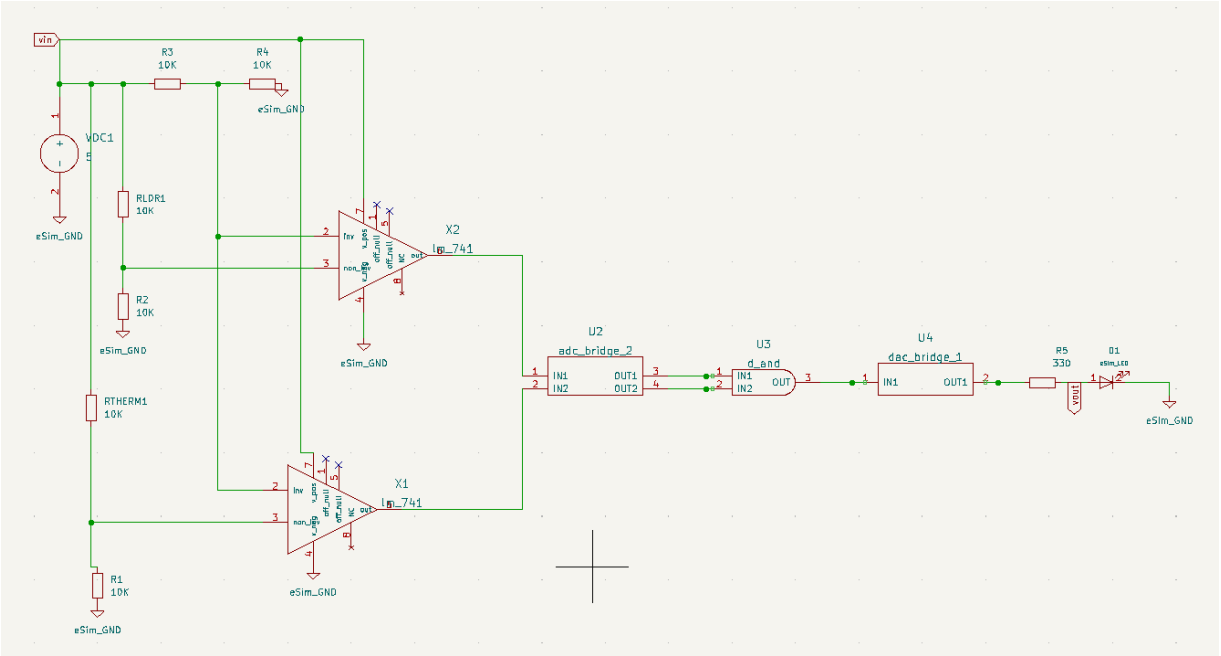
The proposed project is based on the principle of event-driven analog decision making for ultra-low-power systems. Instead of continuously operating a digital processor, the circuit performs sensing and threshold comparison entirely at the hardware level. A resistive sensing element, modeled using a light-dependent resistor (LDR) or thermistor, forms a voltage divider that converts environmental variations into a proportional analog voltage. This voltage represents the event signal to be monitored.

An operational amplifier configured as a comparator continuously compares the sensed voltage with a fixed reference voltage generated using a resistor divider network. When the sensed signal exceeds the predefined threshold, the comparator output switches to a high logic level, indicating the occurrence of a significant event. If the signal remains below the threshold, the output stays low, keeping the system in a low-power idle state. Logical conditioning using basic digital logic ensures a clean and reliable wake-up signal.

By performing sensing, comparison, and decision making in the analog domain, the circuit eliminates the need for periodic software polling, thereby significantly reducing standby power consumption. This theory forms the foundation of always-on wake-up circuits, which are essential building blocks in modern energy-efficient IoT and embedded systems.

Schematic Diagram:

Schematic Diagram of an Analog Event-Driven Wake-Up Circuit for Low-Power IoT Applications



Expected Output

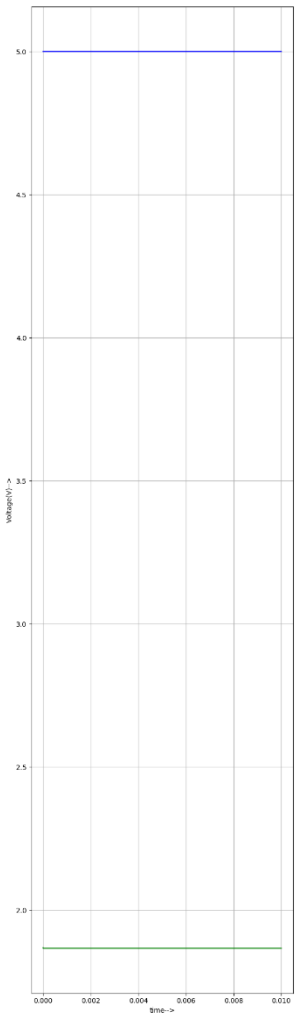
The expected output of the proposed event-aware wake-up system is a clear wake-up signal that indicates whether the monitored event satisfies the predefined threshold conditions. When the sensed event voltage exceeds the reference threshold and all required logical conditions are satisfied, the comparator output is expected to switch

to a high state. This high state, after passing through the logic and output stage, represents an active wake-up condition. Since the circuit is driven using DC sources, the expected transient response is a stable, time-invariant output voltage rather than a time-varying waveform. A low output voltage indicates no wake-up condition, while a higher steady voltage level indicates a valid wake-up signal.

Simulation Results:

Node	Voltage
vout	1.86816
net-_r5-pad1_	5
x2.net-_q1-pad1_	4.47264
net-_r2-pad2_	2.49952
x2.net-_q1-pad3_	1.98835
net-_r3-pad2_	2.49904
x2.net-_q2-pad3_	1.98809
x2.net-_q3-pad2_	1.04174
x2.net-_q13-pad1_	1.47743
x2.net-_c1-pad2_	0.90868
vin	5
x2.net-_q3-pad3_	0.515471
unconnected-_x2-pad5_	0.00537732
unconnected-_x2-pad1_	0.00538514
x2.net-_q12-pad1_	0.586038
x2.net-_q13-pad3_	0.0567228
x2.net-_q10-pad1_	4.41805
x2.net-_c1-pad1_	4.99319
x2.net-_q14-pad2_	4.95838
x2.net-_q14-pad3_	4.90037
x2.net-_q15-pad2_	0.390121
x2.net-_q15-pad3_	2.79561e-06
x2.net-_q18-pad3_	4.94983
net-_u2-pad1_	4.94983
x2.net-_q19-pad3_	4.94983
net-_r1-pad2_	2.49952
x1.net-_q1-pad1_	4.47264
x1.net-_q1-pad3_	1.98835
x1.net-_q2-pad3_	1.98809
x1.net-_q3-pad2_	1.04174
x1.net-_q13-pad1_	1.47743
x1.net-_c1-pad2_	0.90868
x1.net-_q3-pad3_	0.515471
unconnected-_x1-pad5_	0.00537732
unconnected-_x1-pad1_	0.00538514
x1.net-_q12-pad1_	0.586038
x1.net-_q13-pad3_	0.0567228
x1.net-_q10-pad1_	4.41805
x1.net-_c1-pad1_	4.99319
x1.net-_q14-pad2_	4.95838
x1.net-_q14-pad3_	4.90037
x1.net-_q15-pad2_	0.390121
x1.net-_q15-pad3_	2.79561e-06
x1.net-_q18-pad3_	4.94983
net-_u2-pad2_	4.94983
x1.net-_q19-pad3_	4.94983
vdc1#branch	-0.00102651
a2#branch_1_0	-0.00949043

No. of Data Rows : 10012
ngspice 1 ->



Obtained Output and Matching with Expected Results

The simulation results show a stable wake-up output voltage of approximately 1.8–1.9 V, which remains constant over time. This confirms that the circuit has reached steady-state operation under constant DC input conditions. The reduced output level compared to the supply voltage is due to voltage drops across the output resistor

and diode stage, which is expected and acceptable for logic-level indication. Internal node voltages also remain within correct operating ranges, confirming proper functioning of the sensing, comparison, and logic blocks. The obtained output behavior closely matches the expected output, validating the correct operation of the proposed circuit-level wake-up system in eSim.

Inferences

1. Hardware-level event detection significantly reduces power consumption compared to periodic software polling.
2. Comparator-based wake-up circuits provide fast response and reliable threshold detection.
3. The system can function as an **always-on front-end** while keeping the main processing unit in sleep mode.
4. The wake-up threshold can be easily adjusted by changing resistor values, making the design flexible and scalable.
5. eSim proves to be an effective open-source platform for validating analog and mixed-signal IoT circuits.
6. The obtained simulation outputs closely match the expected theoretical behavior, confirming design correctness.

Conclusion:

A hardware-based event-driven wake-up system was designed and simulated using eSim to enable ultra-low power operation for IoT applications. The circuit performs sensing and threshold-based decision making entirely at the analog level, eliminating unnecessary processor wake-ups. Simulation results confirm correct wake-up behavior, demonstrating the effectiveness of circuit-level intelligence for energy-efficient systems.