Design of SRAM Based BTI Sensor for Improved Cell Stability

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ABSTRACT

With continuous scaling of CMOS technology, reliability challenges such as Bias Temperature Instability (BTI) have become a major concern in modern integrated circuits. BTI causes time-dependent degradation of transistor parameters, leading to increased delay and reduced stability, particularly in Static Random Access Memory (SRAM) cells. Since SRAM occupies a large portion of System-on-Chip (SoC) area, its reliability directly affects overall system performance.

This project focuses on the **design and simulation of an SRAM cell**, which forms the core element of an SRAM-based BTI sensor aimed at improving cell stability. The complete BTI sensor architecture includes additional blocks such as transition detector and pulse detector; however, **in this work only the SRAM cell is implemented and analyzed using eSim**. The remaining sensor blocks are studied theoretically and proposed as future extensions. Simulation results validate correct SRAM read and write functionality, providing a strong foundation for BTI-aware memory design.

Keywords: SRAM, Bias Temperature Instability (BTI), CMOS memory, Cell stability, Aging effects

I. INTRODUCTION

The rapid advancement of CMOS technology has enabled high-performance and low-power System-on-Chip (SoC) designs. However, aggressive scaling has introduced significant reliability issues, among which Bias Temperature Instability (BTI) is one of the most critical. BTI results in gradual degradation of transistor threshold voltage over time, leading to increased delay and performance loss.

BTI is classified into Negative Bias Temperature Instability (NBTI), which mainly affects PMOS transistors, and Positive Bias Temperature Instability (PBTI), which affects NMOS transistors. These effects severely impact SRAM cells due to their continuous biasing nature. As SRAM constitutes a major portion of modern SoCs, BTI-induced degradation can lead to reduced stability margins and eventual memory failure.

To address this issue, SRAM-based BTI sensors are proposed in literature to actively monitor aging effects. This project concentrates on the **SRAM cell design**, which is the fundamental block of such sensors.

II. CIRCUIT DIAGRAM

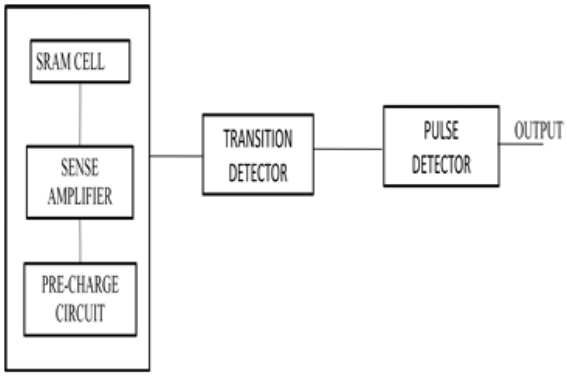


Fig : Complete Sensor block diagram

III. PROPOSED SYSTEM

The complete SRAM-based BTI sensor architecture consists of three blocks:

1. **SRAM Cell (Implemented)**
    - Designed and simulated in eSim
    - Verified read and write operations
2. **Transition Detector (Not Implemented)**
    - Intended to detect slow bit-line transitions caused by aging
    - Studied theoretically from reference literature
3. **Pulse Detector (Not Implemented)**
    - Used to classify aging based on transition pulse width
    - Proposed as future work

In this project, **only the SRAM cell block is implemented**, while the remaining blocks are discussed conceptually.

IV. eSim IMPLEMENTATION

The SRAM cell was designed using CMOS transistors available in eSim. Proper connections of word line, bit lines, power supply, and ground were ensured. Transient simulations were performed to validate read and write operations.

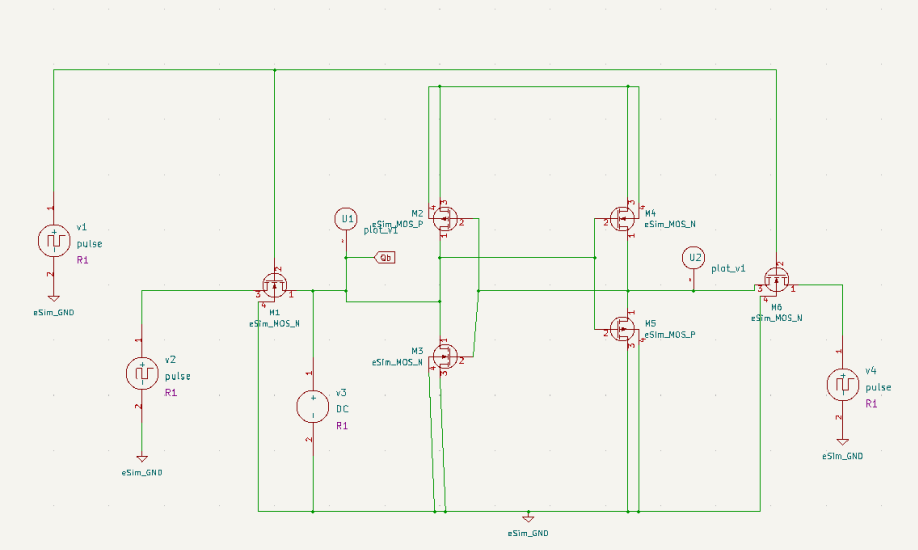


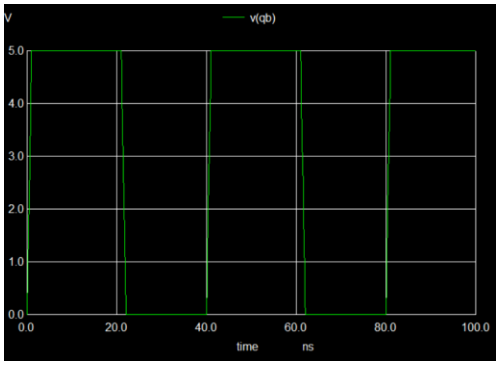
Figure: SRAM Cell Implementation in eSim

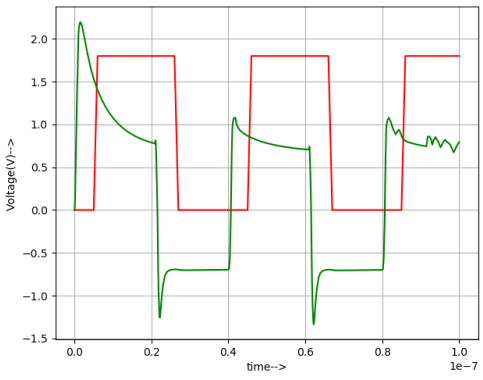
V. SIMULATION RESULTS

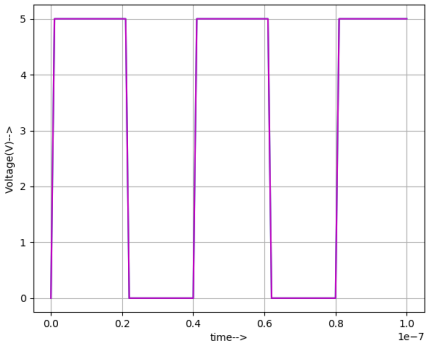
Simulation waveforms confirm:

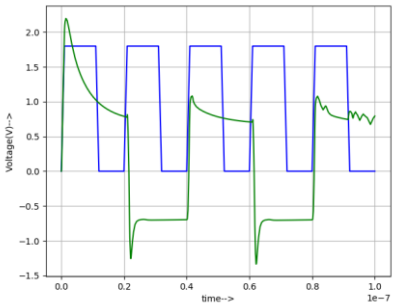
- Correct storage of logic ‘0’ and ‘1’
- Successful read operation without data disturbance
- Stable operation of the SRAM cell

Figure: Input and Output Waveforms









VI. APPLICATIONS

SRAM-based BTI sensors and stable SRAM cells are useful in:

1. Cache memories in processors
2. Low-power embedded systems
3. Reliability-aware SoCs
4. Aging monitoring circuits
5. High-performance digital systems

VII. CONCLUSION

This project presented the **design and simulation of an SRAM cell** intended for use in an SRAM-based BTI sensor. The SRAM cell was successfully implemented and verified using eSim, demonstrating correct read and write operations. Although the complete BTI sensor includes transition and pulse detection circuits, these blocks were not implemented and are proposed as future work.

The implemented SRAM cell provides a reliable foundation for developing aging-aware memory systems and can be extended to a full BTI sensor architecture in future work.

REFERENCE

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