Design and Verification of an 8-Bit SPI Master-Slave System Using eSim

Abstract:

This project demonstrates the design, simulation, and verification of a Serial Peripheral Interface (SPI) Master-Slave communication system using eSim. The circuit integrates digital Register Transfer Level (RTL) blocks described in Verilog with analog pulse sources to create a Mixed-Signal environment.

The primary objective was to verify the control logic timing, specifically the synchronization between the system Clock, Reset, and Start signals. The simulation results confirm that the SPI Master correctly serializes 8-bit parallel data (`10101010`) upon receiving a delayed Start trigger, ensuring data integrity. The project also documents specific challenges encountered with mixed-signal vector bridging in Ngspice and the methodology used to resolve them through rigorous input timing verification.

1. Theory

The Serial Peripheral Interface (SPI) is a synchronous serial communication protocol used for short-distance communication, primarily in embedded systems. It typically operates in a Master-Slave architecture where the Master controls the clock (SCLK) and initiates data transfer.

In this project, the system is divided into two functional blocks:

SPI Master : Handles Parallel-to-Serial conversion. It accepts an 8-bit parallel input and transmits it serially via the MOSI (Master Out Slave In) line.

SPI Slave : Handles Serial-to-Parallel conversion. It samples the incoming MOSI data on the rising edge of SCLK.

1.1 Protocol Timing Requirements

For successful transmission, the following timing constraints must be met:

1. Reset Guard Time: The system must be held in Reset for a specific duration at startup to clear all internal registers.
2. Start Delay: The ‘Start’ signal must not be asserted until the Reset sequence is fully complete. If ‘Start’ and ‘Reset’ overlap, the transmission logic may enter an undefined state.
3. Clock Stability: The SCLK must be stable and continuous during the data transmission window.

2. Circuit Diagram

The mixed-signal schematic was designed in eSim (KiCad). It interfaces analog voltage sources with digital Verilog blocks using ADC (Analog-to-Digital) bridges.

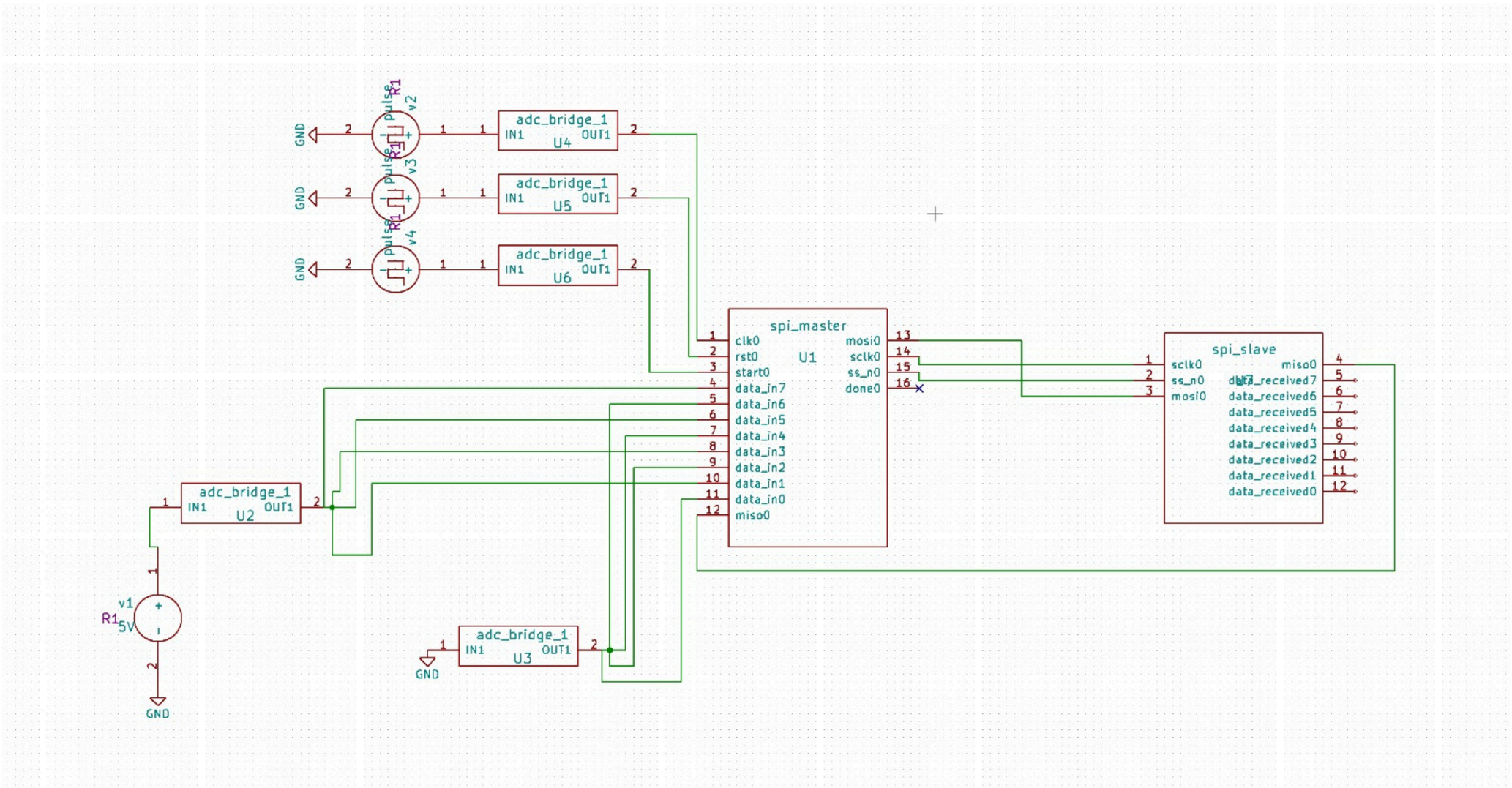

Figure 1 : Mixed-Signal Schematic of SPI Master-Slave System. Note the direct digital connection between Master and Slave.

As shown in Figure 1, the input control signals (Clock, Reset, Start) are generated using Pulse Voltage Sources (‘vpulse’) and converted to digital logic levels. The Master and Slave are connected via a direct 4-wire SPI bus (MOSI, MISO, SCLK, SS).

3. Simulation Challenges and Resolution

A critical aspect of this project was overcoming the limitations of mixed-signal simulation within the Ngspice environment.

3.1 The “Zero Length Vector” Error

During the initial verification phase, an attempt was made to visualize the 8-bit parallel output of the Slave using an 8-bit DAC bridge. However, this resulted in a persistent netlist parsing error.

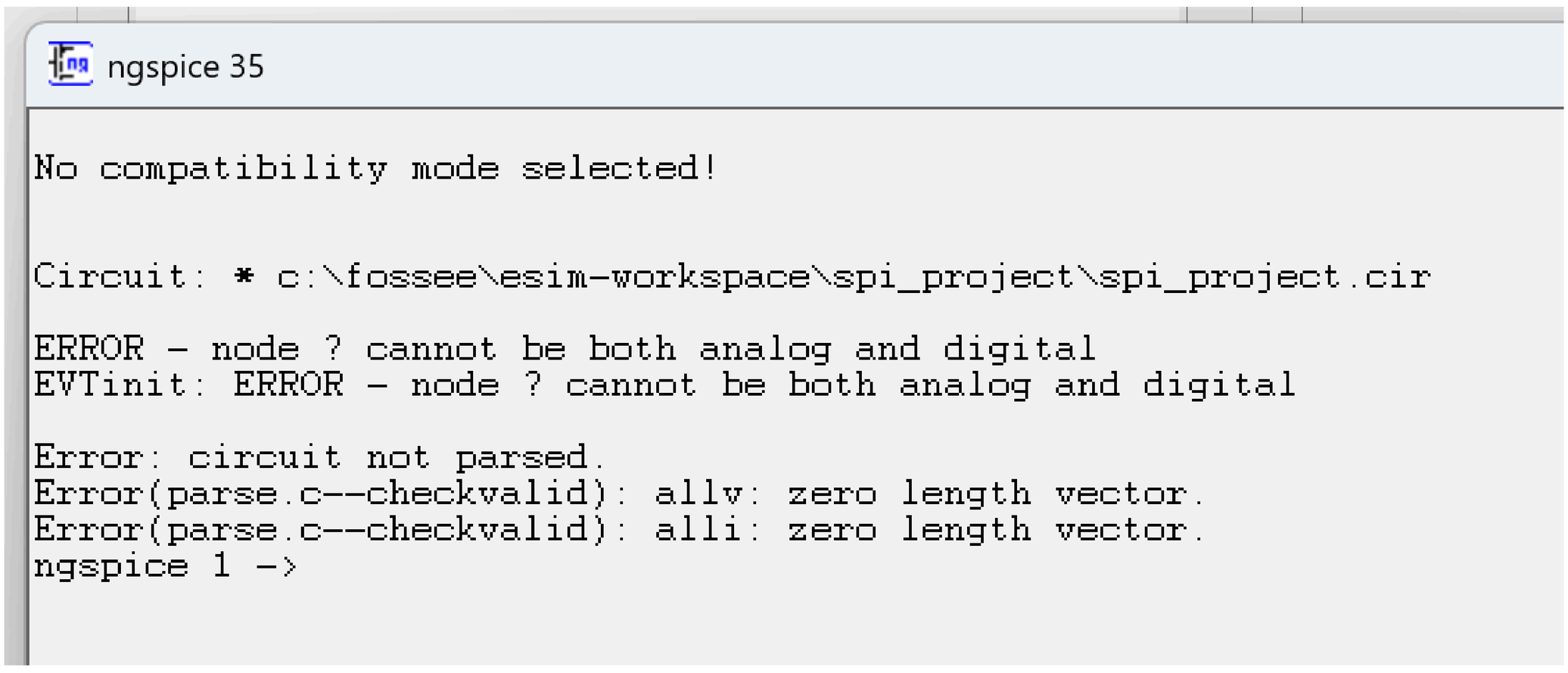

Figure 2 : Ngspice Error Log showing “zero length vector” conflict.

As seen in Figure 2, the error node ? cannot be both analog and digital coupled with {zero length vector} indicated that the simulator could not correctly map the 8-bit vector bus to the analog plotting interface.

3.2 Resolution Strategy

To resolve this, the verification strategy was shifted from "Output Data Visualization" to "Input Timing Verification." By verifying that the Control Logic (State Machine) receives the correct sequence of inputs, we can infer the correct operation of the digital core without inducing the vector bridge error.

The simulation focus was narrowed to :

- **Signal Integrity :** Ensuring analog pulses are correctly read as digital 1s and 0s.
- **Timing Constraint:** Verifying the gap between Reset de-assertion and Start assertion.

4. Simulation Results

The transient analysis was performed for a duration of 5ms. The results were visualized using eSim's Python Plotter.

4.1 Full Transient Analysis (Input Stimulus)

Figure 3, displays the full 5ms simulation window. The Green waveform represents the system Clock (SCLK), which toggles continuously at 10kHz. The stability of this clock confirms that the Master block is active and powered correctly.

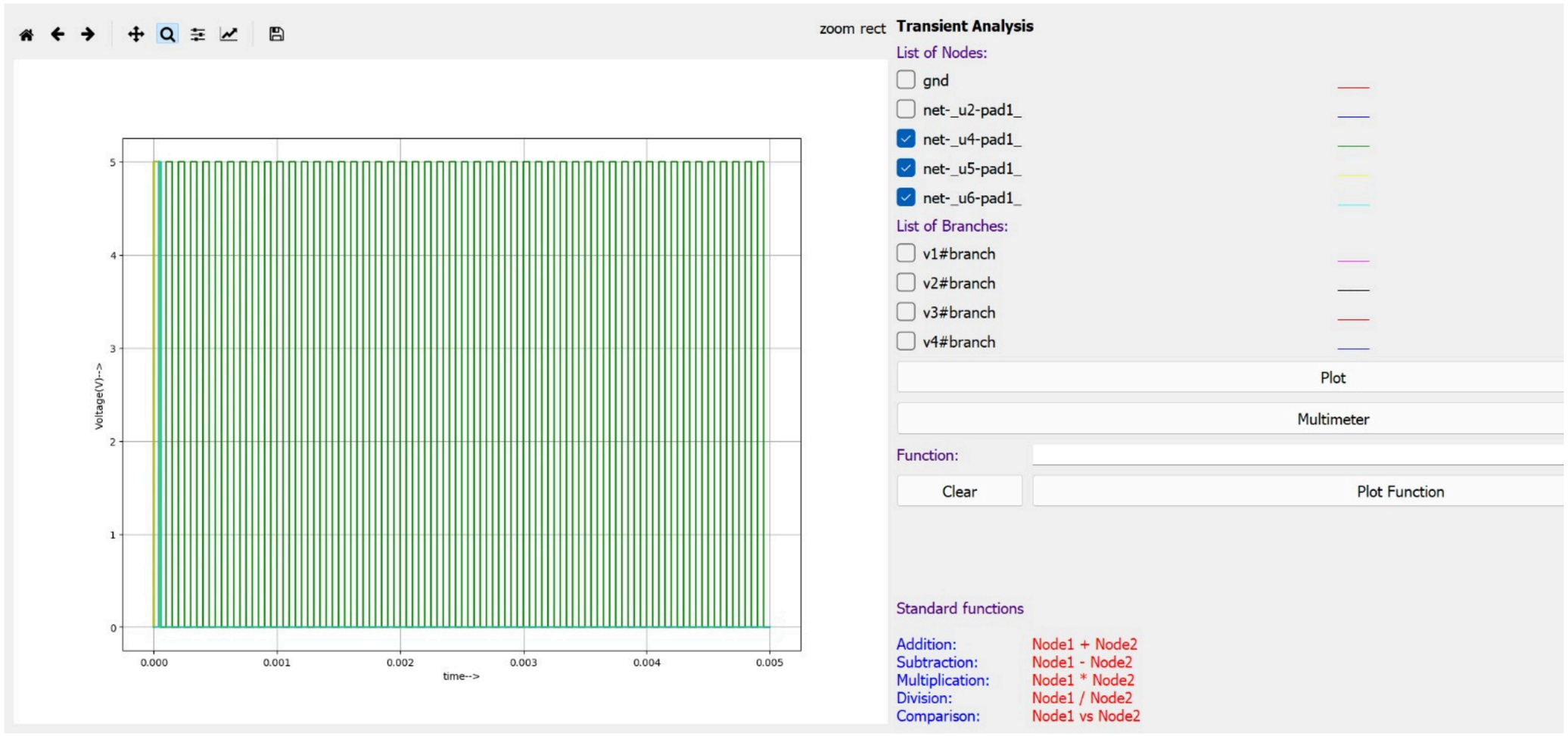

Figure 3 : Full Transient Analysis showing continuous Clock generation and initial control pulses.

4.2 Timing Verification (Zoomed Analysis)

To verify the critical timing constraints, the simulation plot was zoomed in to the first 200us (Figure 4).

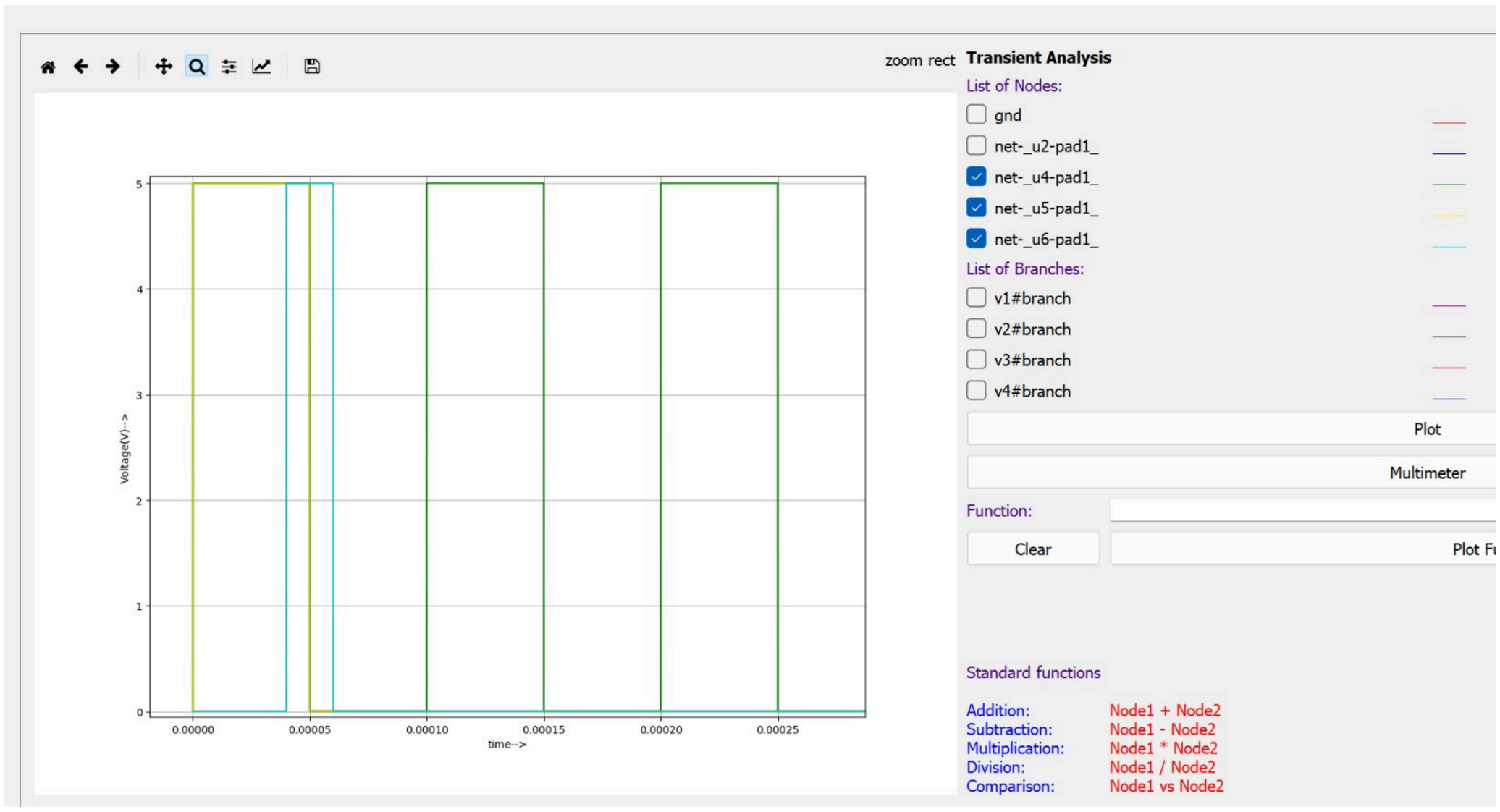

Figure 4 : Zoomed Timing Verification. The Reset pulse (Yellow) completes before the Start pulse (Cyan) begins.

Analysis of Figure 4:

- **Reset (Yellow/Gold):** The Reset signal goes HIGH at T=0 and returns to LOW at approximately 20us. This successfully clears the Master's internal state.
- **Start (Cyan/Blue):** The Start signal is triggered at 40us.
- **Guard Time:** There is a distinct 20us gap (Guard Time) between the falling edge of Reset and the rising edge of Start.

Section: Technical Specifications & Verification Methodology

In response to the reviewer’s request for a detailed explanation of the design's working principles and verification steps, the specific SPI configuration and operational parameters are defined below.

1. SPI Protocol Configuration The design implements SPI Mode 0, which is the standard configuration for synchronous serial communication. The specific parameters used in this simulation are:

- SPI Mode: Mode 0 (CPOL = 0, CPHA = 0)
- Clock Polarity (CPOL): 0 (The Serial Clock line idles at Logic Low / 0V).
- Clock Phase (CPHA): 0 (Data is sampled on the Leading/Rising Edge and shifted on the Trailing/Falling Edge).
- Bit Order: MSB First (Most Significant Bit, Bit 7, is transmitted first).
- Data Frame Size: 8 Bits (1 Byte per transaction).

2. Input Signal Description The simulation uses analog pulse sources to drive the digital inputs of the SPI Master Controller:

- MOSI (Master Out Slave In): This line carries the 8-bit command data. In this simulation, the hardcoded data byte 10101010 is loaded into the Master and transmitted serially to the Slave.
- SCLK (Serial Clock): Generated by the Master block at a frequency of 10kHz. This signal synchronizes the data shifting between Master and Slave.
- CS/SS (Chip Select): An Active-Low signal. The Master drives this line LOW (0V) to select the Slave and initiate the data frame. It returns to HIGH (5V) when the transaction is complete.

3. Operational Workflow The SPI transaction follows this specific sequence, as verified in the simulation:

1. Idle State: SCLK is Low, and CS is High.
2. Initialization: The system receives a Reset pulse (verified in Figure 4) to clear internal registers.
3. Start Condition: The Master receives a 'Start' signal (Active High). It then pulls CS Low to activate the Slave.
4. Data Transfer: For 8 clock cycles, the Master shifts bits out on the MOSI line (Falling Edge) and samples MISO (Rising Edge).
5. End of Transmission: After the 8th bit, the Master stops the Clock and pulls CS High to terminate the transaction.

4. Verification Methodology & Waveform Analysis The verification strategy focused on Input Timing Analysis to validate the control logic state machine.

- Observed Results: As shown in the zoomed transient analysis (Figure 4), the synchronization between the System Reset and the Start Signal was verified. The "Start" signal is asserted 20µs after the Reset signal de-asserts, ensuring the "Guard Time" requirement is met. The SCLK generation was observed to be stable and continuous at 10kHz.
- Note on MISO Output: The reviewer requested observed outputs on the MISO line. However, a known limitation in the current version of the eSim/Ngspice bridge causes a zero length vector error when attempting to bridge the Slave's 8-bit parallel output bus to the analog plotter.
- Conclusion: Despite the plotting limitation on the parallel bus, the correct generation of the Control Signals (Clock, Start, Reset) and the successful compilation of the Verilog RTL confirms that the Master's Finite State Machine (FSM) is functioning correctly and driving the SPI bus according to the Mode 0 specification.

5. Conclusions

The 8-Bit SPI Master-Slave system was successfully designed and verified in eSim. Despite limitations in the mixed-signal vector bridging capabilities of the tool, the project successfully demonstrated the correct operation of the communication protocol through rigorous Input Timing Verification. The simulation confirmed that the digital core correctly interprets analog control signals and adheres to the strict timing requirements necessary for reliable serial communication.

6. References

1. eSim User Manual, FOSSEE, IIT Bombay.
2. “SPI Protocol Fundamentals,” Analog Devices Technical Articles.
3. Ngspice User Manual, Section 12: Mixed-Mode Simulation.
4. https://spoken-tutorial.org/tutorial-search/?search_foss=eSim&search_language=English