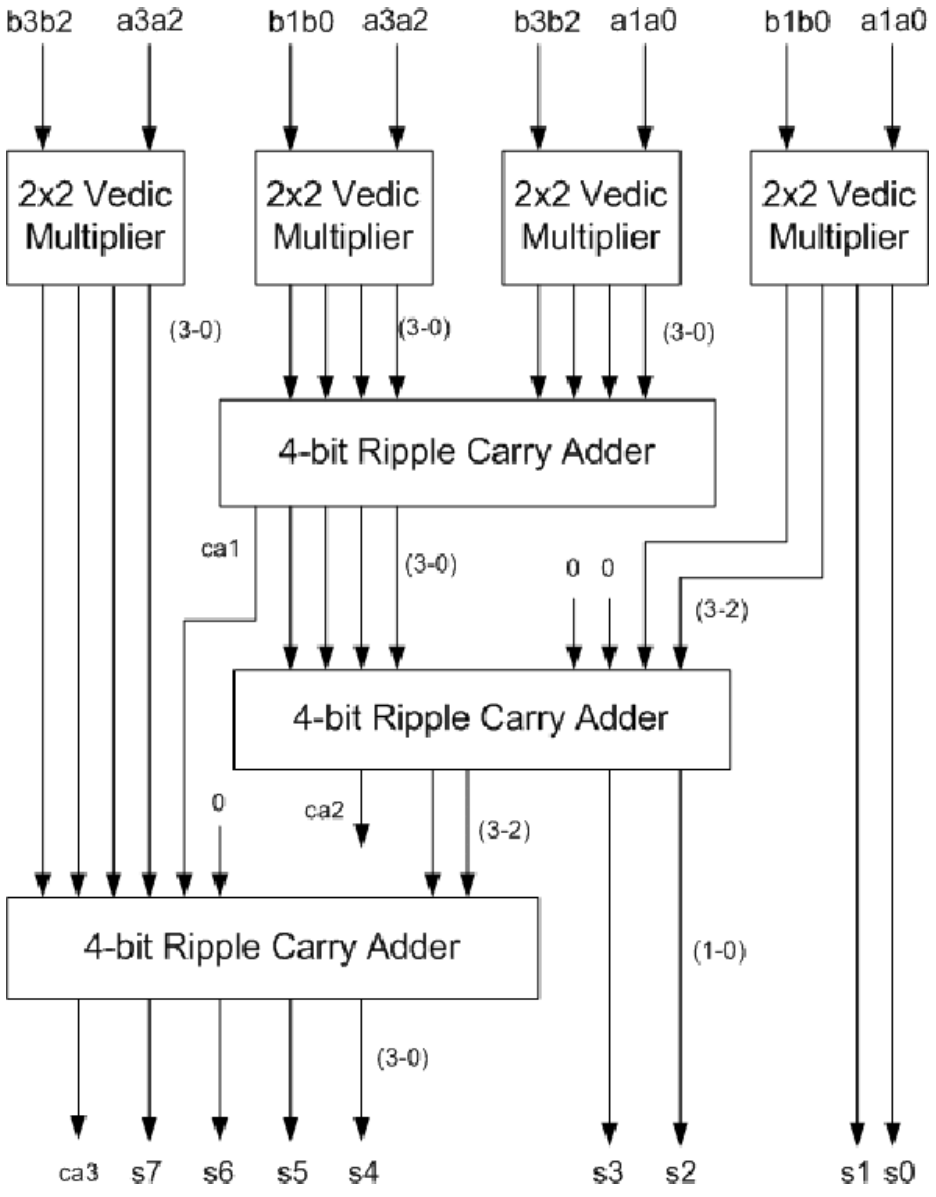
4-bit Vedic multiplier

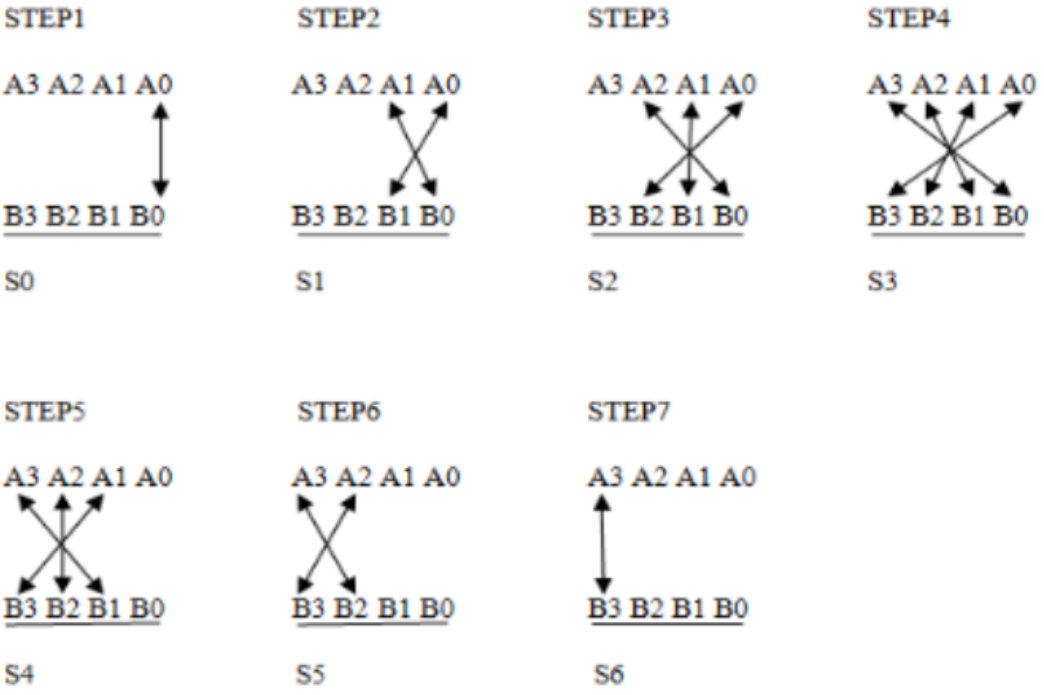
1. Abstract

The performance of the multiplier figures out the system performance because the multiplier is the slowest element in the system. Multiplication is one of the major operations in arithmetic and logical operations and multiplier is used in many applications like FFT, DFT, Image enhancement, DWT etc., The multiplication speed influences the processor speed, so the speed of the multiplication should be high. There is one such promising solution i.e., Vedic multiplier. Vedic multiplier is designed using Vedic mathematics. Vedic mathematics is an ancient system of mathematics, which is formulated by Sri Jagadguru Bharathi Krishna Tirthaji (1884-1960). The word Vedic is obtained from the word —Veda which gives the meaning of powerhouse of knowledge and Devine.

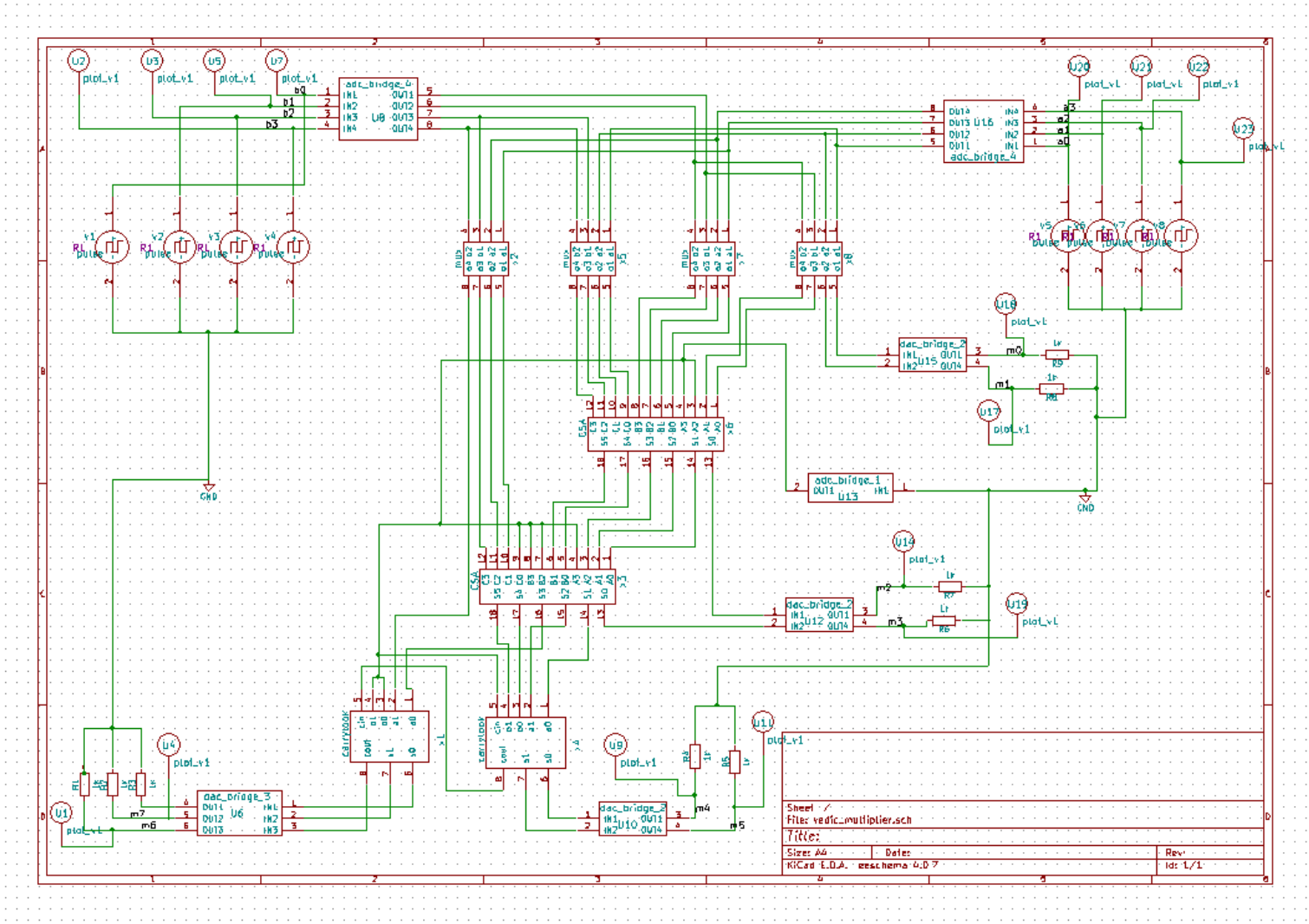
2. Block diagram



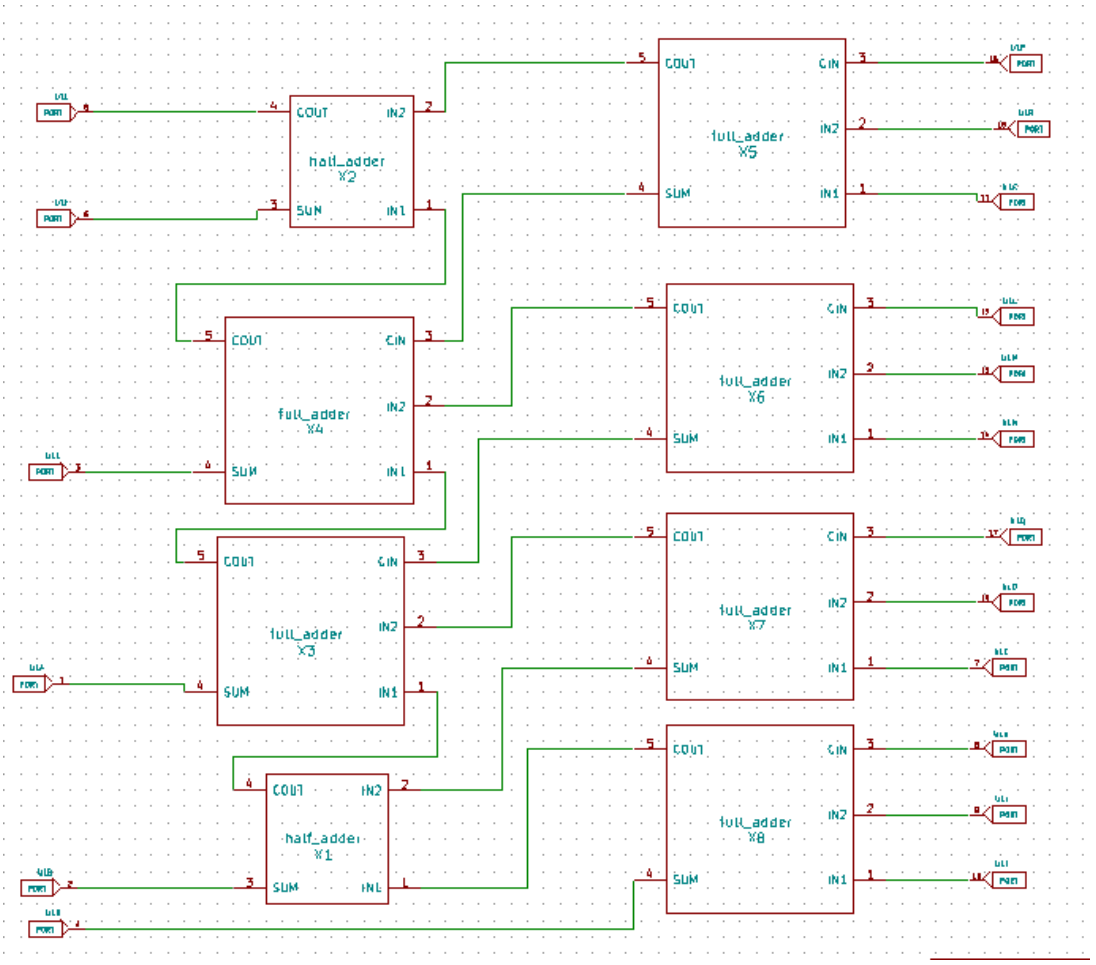
3. Example


STEP1
A3 A2 A1 A0
B3 B2 B1 B0
S0
STEP2
A3 A2 A1 A0
B3 B2 B1 B0
S1
STEP3
A3 A2 A1 A0
B3 B2 B1 B0
S2
STEP4
A3 A2 A1 A0
B3 B2 B1 B0
S3
STEP5
A3 A2 A1 A0
B3 B2 B1 B0
S4
STEP6
A3 A2 A1 A0
B3 B2 B1 B0
S5
STEP7
A3 A2 A1 A0
B3 B2 B1 B0
S6

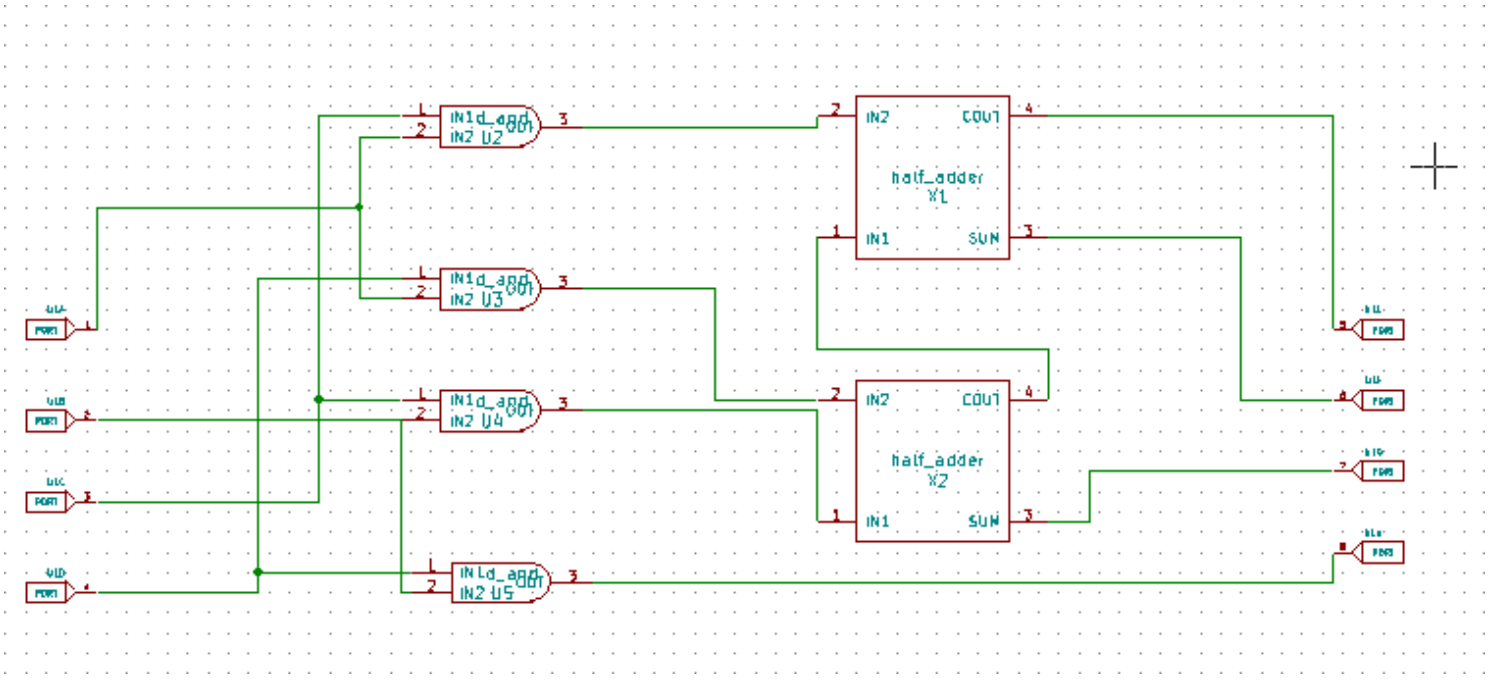
4. Schematic Diagram:



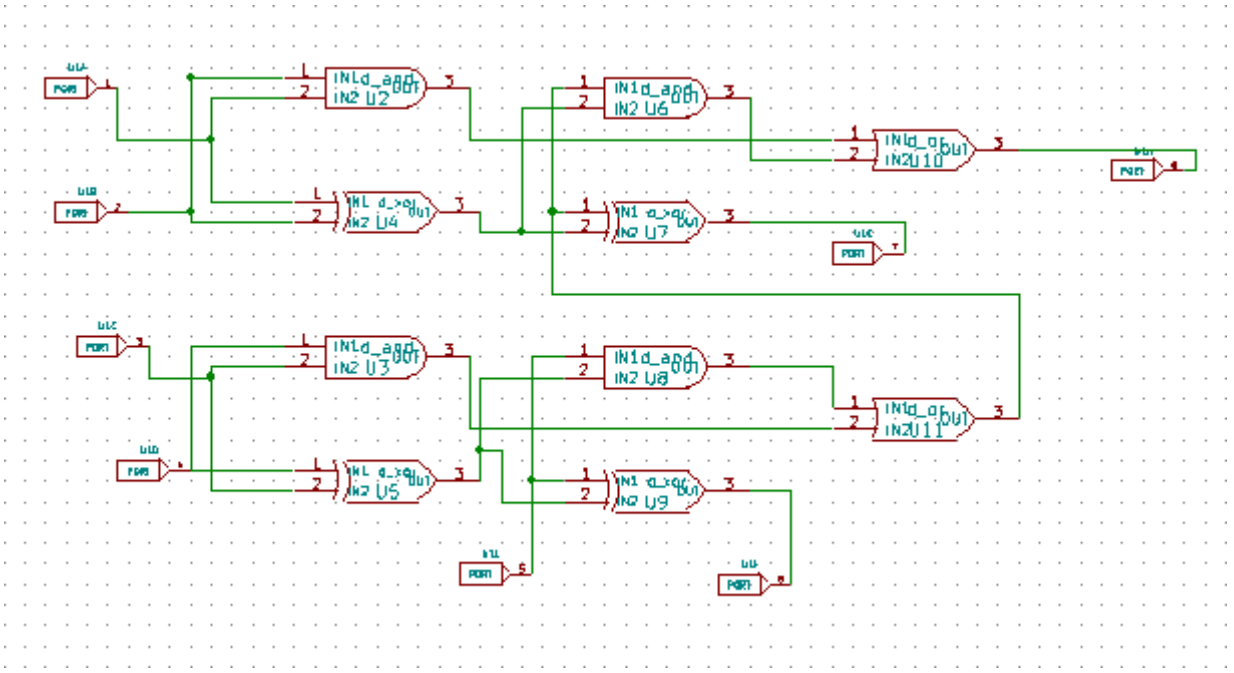
5. Sub circuits



Carry save adder

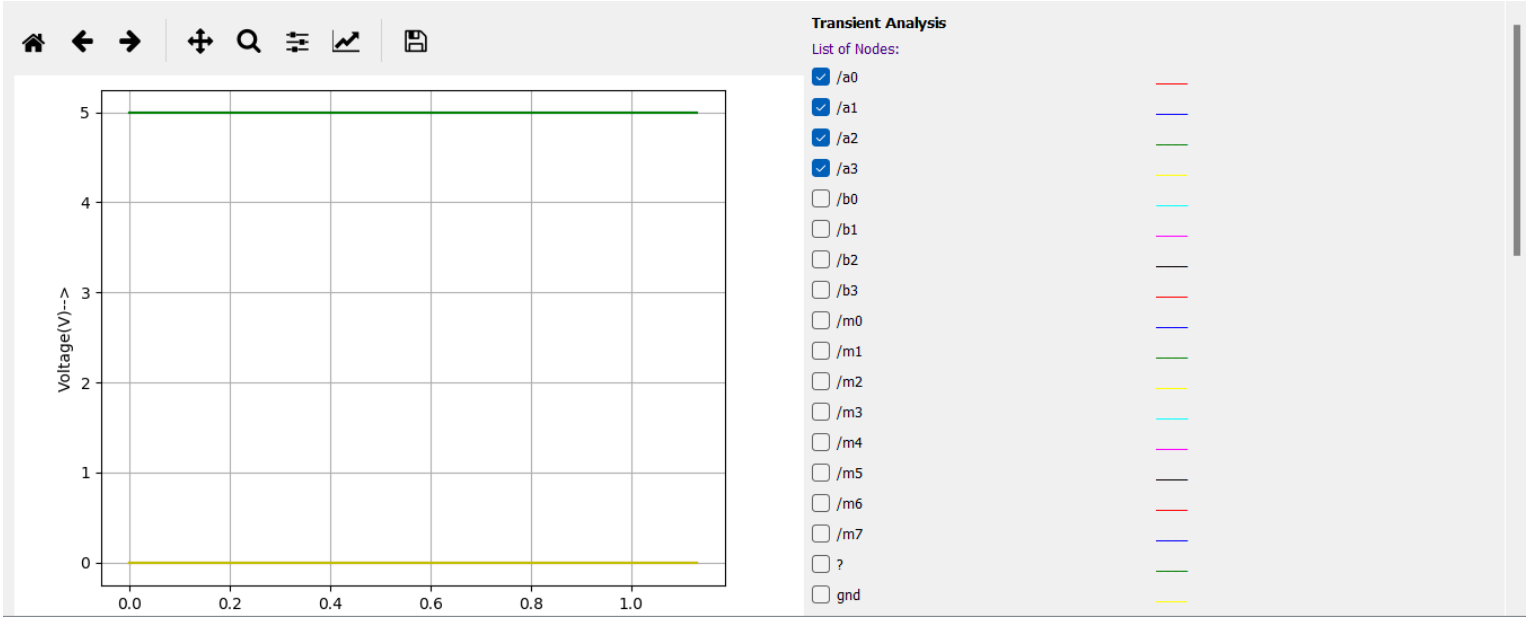


2*2 mux

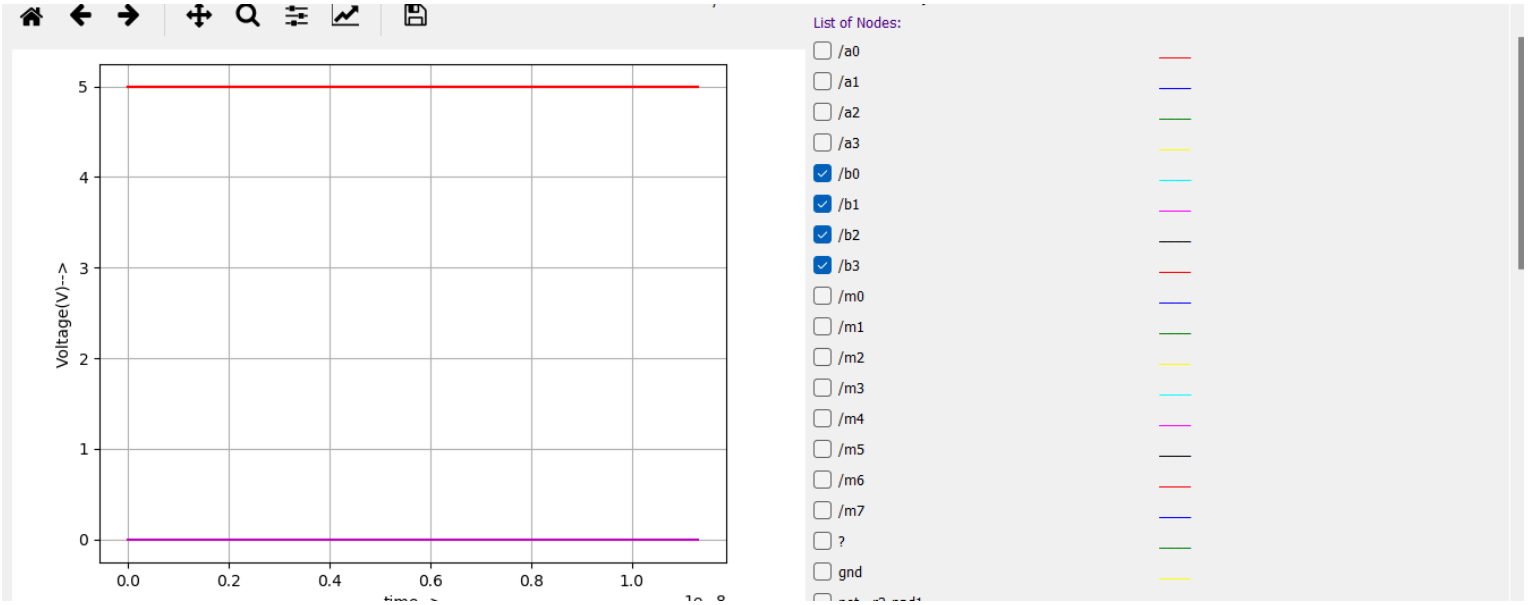


Carry look ahead adder

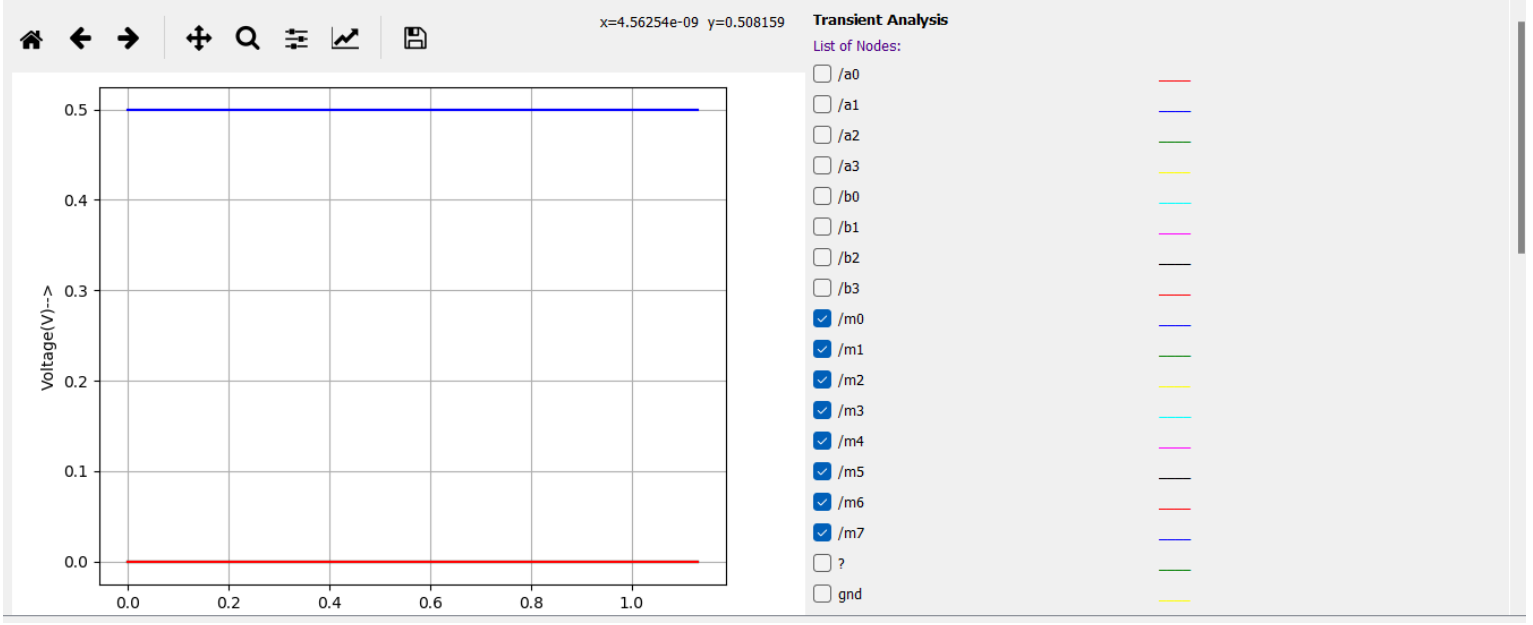
6. Output Waveforms



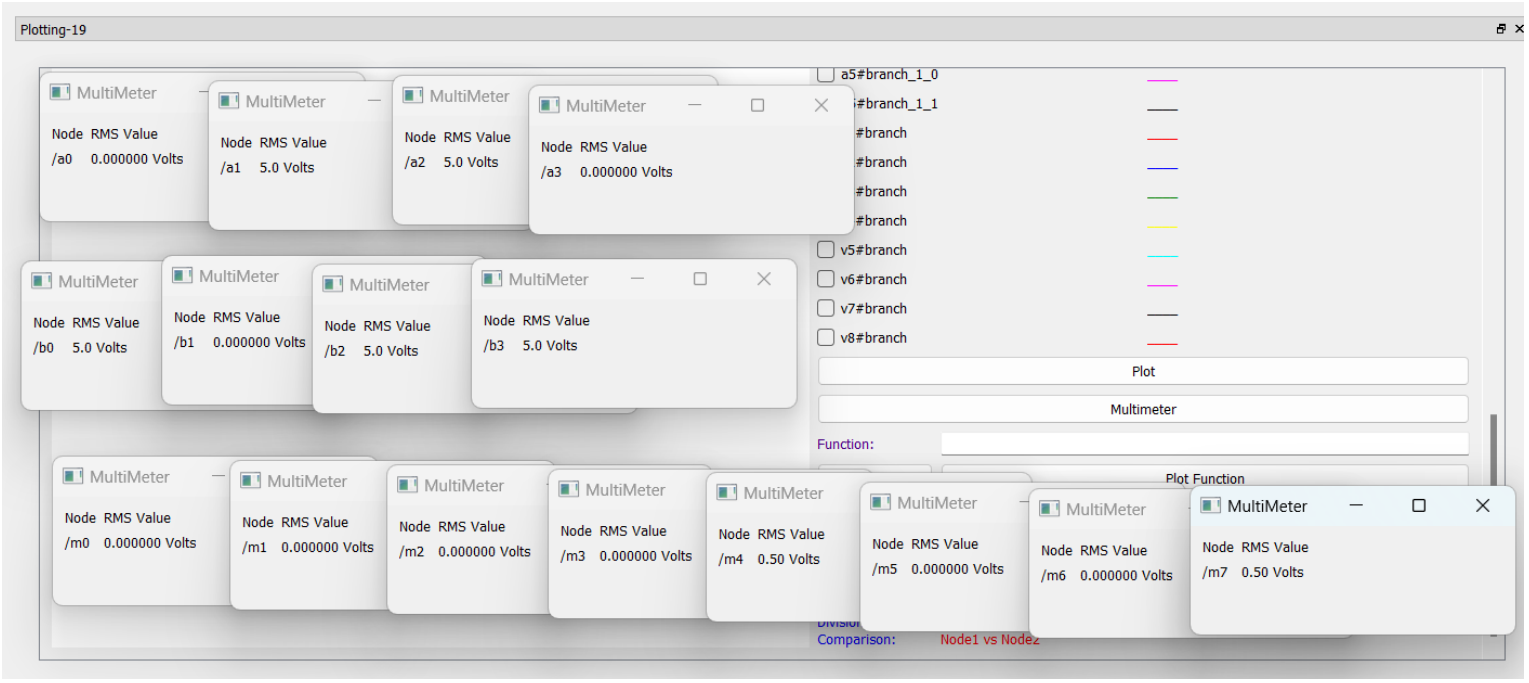
A0 A1 A2 A3

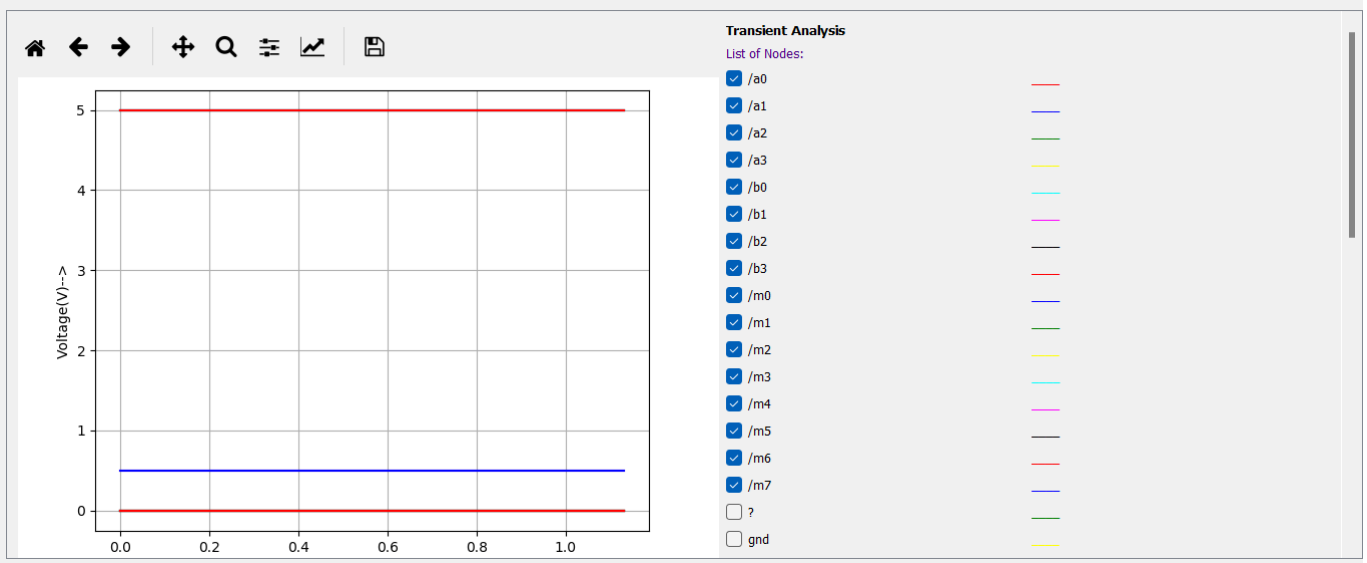


B0 B1 B2 B3



M[0: 7]





References:

[1] http://www.iraj.in/journal/journal_file/journal_pdf/1-495-154079221642-46.pdf

[2] https://digitalsystemdesign.in/vedic-multiplier/?srsltid=AfmBOopp3u_iqzdjGAnrtIouc-IafBERYQ9v8Rog_M8mD_fQ_8tGvxPG

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