### Frequency Divider Using Flipflops

(Divide by 16)

#### 1. Introduction

A **frequency divider** is a digital circuit that reduces the frequency of an input signal by a specific factor, which is generally a power of two. These circuits are widely used in various applications such as clock generation, signal processing, and timing systems in digital electronics. The frequency divider circuit operates by using a series of flip-flops to divide the frequency of a periodic input signal. In this project, we aim to design a frequency divider that divides the input clock frequency by 16 using flip-flops. The choice of a divide-by-16 configuration means that for every 16 cycles of the input signal, the output signal will have just one cycle, thus effectively reducing the frequency by a factor of 16.

### 2. Theory

It works based on the principle that a flip-flop toggles its state (either from 0 to 1 or 1 to 0) at every clock pulse. A single flip-flop divides the input clock frequency by 2. To achieve a higher division factor, multiple flip-flops are cascaded in a series. The divide-by-16 configuration can be constructed by cascading four flip-flops, as each flip-flop reduces the frequency by half.

#### 2.1. Applications

- Clock generation and management in microcontrollers and digital systems.
- Pulse width modulation (PWM) frequency adjustment.
- Digital counters and timers.
- Communication systems where different frequencies are needed at various stages.

### 3. Truth Table

count	f/16	f/8	f/4	f/2
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1

## 4. Circuit



## 5. Schematic Diagram



# 6. Output Waveforms





input clock







f/8



f/16

all frequencies

## References

- [1] https://www.scribd.com/document/401388520 /Frequency-Divider-D-Flip-flops-docx
- [2] https://vlsicoding.blogspot.com/2014/07/ implement-divide-by-2-4-8-16-counter-using-flip-flop.html

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