Circuit Simulation Project

Name of the participant :Dr. Ujwala Sushil Ghodeswar

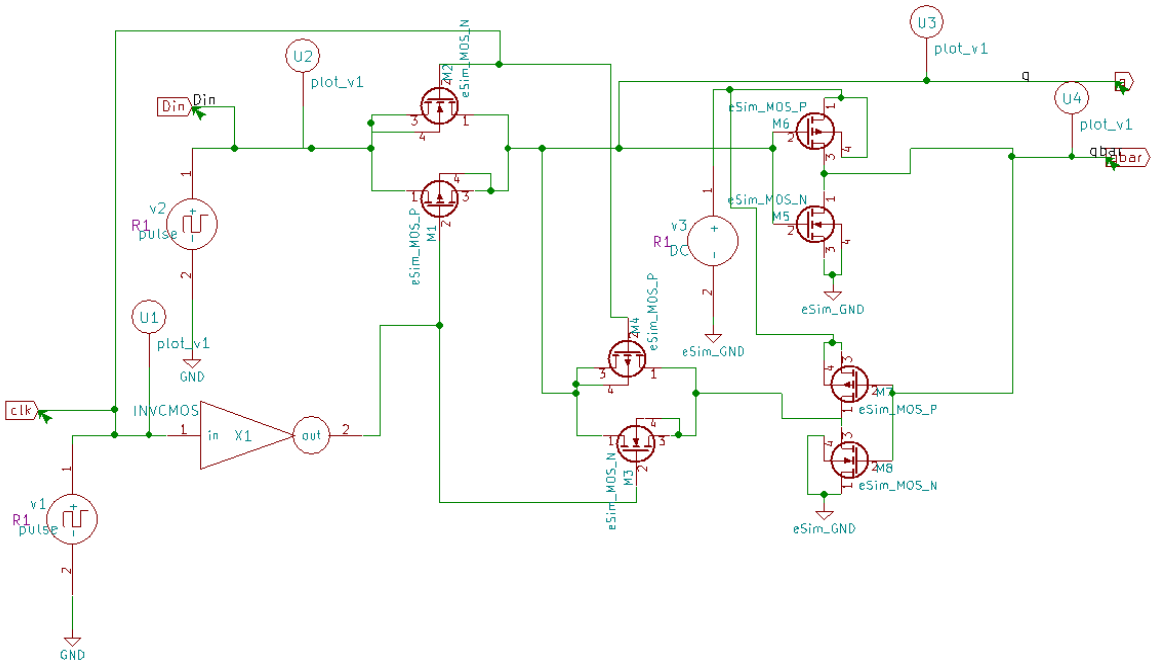
Title of the circuit : Design of positive level triggered CMOS D Latch circuit

Theory/Description :

Design of positive level triggered D latch is designed using MOS transistors at 180nm technology. In this circuit two CMOS inverters, two transmission gates are used. When the clock input is one then input D is connected to the output Q. If the voltage applied to D input is logic level one i.e. 1.8 V then the voltage at Q output is also logic level one i.e. 1.8 V. If the voltage applied to D input is logic level zero i.e. 0 V, then the Q output is same as input. Output voltage at Qbar is equal to the complement of voltage obtained at output Q. This circuit works at the positive level of clock signal hence it is called as positive level triggered D latch.

Power supply of 1.8 Volts is applied for proper conduction of circuit. The design includes schematics design of D latch using NMOS and PMOS transistors. Input source D and Clock is applied. Output of the circuit can be validated using Truth table. All the values can be verified from the truth table.

Circuit Diagram(s) :

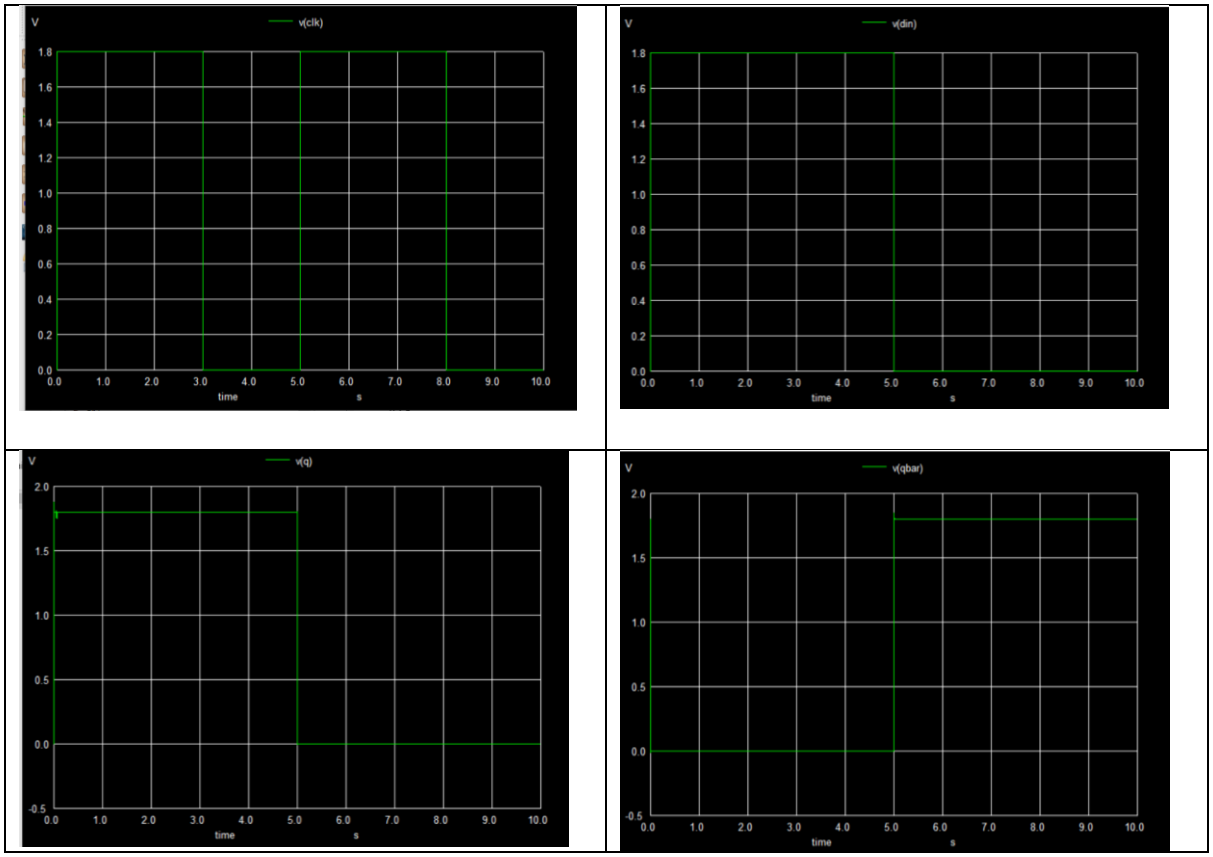


Truth Table:

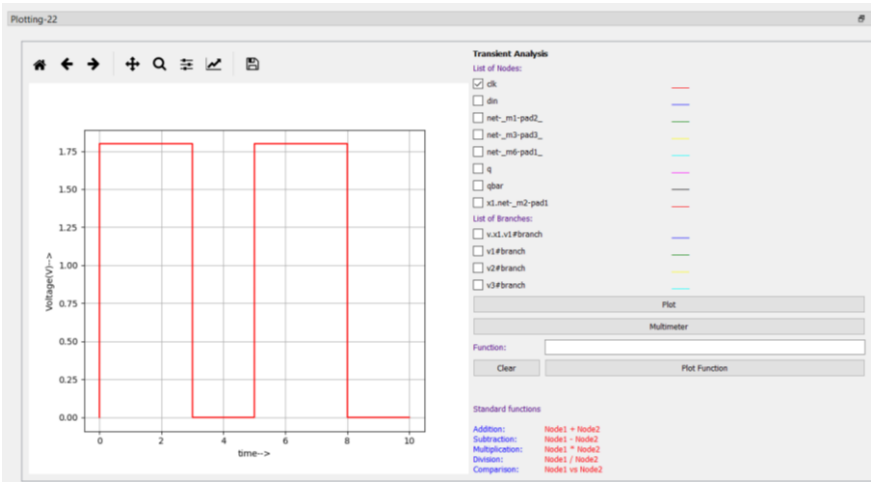
Input Clock(CLK)	Input D	Output Q	Output Qbar
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Results (Input, Output waveforms and/or Multimeter readings) :

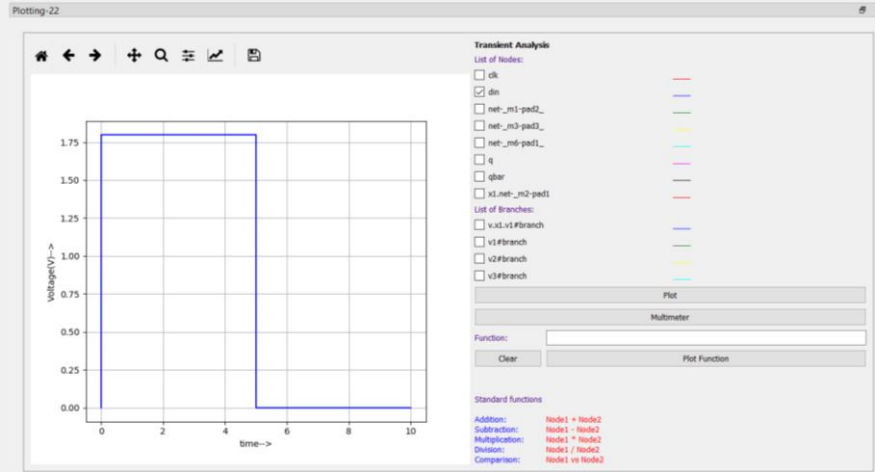
NGSPICE Plot:



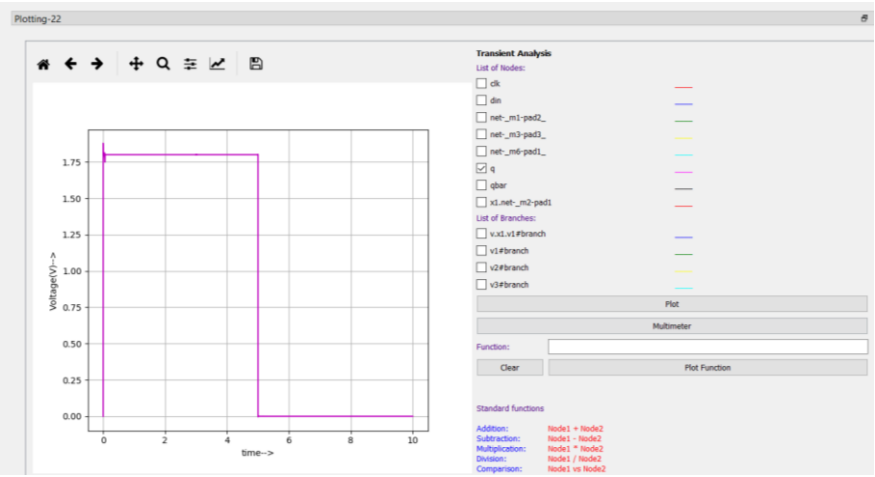
Python Plot of Input clk:



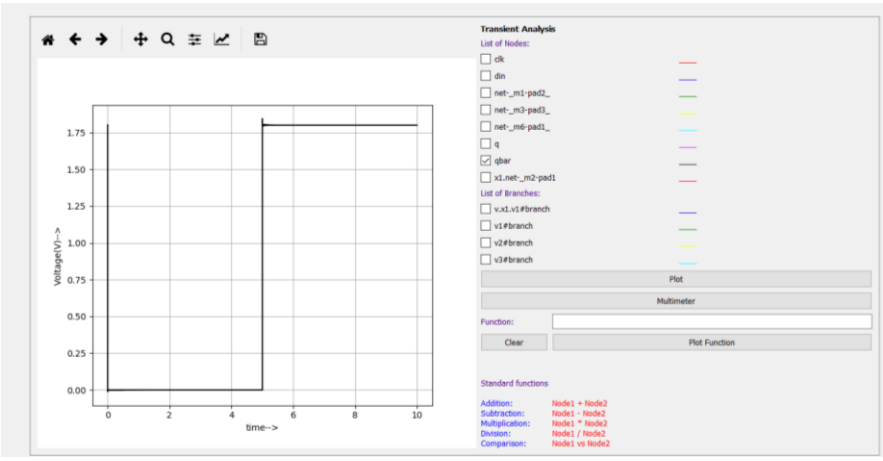
Python plot of Input Din



Python plot of output Q:



Python plot of output Qbar:



Source/Reference(s) :

1)CMOS VLSI Design A circuit and systems perspective by Neil H.E.Weste,David M.Harris. fourth edition.

Conclusion: Thus, Positive Level Triggered CMOS D Latch Circuit was designed using Transmission gate and output waveform obtained successfully using eSIM software.