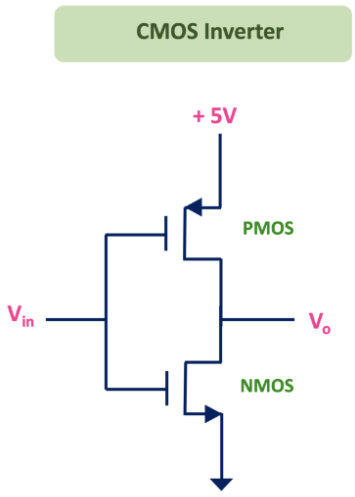
Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

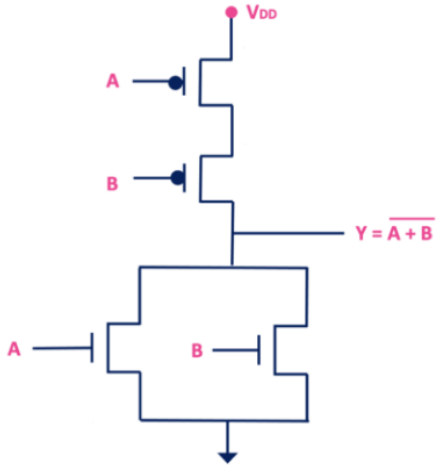
Name of the participant : Vithul Vinu

Title of the circuit : LOGIC GATES REPRESENTED USING CMOS IN A SINGLE CIRCUIT

Theory/Description : The project involves the design and simulation of an integrated circuit containing CMOS-based logic gates: NOT, AND, NOR, NAND, XOR, and XNOR. Each gate is controlled by two input voltages, A and B. With a Single Circuit all the logic gate outputs are observed at the same time. Using simulation tools like NGSPICE or KiCad, the circuit's functionality will be validated and optimized for performance and efficiency. The final integrated circuit will demonstrate the practical implementation of these gates in a cohesive system, with comprehensive documentation detailing the design process, simulation results, and optimization strategies.



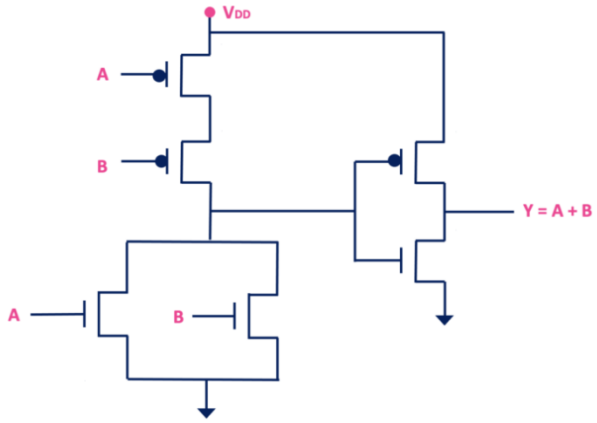
NOR Gate



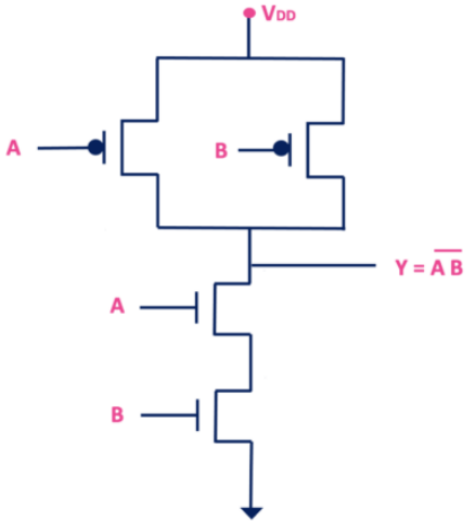
Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

OR Gate



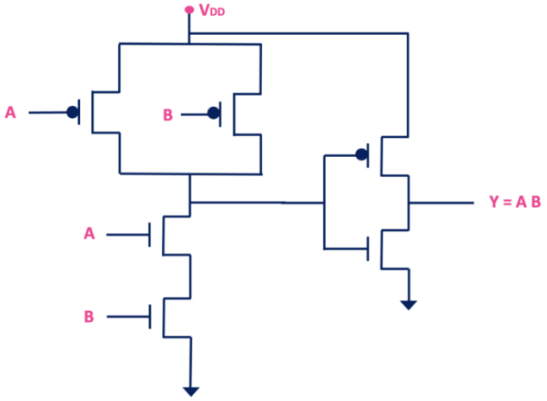
NAND Gate:



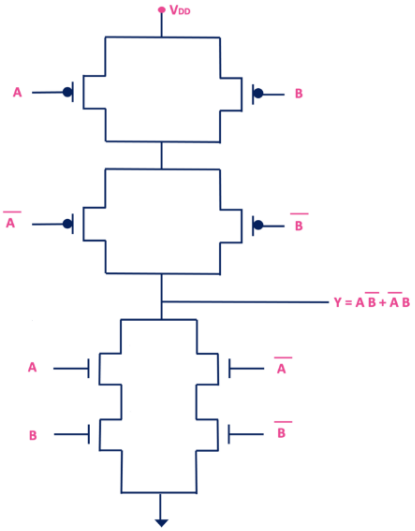
Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

AND Gate



XOR Gate



Buffer

Input	Output
0	0
1	1

Inverter

Input	Output
0	1
1	0

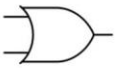
AND

A	B	Output
0	0	0
1	0	0
0	1	0
1	1	1

NAND

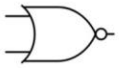
A	B	Output
0	0	1
1	0	1
0	1	1
1	1	0

OR



A	B	Output
0	0	0
1	0	1
0	1	1
1	1	1

NOR



A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

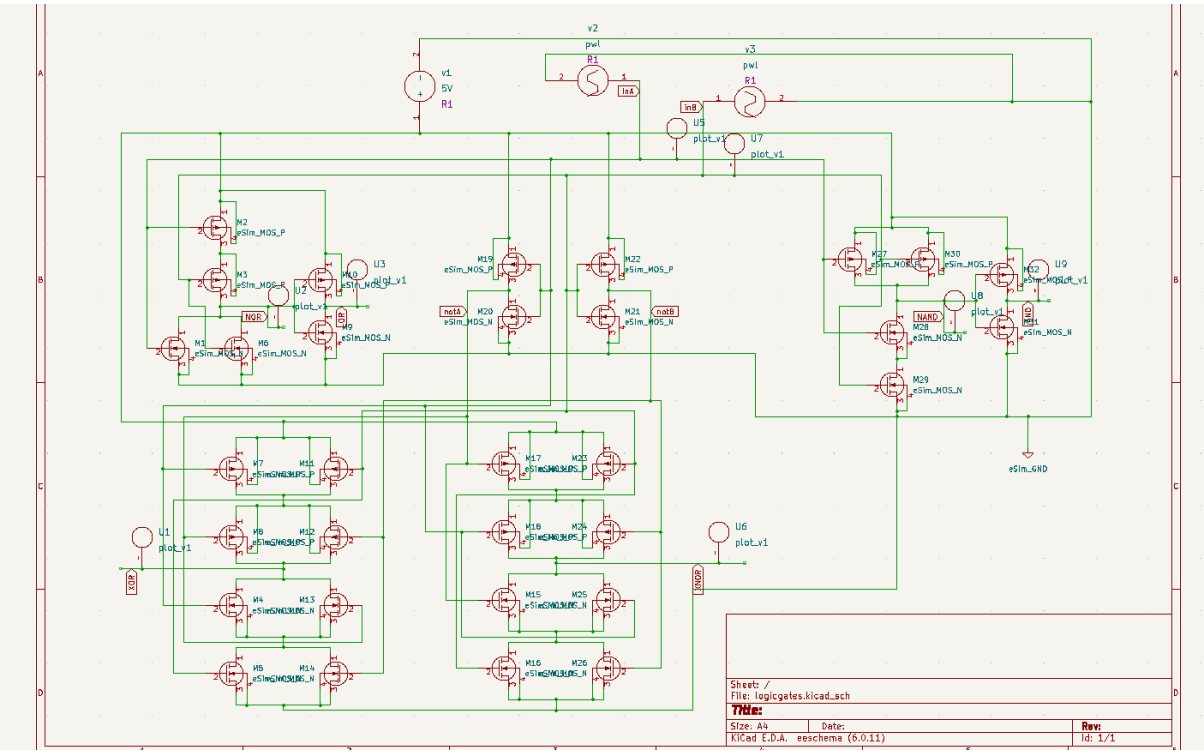
XOR

A	B	Output
0	0	0
1	0	1
0	1	1
1	1	0

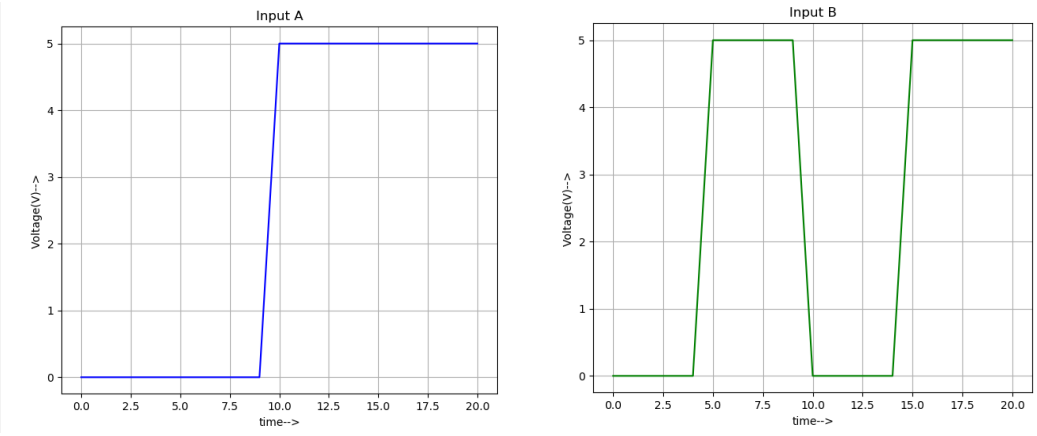
XNOR

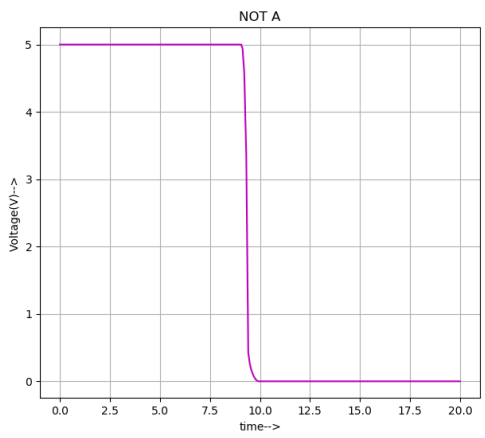
A	B	Output
0	0	1
1	0	0
0	1	0
1	1	1

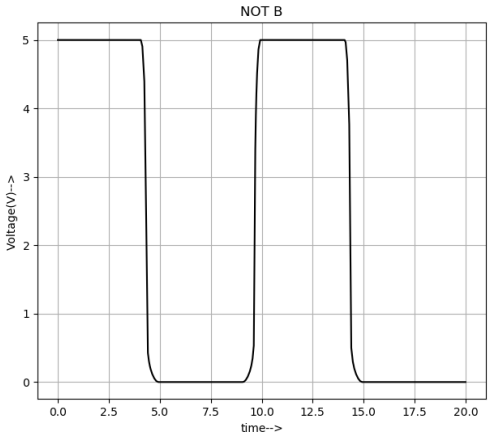
Circuit Diagram(s) :

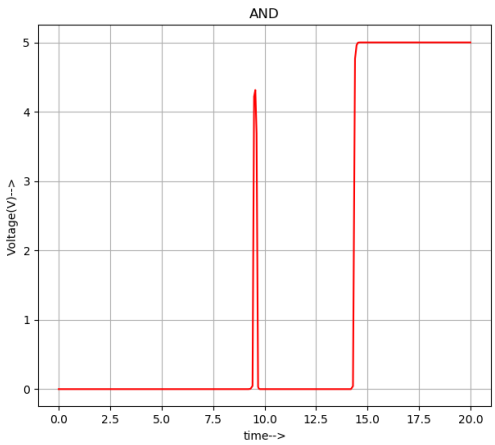


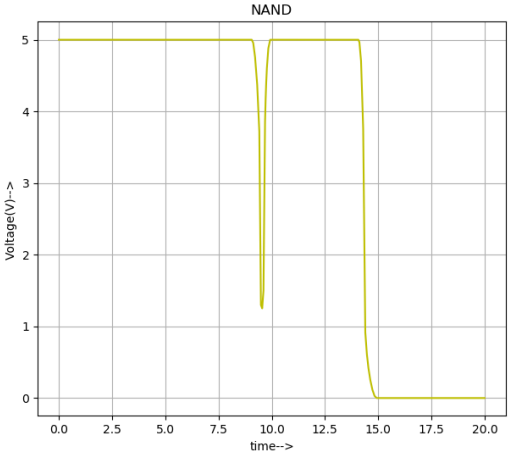
Results (Input, Output waveforms and/or Multimeter readings) :

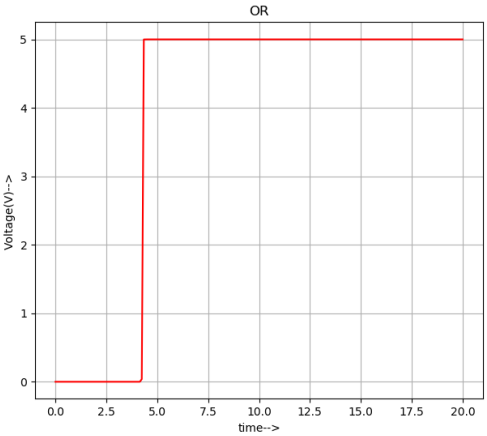


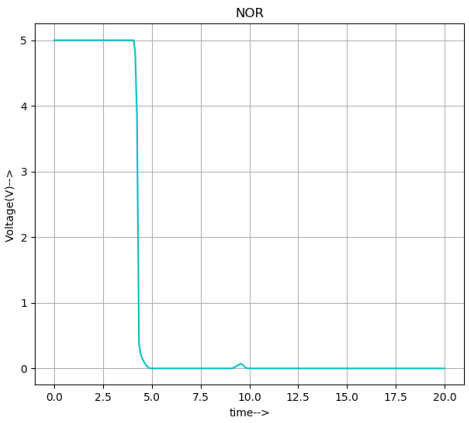

NOT A
Voltage(V)-->
time-->

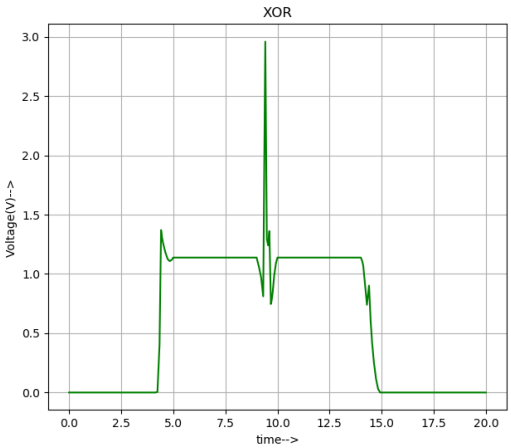

NOT B
Voltage(V)-->
time-->

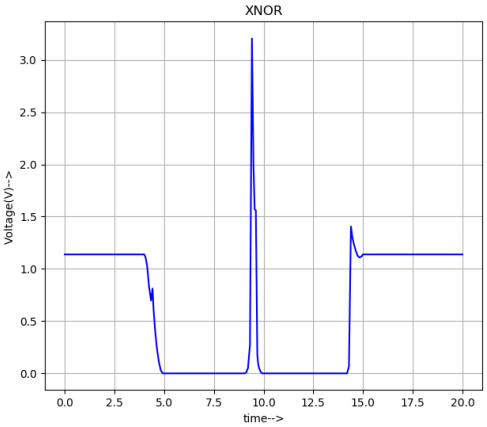

AND
Voltage(V)-->
time-->


NAND
Voltage(V)-->
time-->


OR
Voltage(V)-->
time-->


NOR
Voltage(V)-->
time-->


XOR
Voltage(V)-->
time-->


XNOR
Voltage(V)-->
time-->

Source/Reference(s) :

https://www.allaboutelectronics.org/cmos-logic-gates-explained/

https://youtu.be/R2y5bXrKBXw?si=IDAwoHTDL2CKtNIN