Design and Implementation of 3x3 CNOT Peres Quantum Gate using SKY130

Name Of Participant: **Aditya Minocha**

Project Title: Design and Implementation of 3x3 CNOT Peres Quantum Gate using SKY130

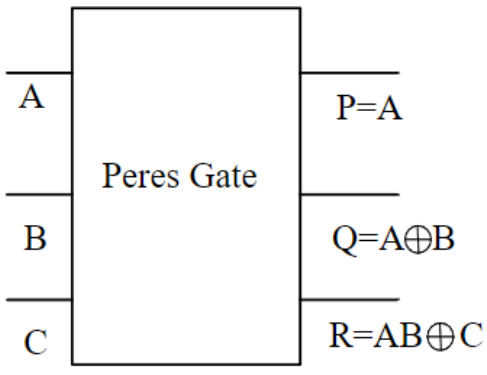
Abstract:

Quantum computing represents a thriving and captivating realm of research, drawing inspiration from the principles of Quantum Mechanics. It holds the promise of revolutionizing computers as we know it, by paving the way for constructing vastly more efficient computers than those existing today. One of its most intriguing features lies in its potential to solve certain problems that are virtually unsolvable in polynomial time within the classical domain, accomplishing this feat in polynomial time within the quantum domain. Additionally, the complexity of various problems can be significantly reduced by transposing them into the quantum domain. Quantum Circuits (QCs) present another compelling advantage, enabling the execution of massively parallel computations in a single time step.

Keeping the growing popularity of quantum gates in mind, this project is based on the design and implementation of a Reversible Quantum Gate, which forms the building blocks of quantum computing.

This project proposes the design of a 3x3 Reversible Peres Gate, using SKY130 in eSim software. A Peres gate is a 3 inputs 3 outputs (3×3) reversible gate having the mapping,

(A, B, C) to (P =A, Q =A XOR B, R =(A.B) XOR C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. It is comprised of two XOR gates and one AND gate. A circuit is called reversible only when its inputs can be determined from its outputs and the input-output possesses one-to-one mapping. Fredkin gate, Toffoli gate, interaction gate, and switch gate are other such examples of reversible logic gates.



A 3x3 Peres Quantum Gate

These logic gates have the number of outputs to be always equal to the number of inputs. Reversible logic gates are memoryless logic units and the function realized by a reversible circuit is a mathematically Injective logic function. Reversible logic gates are attracting a lot of attention due to their zero-power dissipation under ideal conditions. The important cost metrics in reversible logic circuits are the quantum cost, the delay, and the number of garbage

outputs. Garbage outputs are the unutilized outputs in reversible circuits that exist just to maintain reversibility but do not perform any useful operations. The Quantum Cost of Peres Gate is estimated to be 4.

The reversibility of computation has been achieved in such gates at the cost of introducing the constant inputs and garbage outputs, but less energy dissipation. The reversible logic has found various applications in quantum computing, low-power VLSI Design, optical computing, and many more.

In quantum computation, quantum bits (qubits) are used instead of classical binary bits to represent information. These information units are derived from the states of micro-particles such as photons, electrons, or ions. These states are the basis states of the computational quantum system. The 3x3 Reversible Peres Quantum Gate extends the functionality of the Peres Quantum Gate to operate on three qubits.

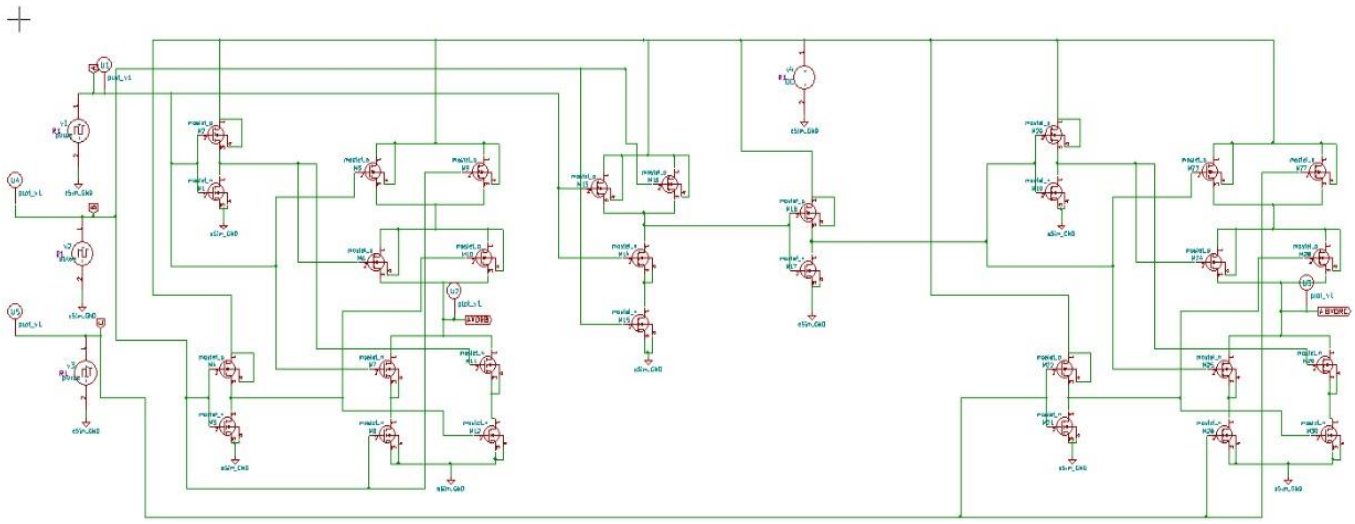
It aims to detect entanglement among these qubits, where their states are intricately correlated despite physical separation. If the qubits are entangled, the gate produces a specific output indicating the presence of entanglement; otherwise, it outputs a different result suggesting independent states. The gate's reversibility ensures that the quantum information encoded in the input qubits can be retrieved from the output, a crucial requirement in quantum computing to preserve information integrity and avoid loss.

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Truth Table of 3x3 Peres Quantum Gate

Circuit Diagram

The following circuit is the implementation of a 3x3 Peres Gate using eSim software.



Circuit Diagram

Results :

Simulated Plots from NG Spice - Inputs

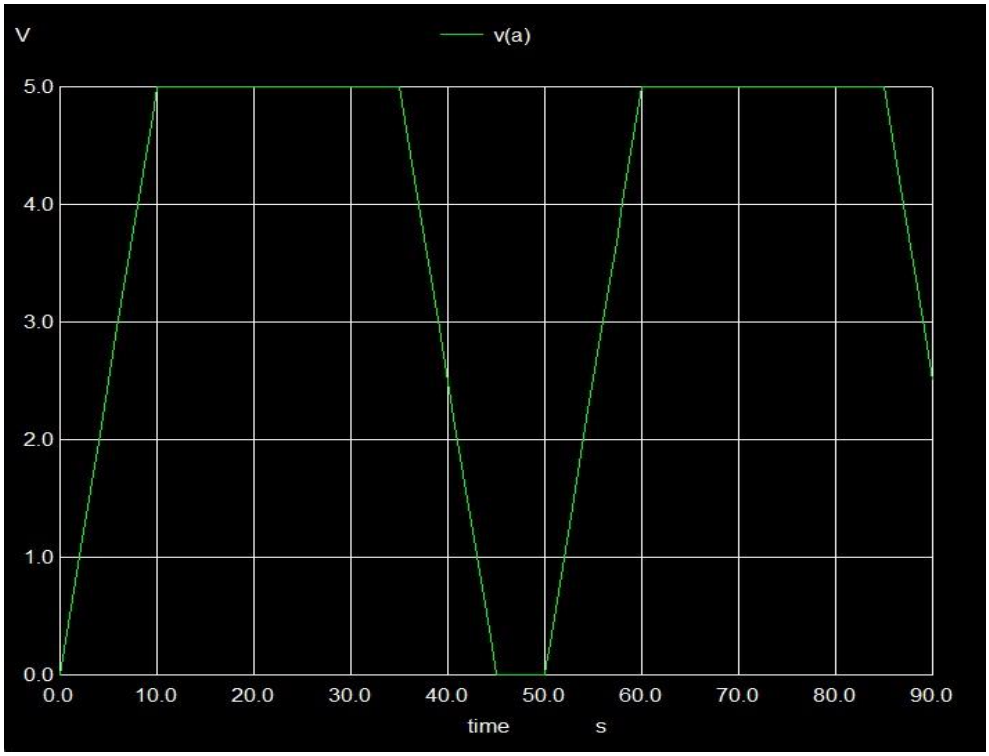


Figure 1 - Graph of Input A

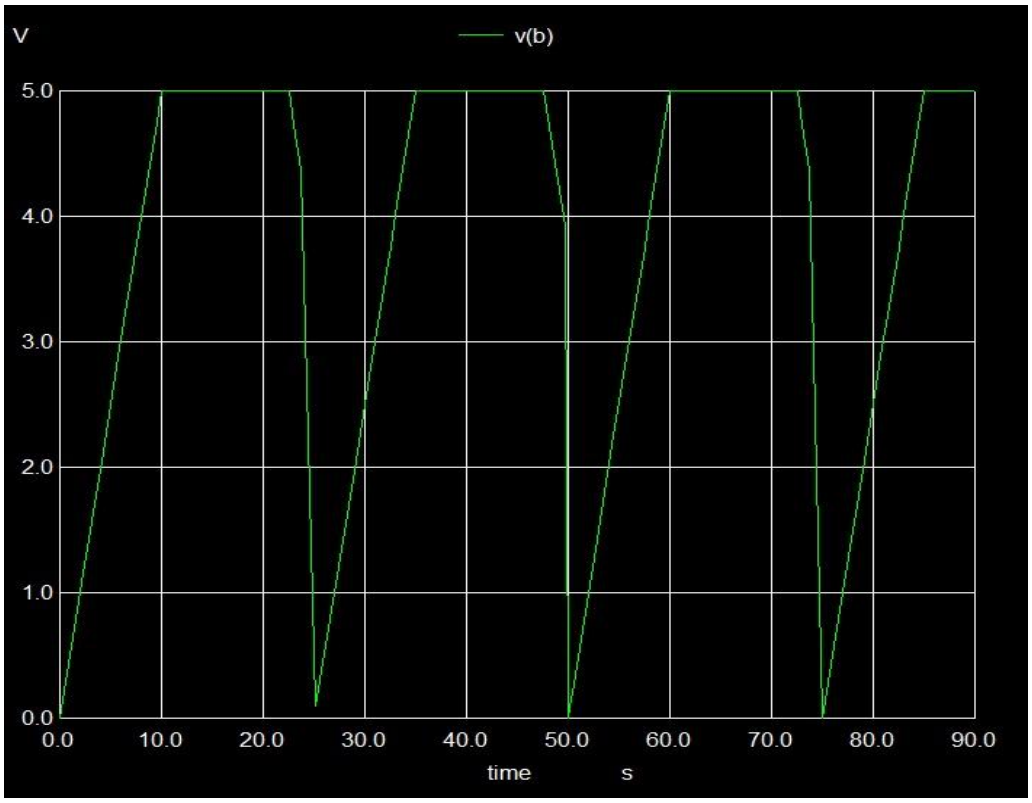


Figure 2- Graph of Input B

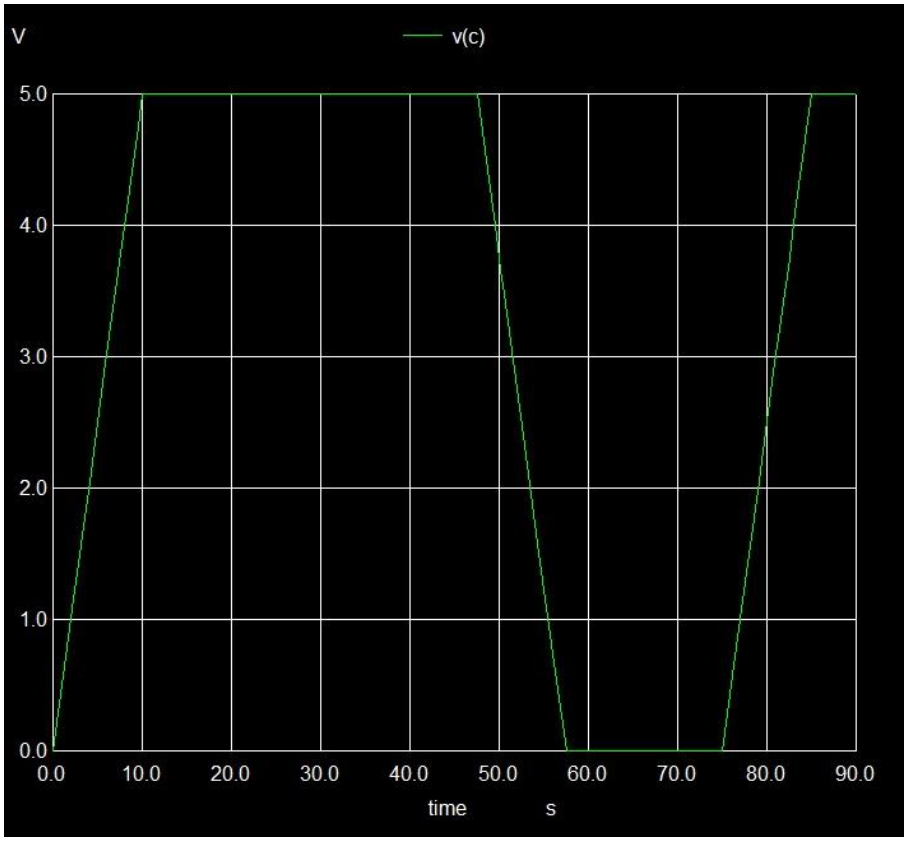


Figure 3- Graph of Vin (C)

Simulated Plots from NG Spice – Outputs

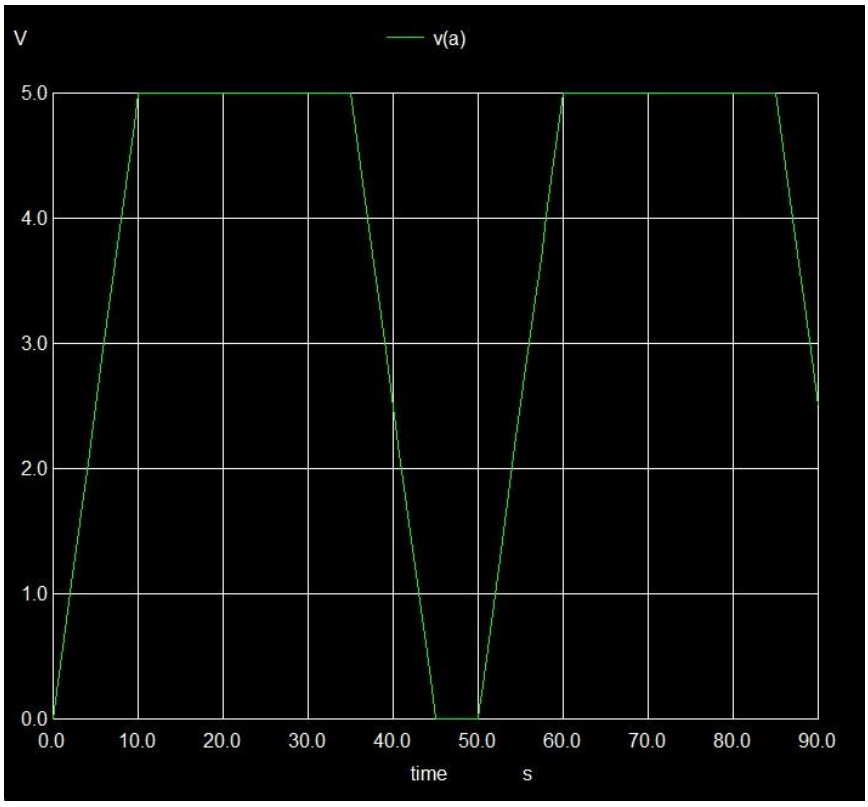


Figure 4 - Graph of Output P = A

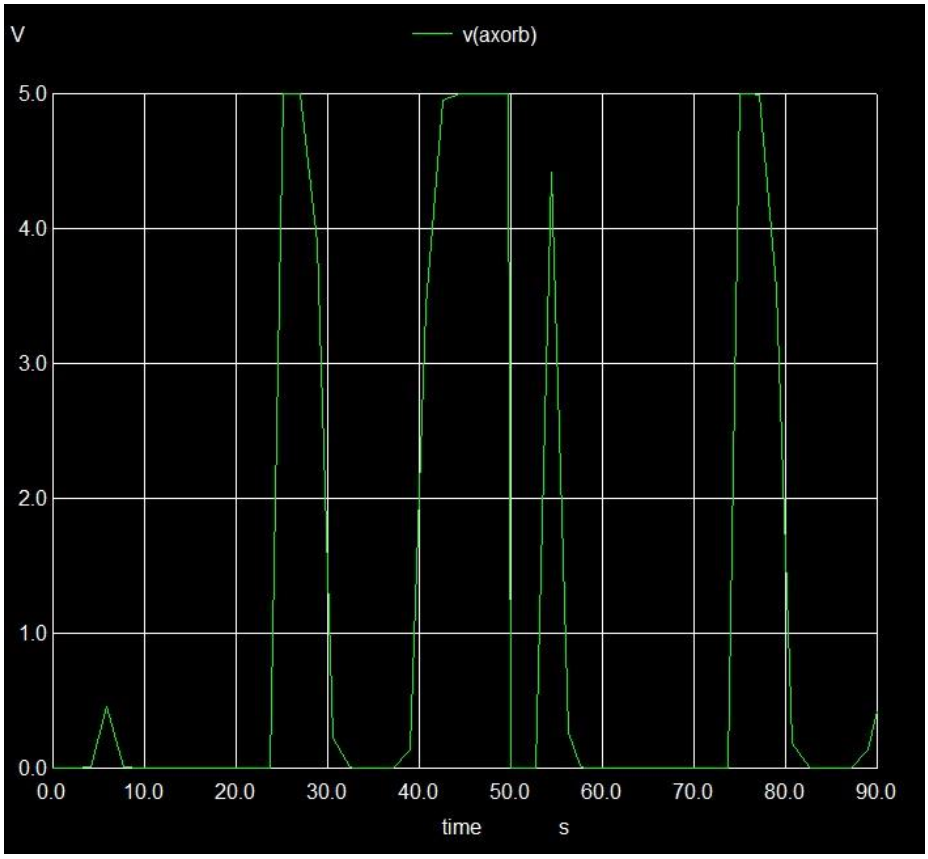


Figure 5 - Graph of Output Q = A XOR B

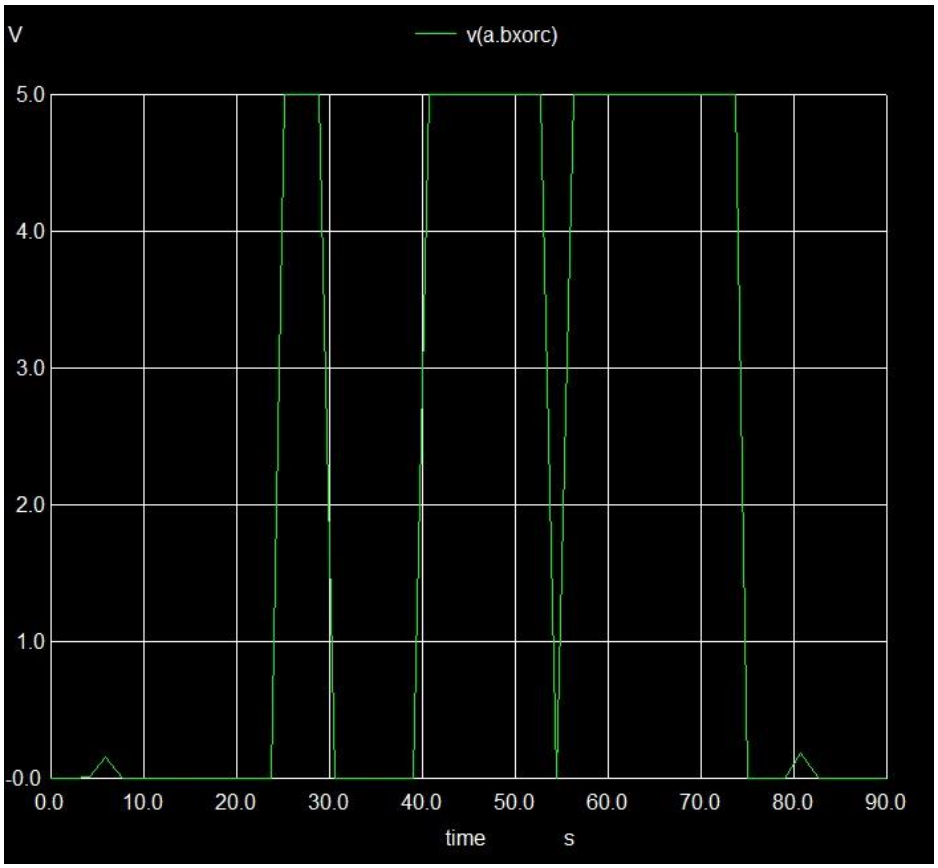


Figure 6 - Graph of Output R = (A.B) XOR C

Simulation Parameters:

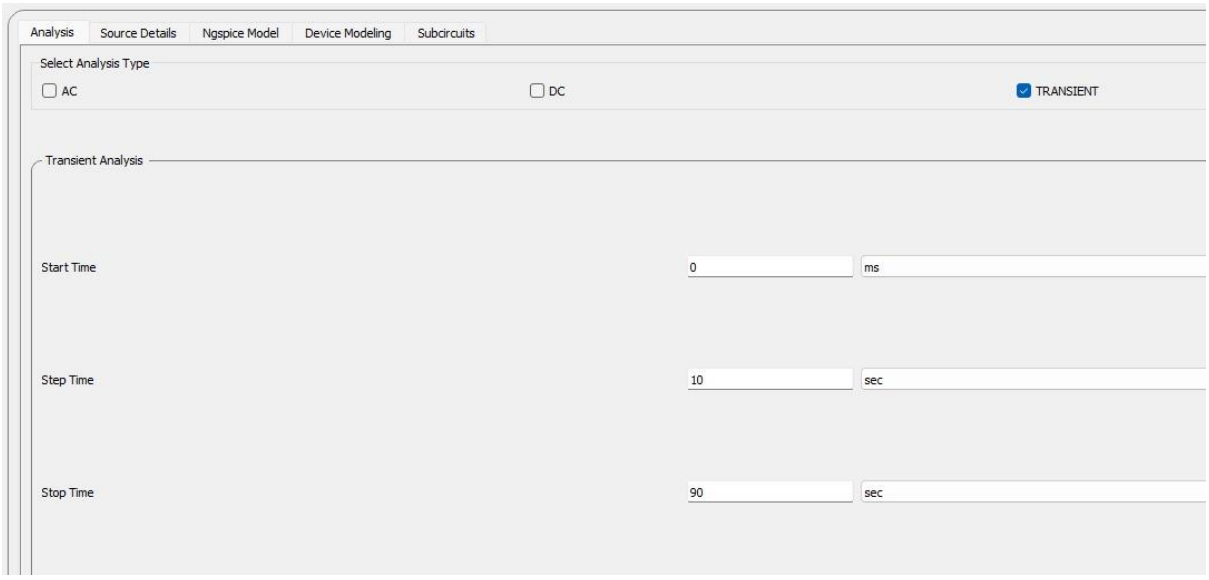


Figure 7 - Simulation Parameters for Transient Analysis

Figure 8 - Voltage Level Inputs

- The MOSFETs chosen were of 5um technology, and they were set at their default parameters –
- Length – 100u
- Width -100u
- Multiplicative Factor - 1

Observations and Conclusions:

From the obtained graphs, we can conclude that the above circuit performs the logic function of a 3x3 Reversible Peres Quantum Gate. The existence of transients is due to various factors including –

1. Parasitic Capacitances in the system.
2. Hard Switching.
3. Non-linear behaviour of MOSFETs.

As we can notice in the above plots, when all three inputs are high from 0 to around 22s, the outputs are as follows-

1. **P = A = 1**
2. **Q= A XOR B = 1 XOR 1 = 0**
3. **R = (A.B) XOR C = (1.1) XOR 1 = 1 XOR 1 = 0**

Hence this confirms the successful working of the circuit.

References:

The following resources and references were used for the completion of the project –

[1] Thapliyal, Himanshu & Ranganathan, N. (2010). Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs. JETC. 6. 14. 10.1145/1877745.1877748.

[2] Chanderkanta, Nan-Kuang Chen, Brajesh Kumar Kaushik, Santosh Kumar, Implementation of reversible Peres gate using electro-optic effect inside lithium-niobate-based Mach-Zehnder interferometers, Optics & Laser Technology, Volume 117, 2019,

[3] Lukac, Martin & Perkowski, Marek & Goi, Hilton & Pivtoraiko, Mikhail & Yu, Chung & Chung, Kyusik & Jeech, Hyunkoo & Kim, Byung-Guk & Kim, Yong. (2003). Evolutionary Approach to Quantum and Reversible Circuits Synthesis. Artif. Intell. Rev.. 20. 361-417. 10.1023/B:AIRE.0000006605.86111.79.