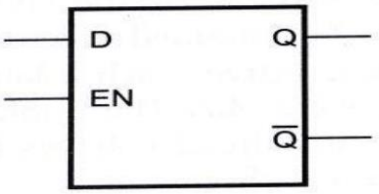
CIRCUIT SIMULATION PROJECT

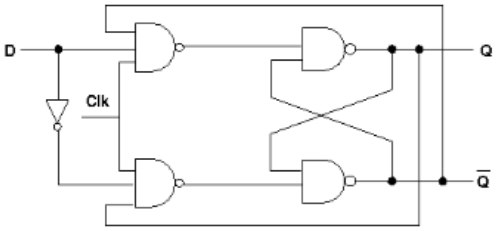
- **Name of the participant:** Abul Hasan
- **Name of the institution:** Aliah University

- **Title Of the Project:** Implementation of Delay flip flop using JK Flip Flop on 180nm CMOS Technology

Theory: - Flip-flops or the information stockpiling components are right around a fundamental part of each consecutive hardware



Logic symbol



Circuit Diagram

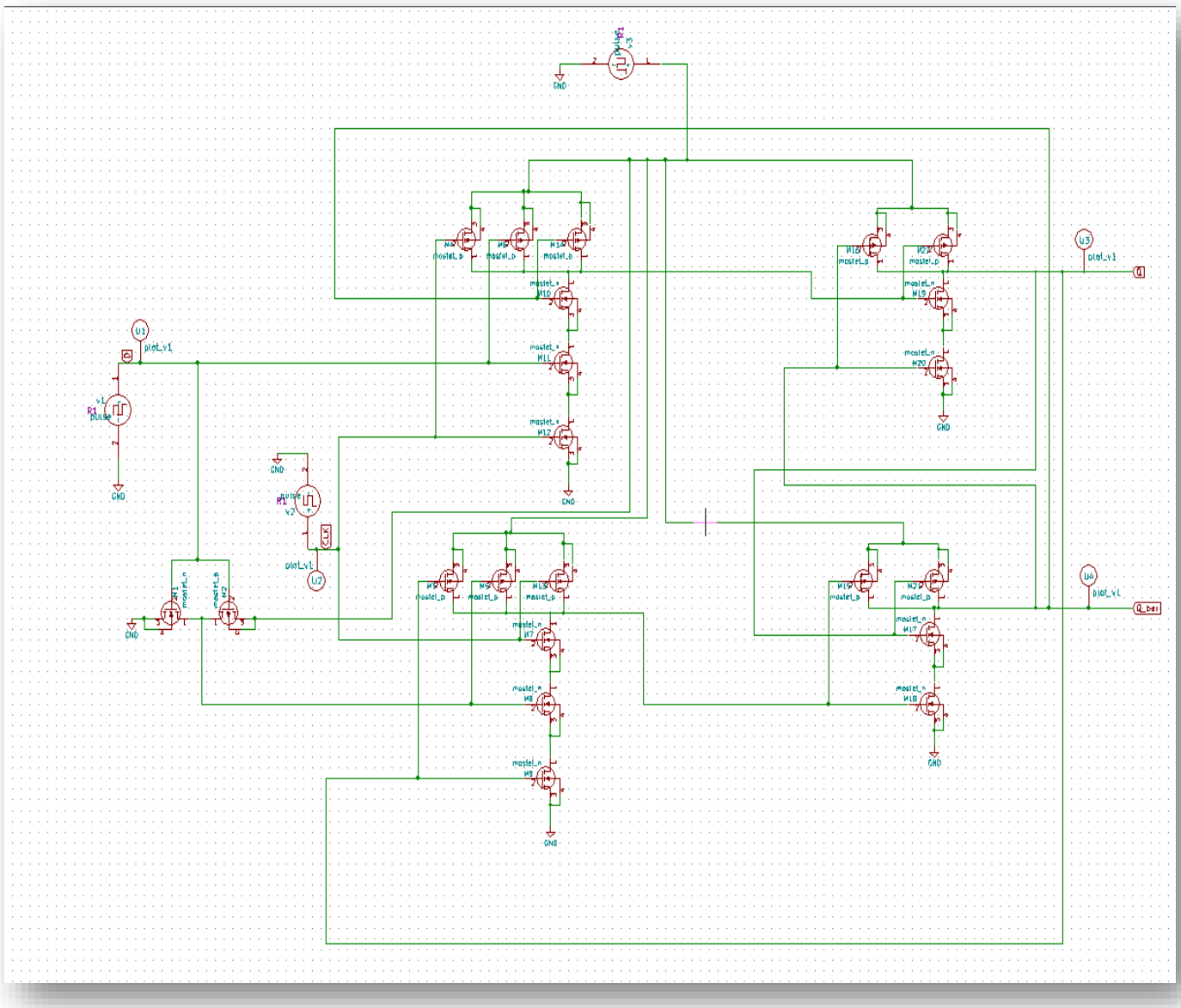
- Among different flip-flops, D flip-flop is regularly utilized. It catches the worth of the D contribution at a specific predefined piece of the clock beat (rising or falling edge of the clock) and its result isn't impacted at different pieces of the clock. According to the timing point of view, postpone created by flipflops consumes a huge piece of the process duration while the working recurrence increments. Throughout the course of recent many years CMOS innovation have gone under uncommon scaling with the perspective on mix thickness, fast and low power dispersal. By and by, a few additional obstacles have come into picture, which are more basic than prior. Changeability is one of them, characterized as the proportion of standard deviation (σ) to mean (μ) of any plan metric. These peculiarities have made semiconductors profoundly delicate to PVT (cycle, voltage and temperature) varieties. Planning a circuit of given details is incredibly troublesome.

Truth Table:-

EN	D	Qn	Qn+1	Stable
1	0	X	0	Reset
1	1	X	1	Set
0	X	X	Qn	No change (NC)

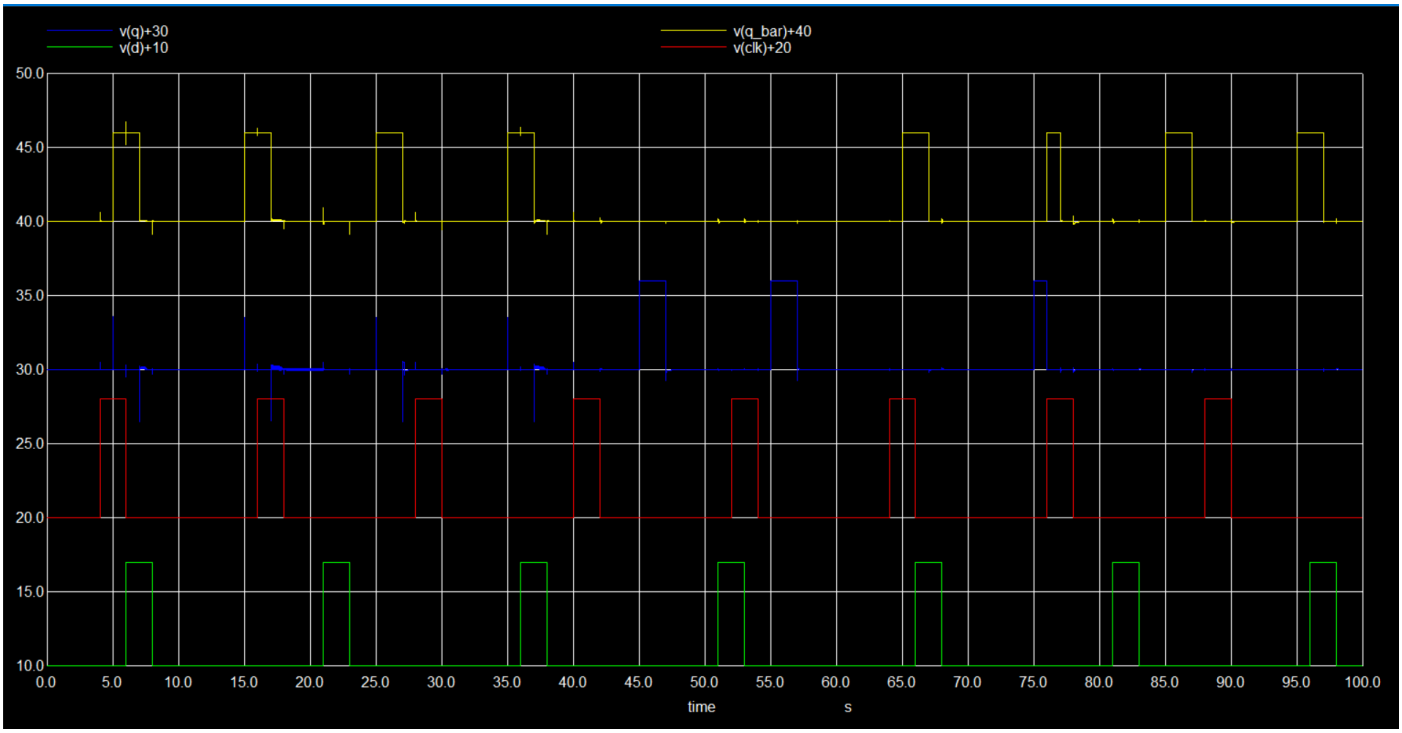
- D flip-flop is a key component in sequential logic circuits, playing a vital role in storing data, ensuring synchronization, and managing control in digital systems. Essentially, the D flip-flop acts as a memory unit, capable of holding a single bit of information. It consists of a data input (often referred to as D), a clock input (CLK), and an output (usually labeled as Q). The behavior of a D flip-flop is dictated by the clock signal. When the clock signal changes (either on the rising or falling edge, depending on the flip-flop's configuration), the D flip-flop captures the data present at its input (D) and stores it internally. This stored data is then reflected at the output (Q) until the next clock signal arrives."

SCHEMATIC DIAGRAM: -The schematic diagram of D Flip Flop in cMOS technology Using eSIM is shown below.

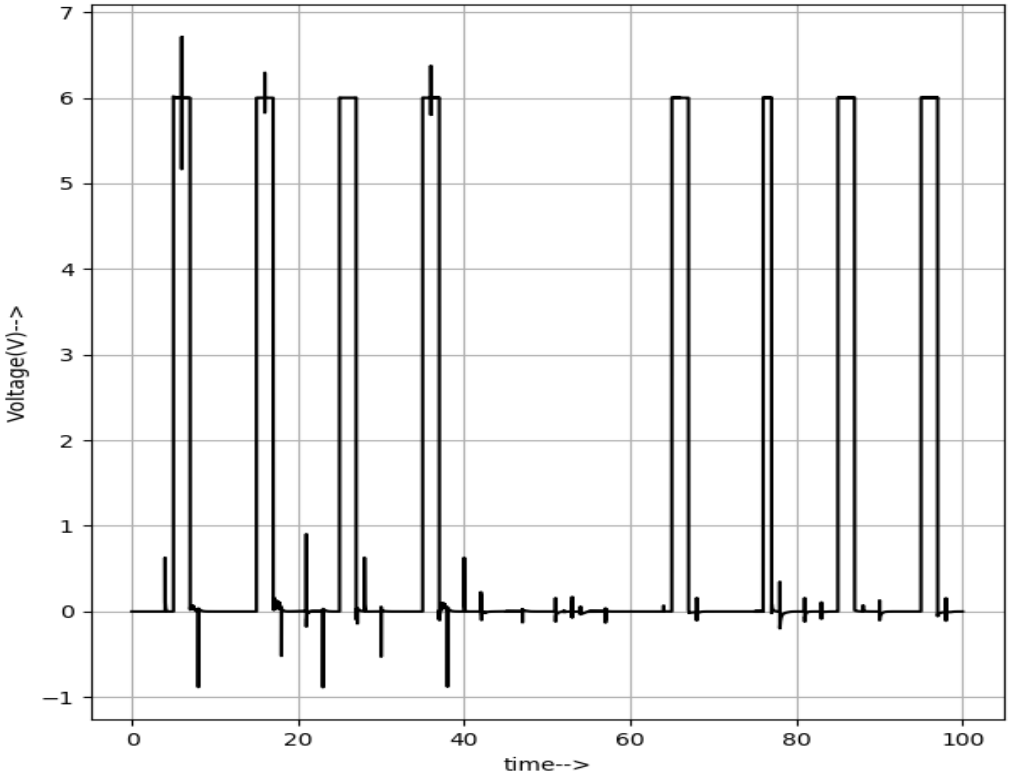


***SIMULATION RESULT*: -**

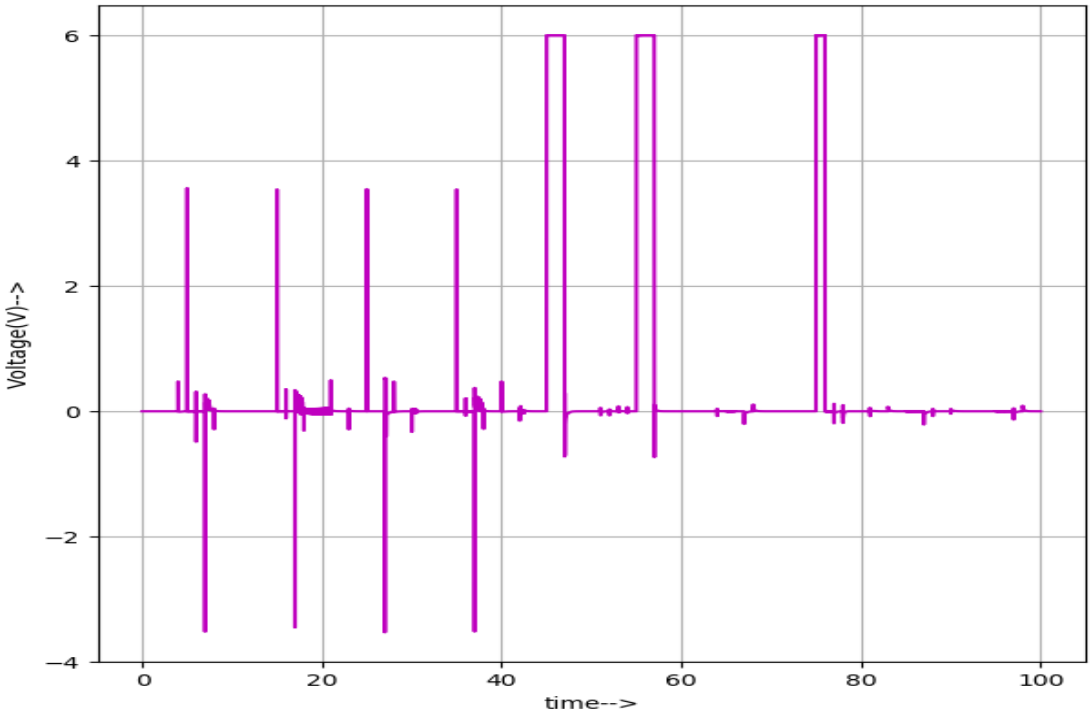
Ngspice plots: D- Flip Flop



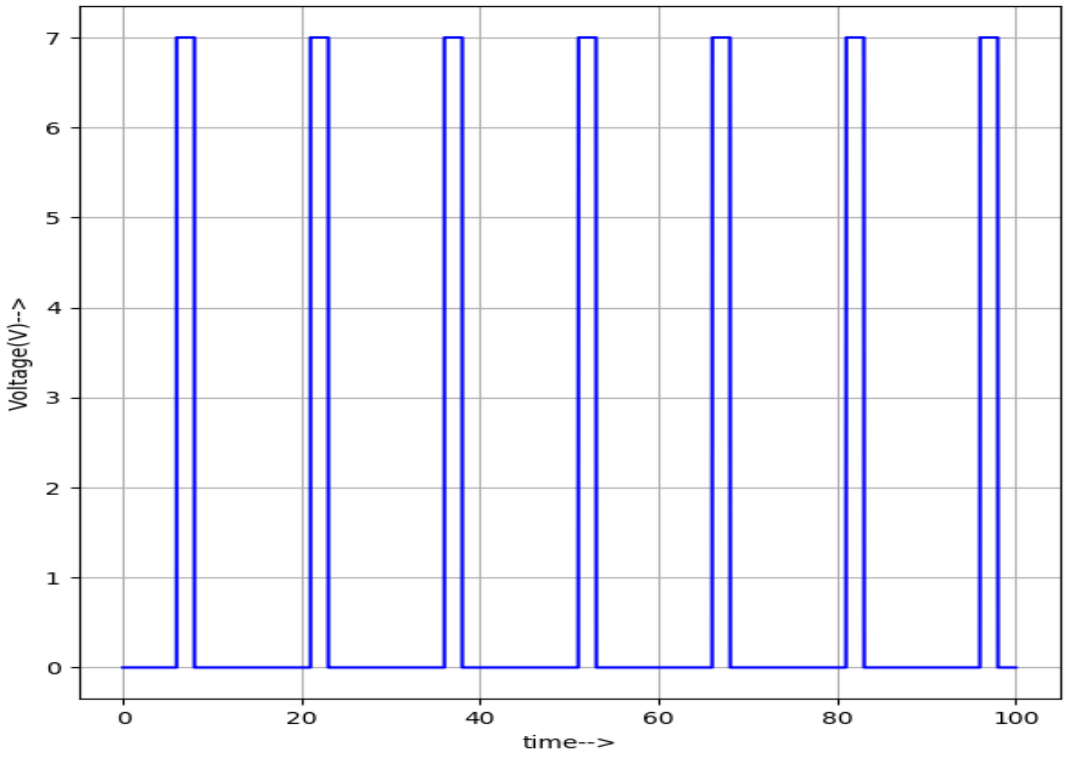
PYTHON PLOT:- D Flip Flop



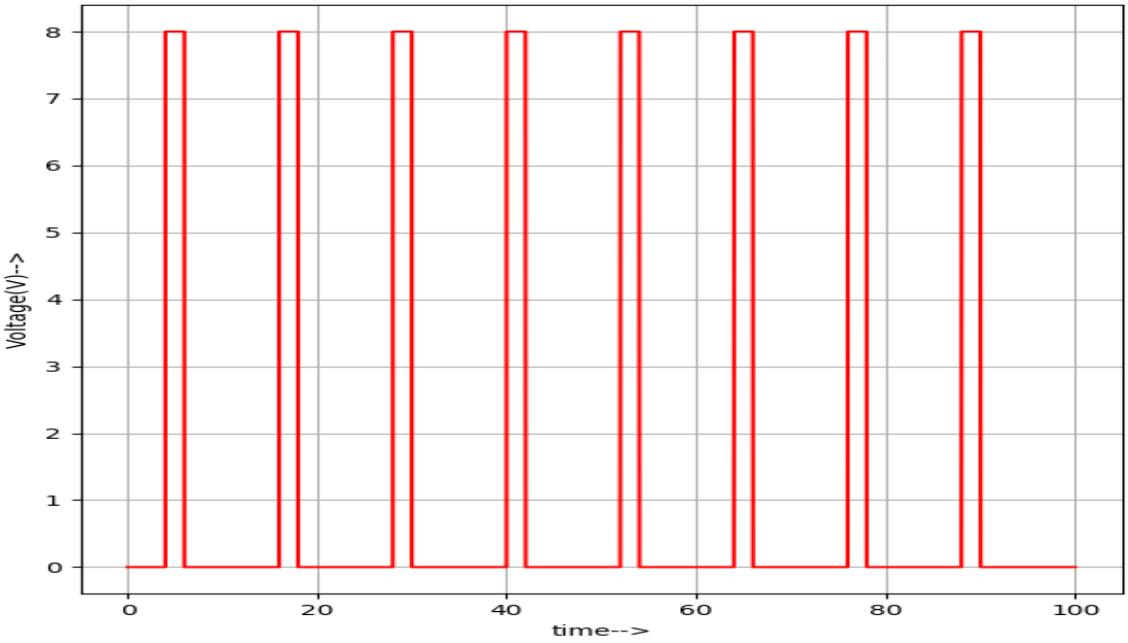
Python plot_Q_bar



PYTHON PLOT_Q

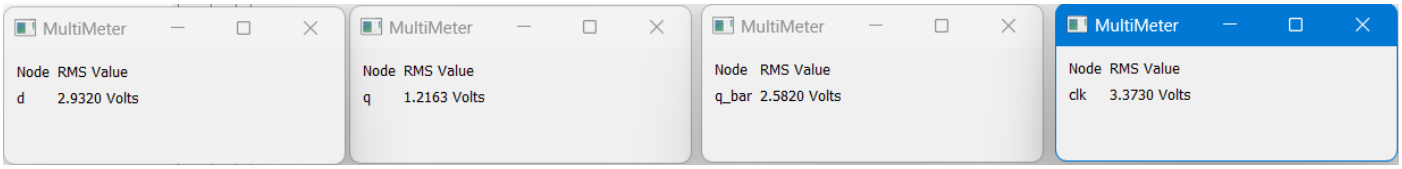


PYTHON PLOT_D



PYTHON PLOT_CLK

- **MULTIMETER VALUES:-**



Conclusion:- Thus,I have simulated the internal diagram of D flip flop Using JK Flip Flop by 180nm CMOS Technology by eSIM EDA Tool to get proper output & graph.

REFERENCES: -

- **Digital logic & computer design by M. MORRIS MANO**
- https://www.india.oup.com/productPage/5591038/7421214/9780199488681
- https://www.india.oup.com/productPage/5591038/7421214/9780199488681'