# CIRCUIT SIMULATION PROJECT

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- **Title of the experiment:-** Implementation Of 3 Input NAND Gate Using Transistor Transistor Logic.

- **Theory:-**

  TTL as outlined above for transistor-transistor logic. It is a logic family implemented with bipolar process technology that combines or integrates NPN transistors, PN junction diodes, and diffused resistors in a single monolithic structure to get the desired logic function. The NAND gate is the basic building block of this logic family.

  The given figure- a shows the internal schematic of a standard TTL NAND gate. The circuit operation is as follows:

  Transistor $T_1$ is a three-emitter NPN transistor, equivalent to three NPN transistors with their base and emitter terminals tied together. The three emitters are the three inputs of the NAND gate.

### ❖ Circuit Operation:-

When the three inputs are in the logic HIGH state as specified by the TTL family ($V_{IH}$ = 2V minimum), the current flows through the base-collector PN junction diode of transistor $T_1$ into the base of transistor $T_2$. Transistor $T_2$ is turned ON to saturation, with the result that transistor $T_3$ is switched OFF and transistor $T_4$ is switched ON. This produces a logic LOW at the output.

When either one of the three inputs or two inputs or all inputs are in the logic LOW state, the base-emitter region of $T_1$ conducts current, driving $T_2$ to cut off in the process. When $T_2$ is in the cut-off state, $T_3$ is driven to conduction and $T_4$ to cut-off. This produces a logic HIGH output.

### ❖ Totem-Pole Output Stage:-

Transistors $T_3$ and $T_4$ constitute what is known as a totem-pole output arrangement. In such an arrangement, either $T_3$ or $T_4$ conducts at a time depending upon the logic status of inputs. The totem-pole arrangement at the output has certain distinct advantages. The major advantage of using a totem-pole connection is that it offers low-output impedance in both HIGH and LOW output states. In the HIGH state, $T_3$ acts as an emitter follower and has an output impedance of about 70Ω. In LOW state, $T_4$ is saturated and the output can be charged rapidly through this low impedance, thus allowing quick transitions at the output from one stage to another.

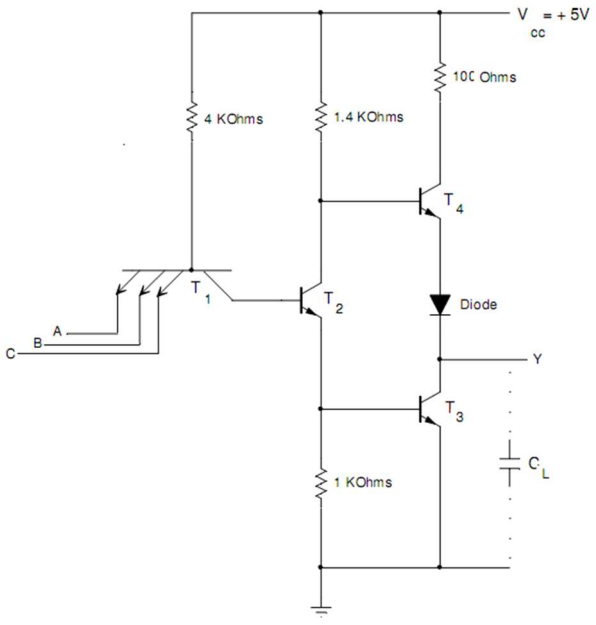



Figure- a: 3 Input TTL NAND gate

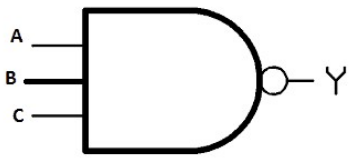


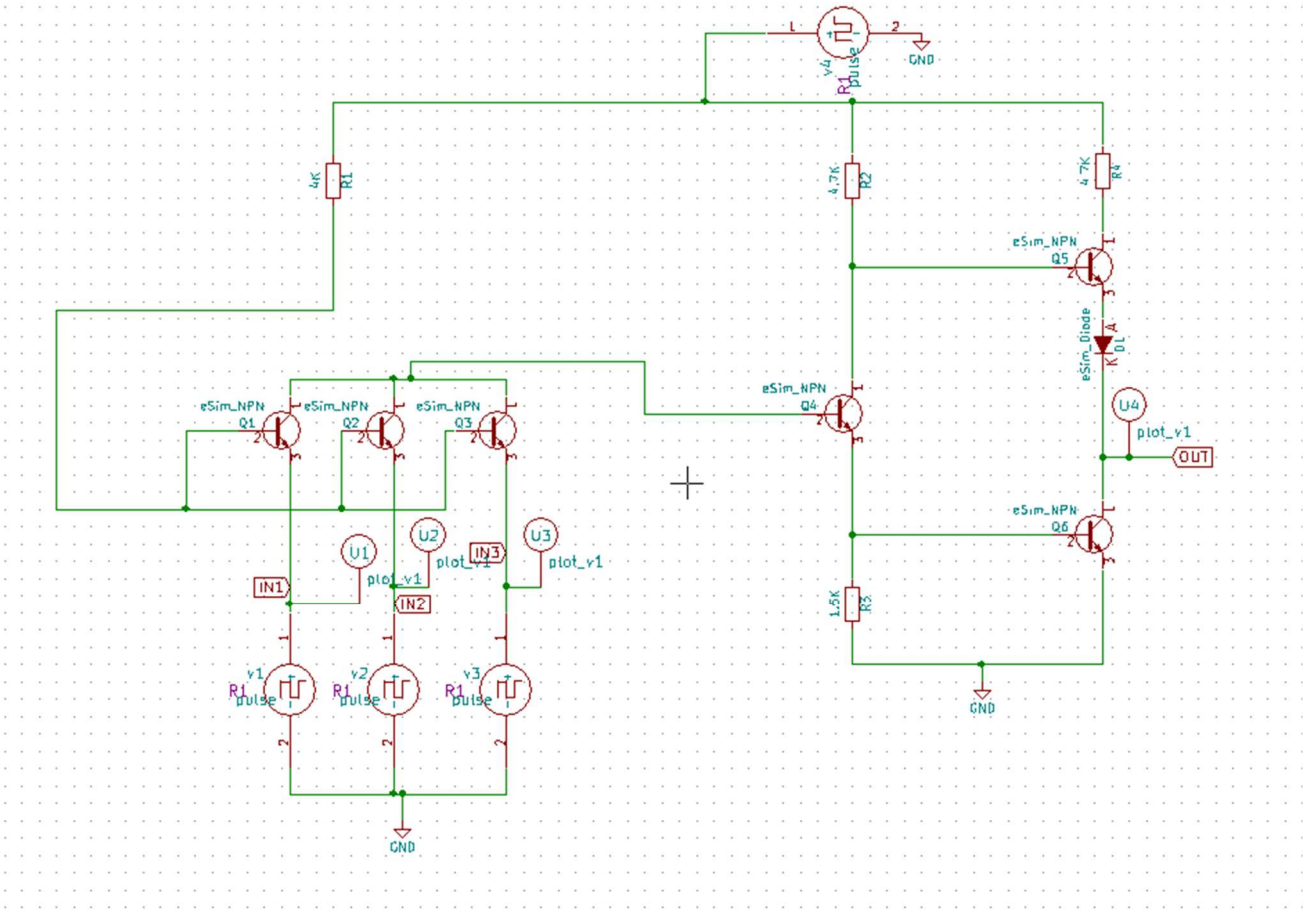

Figure- c: NAND gate

| Input | | | Output |
|---|---|---|---|
| A | B | C | Y |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Figure- b: Truth table

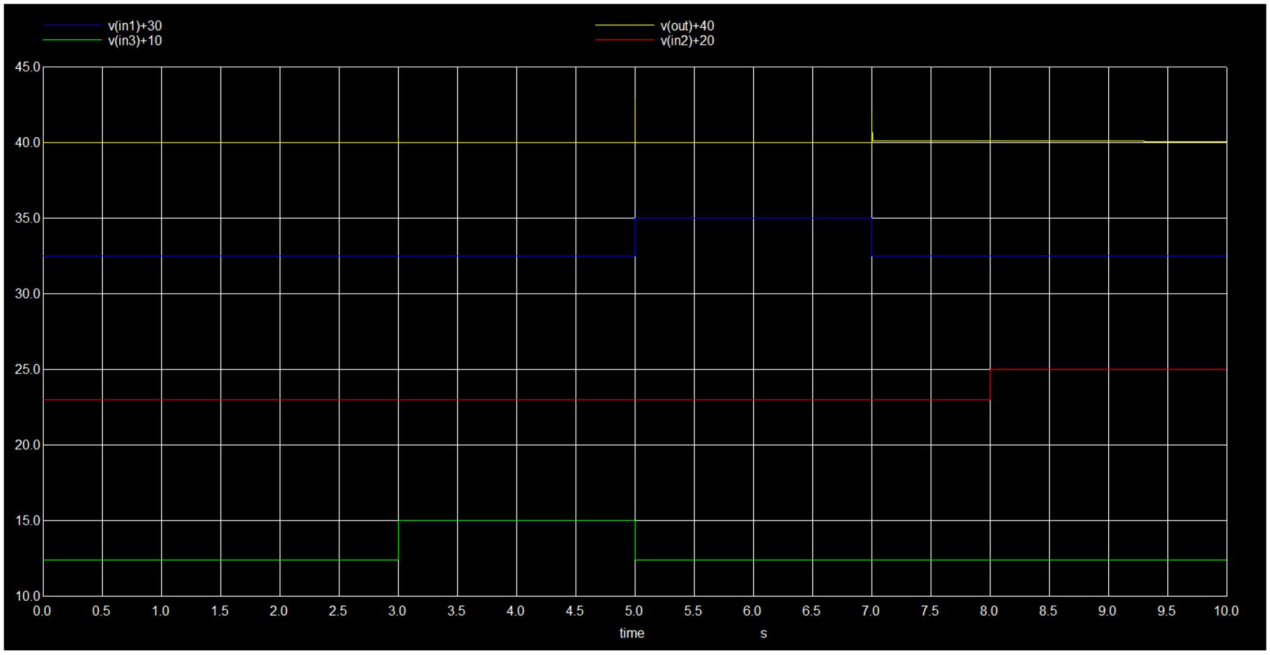
- **Schematic Diagram:**

  The circuit schematic of 3 Input NAND Gate Using Transistor Transistor Logic with totem pole output Logic in eSim is as shown below:-

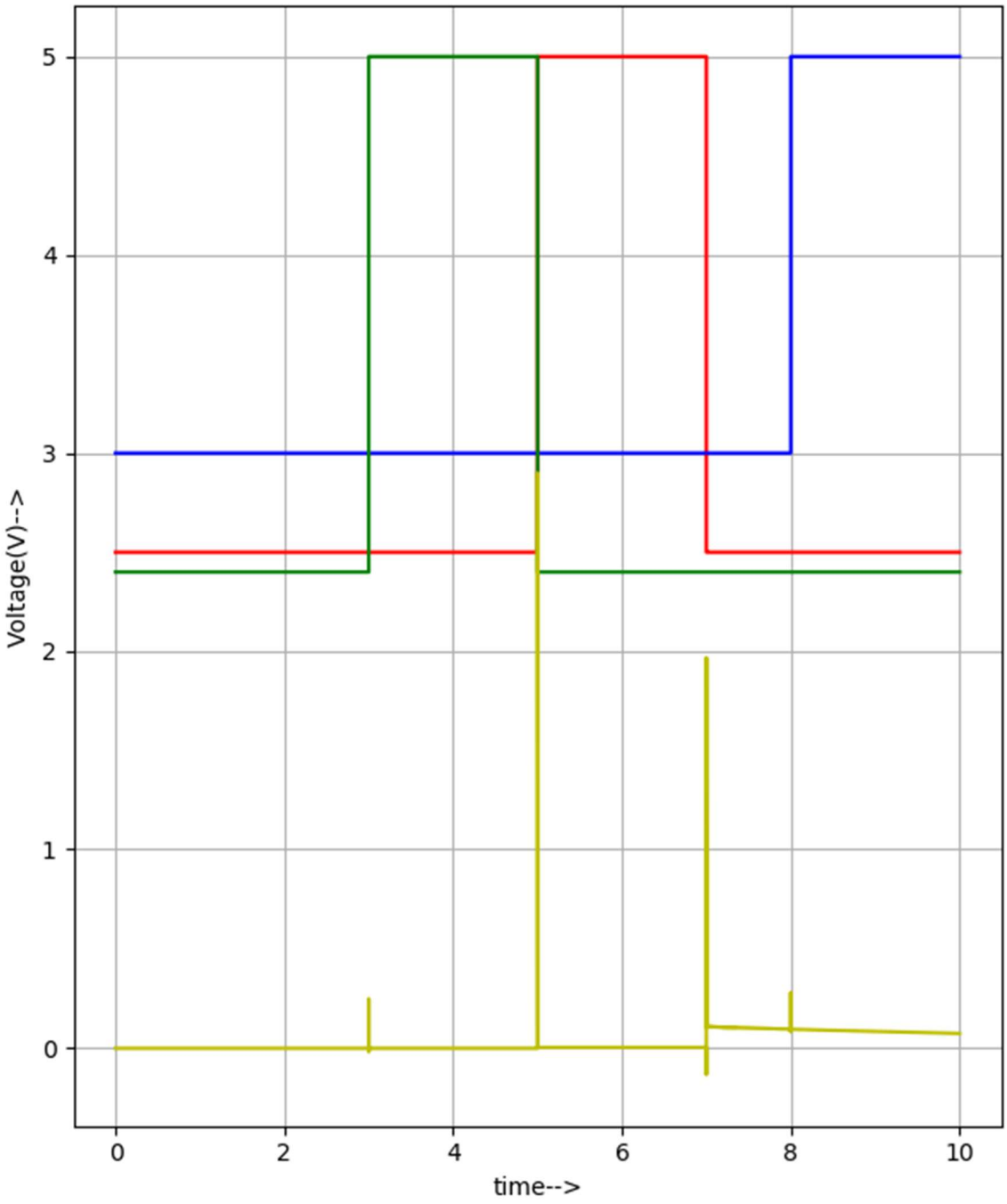



- **<u>Simulation Results:</u>**

  **Ngspice Plots :**



**Python Plot:**




- **Conclusion :**
  TLT NAND gate utilizes a totem pole output structure with transistors T1-T4 and diode D to ensure high-speed transitions and low output impedance. Three conditions dictate its operation: when at least one input is low, all inputs are high, and transitioning from all high inputs to one low input. Through careful transistor arrangement and mode switching, the gate effectively produces the desired output states of high and low.
- **References:-**
  Digital Electronics Principles and Integrated Circuits by Anil K. Maini
  https://www.expertsmind.com/questions/explain-a-ttl-nand-gate-and-its-operation-30161619.aspx
  https://www.elprocus.com/transistor-transistor-logic-ttl/