CIRCUIT SIMULATION PROJECT

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<u>Title of the experiment</u>:- Design And Implementation of Mixed-Signal BCD to 7-Segment Decoder using Verilog.

<u>Theory:-</u>

In **Binary Coded Decimal (BCD)** encoding scheme each of the decimal numbers(0-9) is represented by its equivalent binary pattern(which is generally of 4-bits).

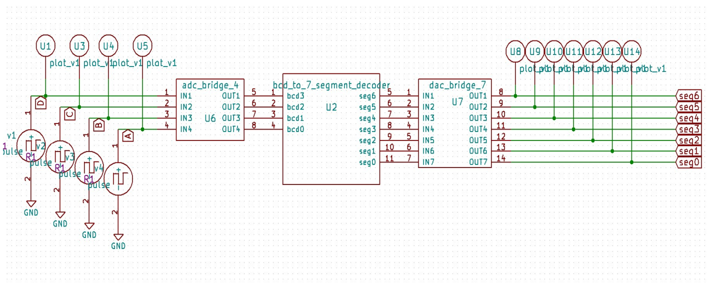
Whereas, **Seven segment** display is an electronic device which consists of seven Light Emitting Diodes (LEDs) arranged in a some definite pattern (common cathode or common anode type), which is used to display Hexadecimal numerals(in this case decimal numbers, as input is BCD i.e., 0-9).

But, seven segment display does not work by directly supplying voltage to different segments of LEDs. First, our decimal number is changed to its BCD equivalent signal then BCD to seven segment decoder converts that signals to the form which is fed to seven segment display.

This BCD to seven segment decoder has four input lines (A, B, C and D) and 7 output lines (a, b, c, d, e, f and g), this output is given to seven segment LED display which displays the decimal number depending upon inputs.

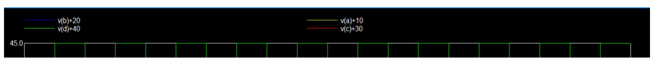
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

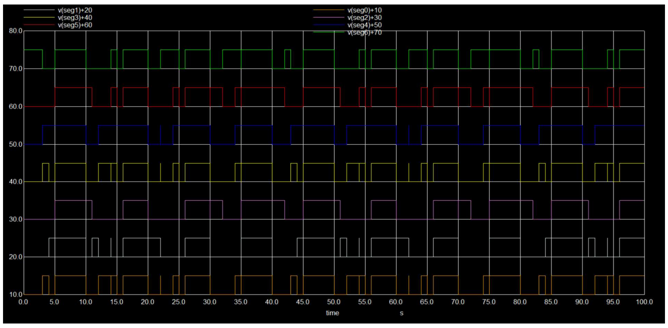
<u>Schematic Diagram:-</u>

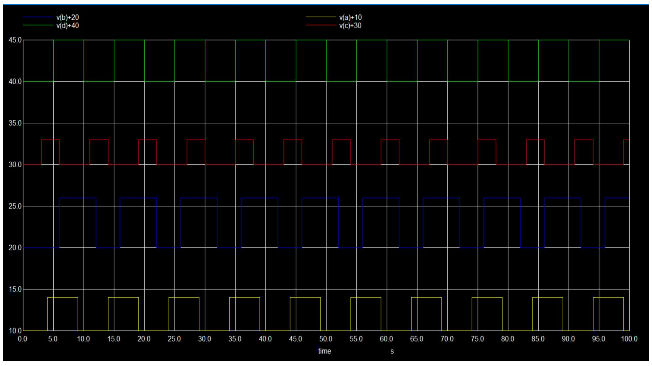


<u>Simulation Results:-</u>

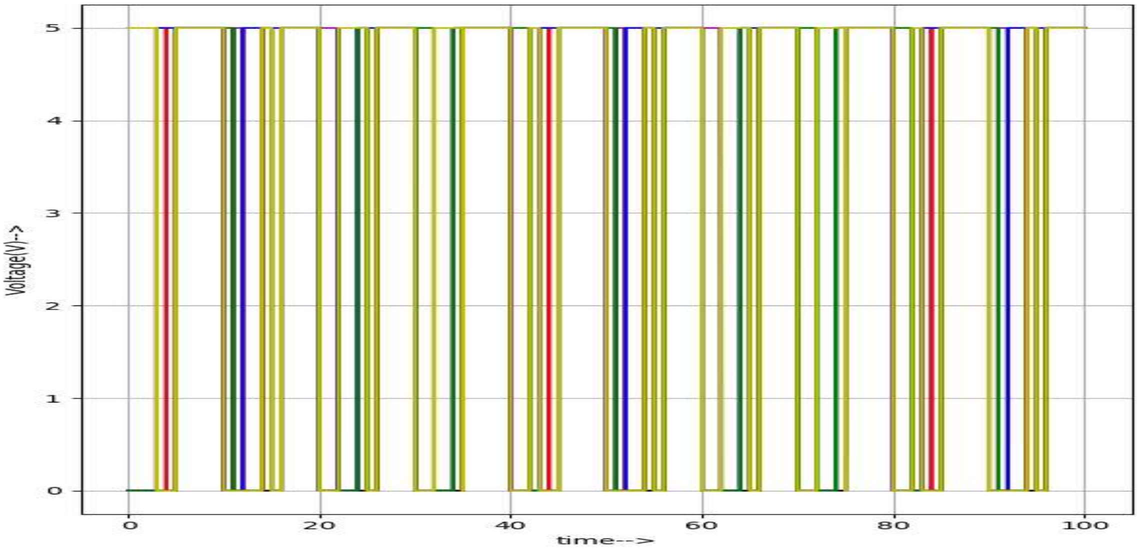
- *<u>NgSpice plot:</u>*

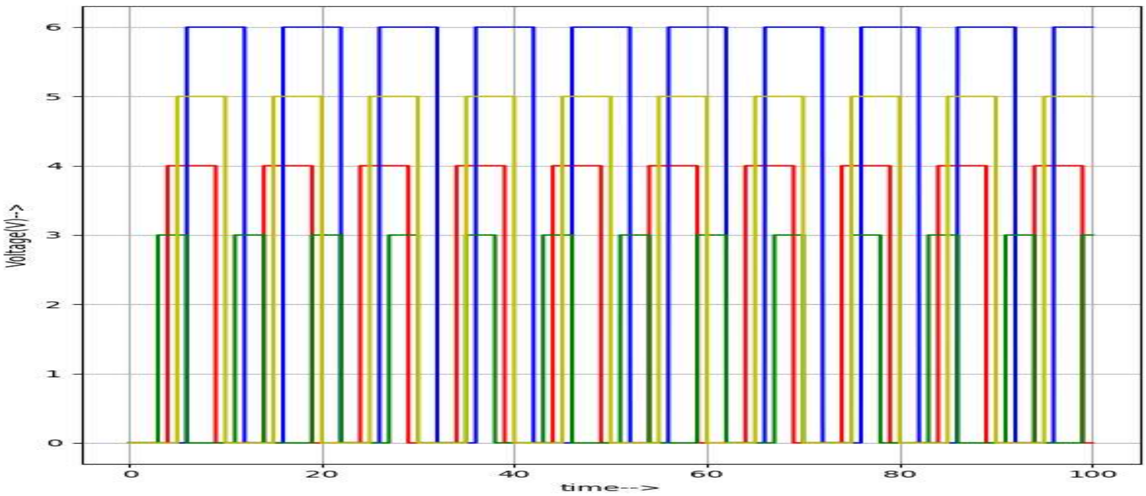






- <u>Python plot:</u>





Verilog program:

```
module BCD_to_7_Segment_decoder(
   input [3:0] bcd,     // 4-bit BCD input signal
   output reg [6:0] seg // 7-segment display output signal
);
always @ (bcd) begin
      case(bcd)
         4'b0000: seg = 7'b1000000;
         4'b0001: seg = 7'b1111001;
         4'b0010: seg = 7'b0100100;
```

```
        4'b0011: seg = 7'b0110000;
        4'b0100: seg = 7'b0011001;
        4'b0101: seg = 7'b0010010;
        4'b0110: seg = 7'b0000010;
        4'b0111: seg = 7'b1111000;
        4'b1000: seg = 7'b0000000;
        4'b1001: seg = 7'b0010000;
        default: seg = 7'b1111111;
     endcase
   end
endmodule
```

Conclusion :-

Thus, we have studied and Implement a Mixed-Signal BCD to 7-Segment Decoder using Verilog.on eSim Circuit Simulation software and we get the appropriate waveform.

Reference :

BCD to 7 Segment Decoder - GeeksforGeeks
How to Build a 7-Segment Display Circuit | Electrical4U
Verilog Coding Tips and Tricks: Verilog code for BCD to 7-segment display converter (verilogcodes.blogspot.com)