CIRCUIT SIMULATON PROJECT

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Title of the experiment:-

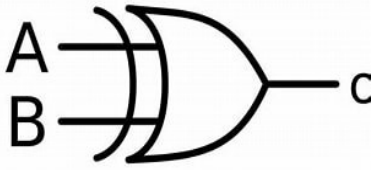
Implementation Of 2 Input Exclusive-OR Gate Using Emitter Coupled Logic

Theory:-

XOR gate is also known as the Exclusive OR gate or Ex-OR gate. It gives the output 1 (High) if an odd number of inputs is high. This can be understood in the Truth Table. It can have an infinite number of inputs and only one output. In most cases, two-input or three-input XOR gates are used. Here I implement two input XOR Gate.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table of XOR Gate

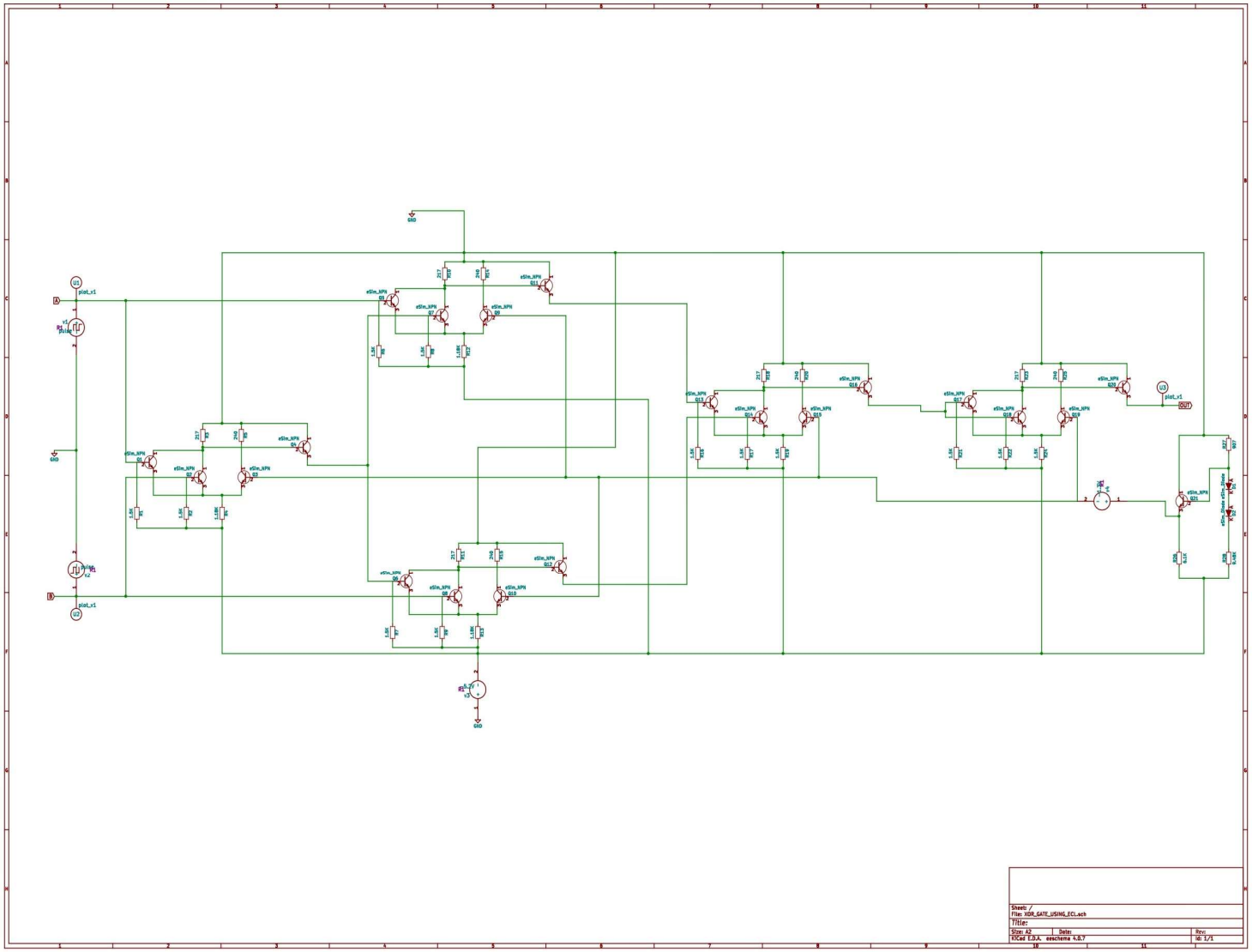


Exclusive-OR Gate

Emitter-coupled logic (ECL) is a non-saturated digital logic family. Since transistors do not saturate, it is possible to achieve propagation delays of 2 ns and even below 1ns. This logic family has the lowest propagation delay of any family and is used mostly in systems requiring very-high speed operation. A XOR circuit of the ECL family is shown in Schematic Diagram. The main outputs provide XOR functions. Each input is connected to the base of a transistor. The two voltage levels are about −0.8 V for the high state and about −1.8 V for the low state. The circuit consists of differential amplifier, a temperature- and voltage-compensated bias network, and emitter-follower output.

Schematic Diagram:-

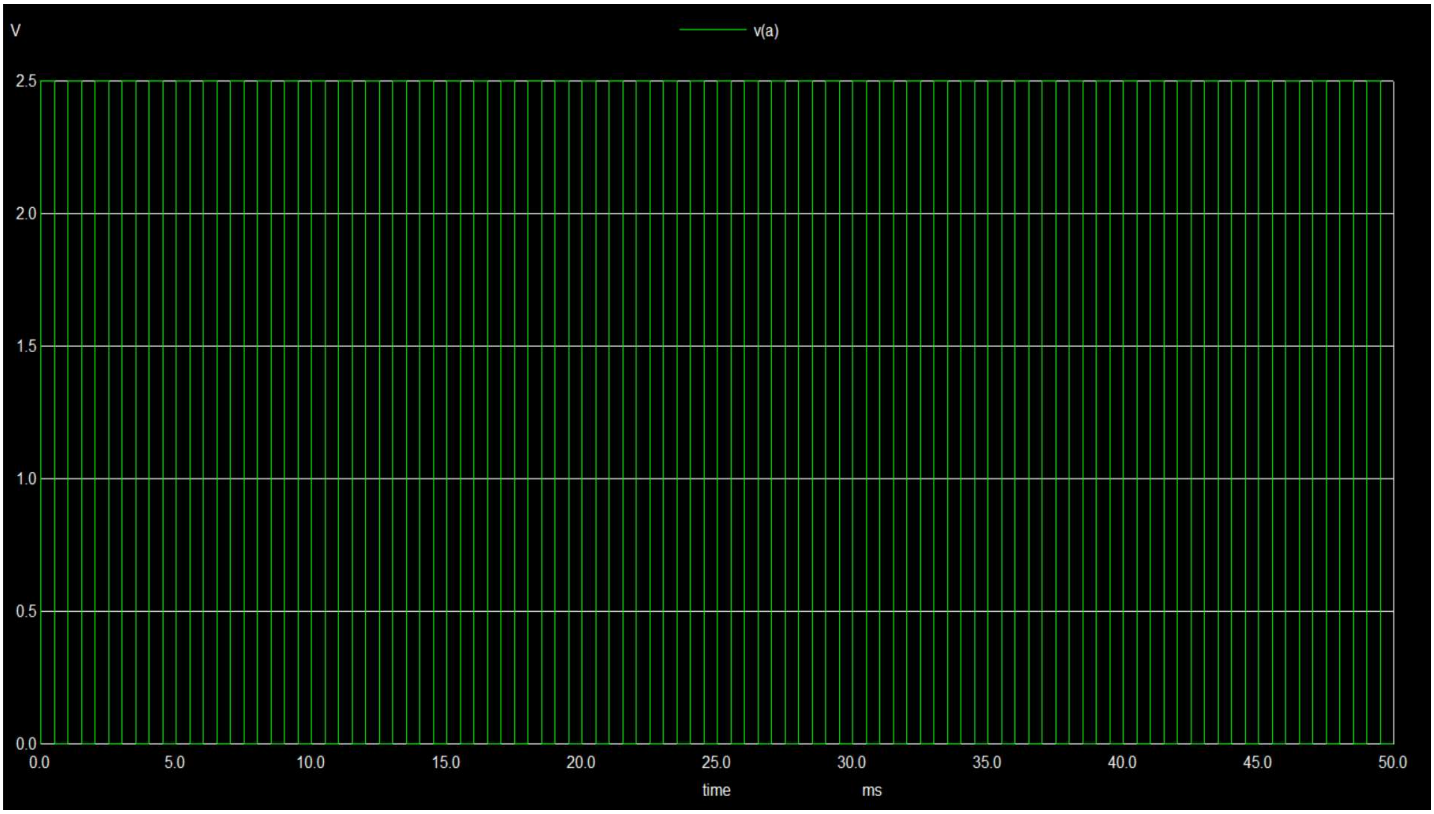
The circuit schematic of 2 Input Exclusive-Or Gate Using Emitter Coupled Logic in eSim is as shown below:



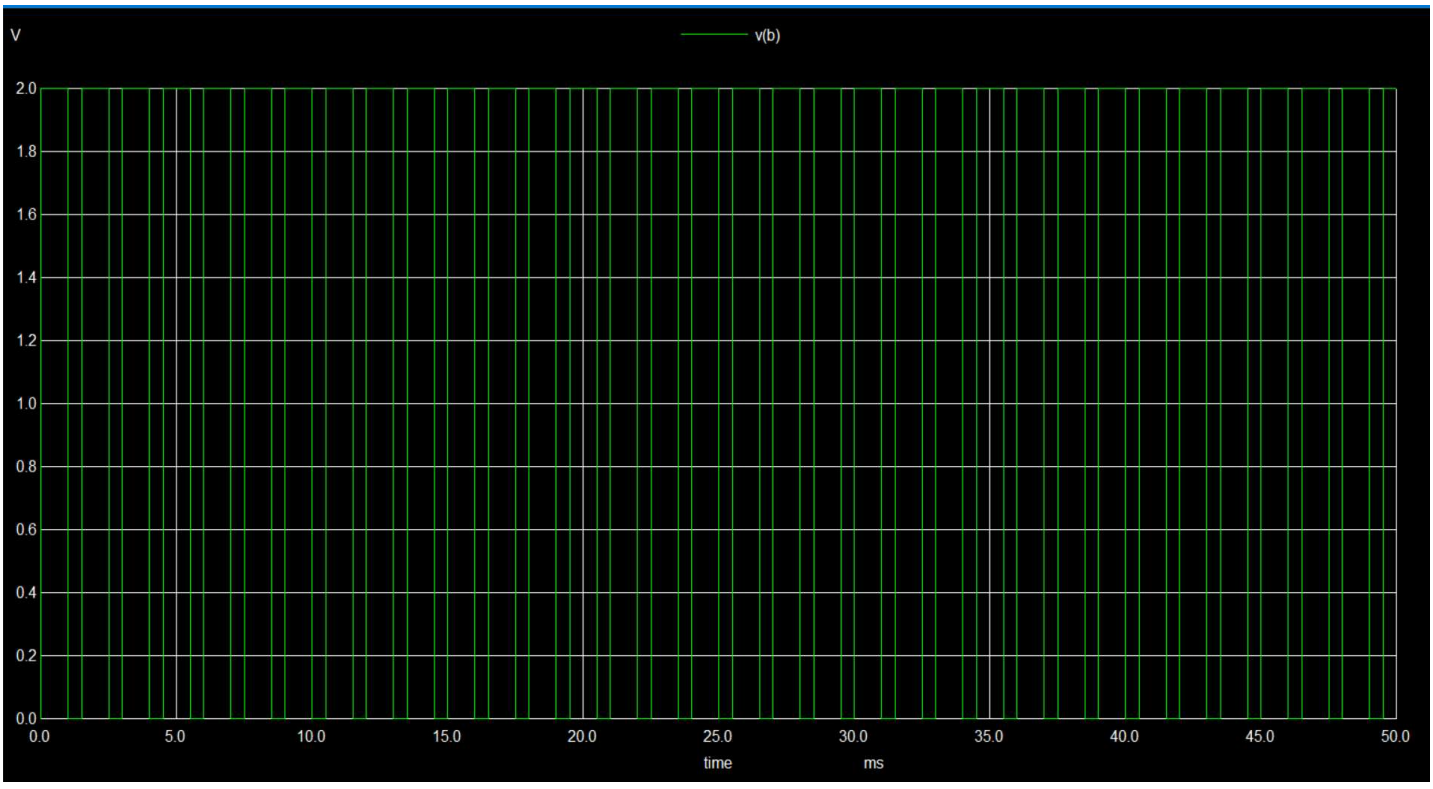
Exclusive-OR Gate using ECL logic

Simulation Results:-

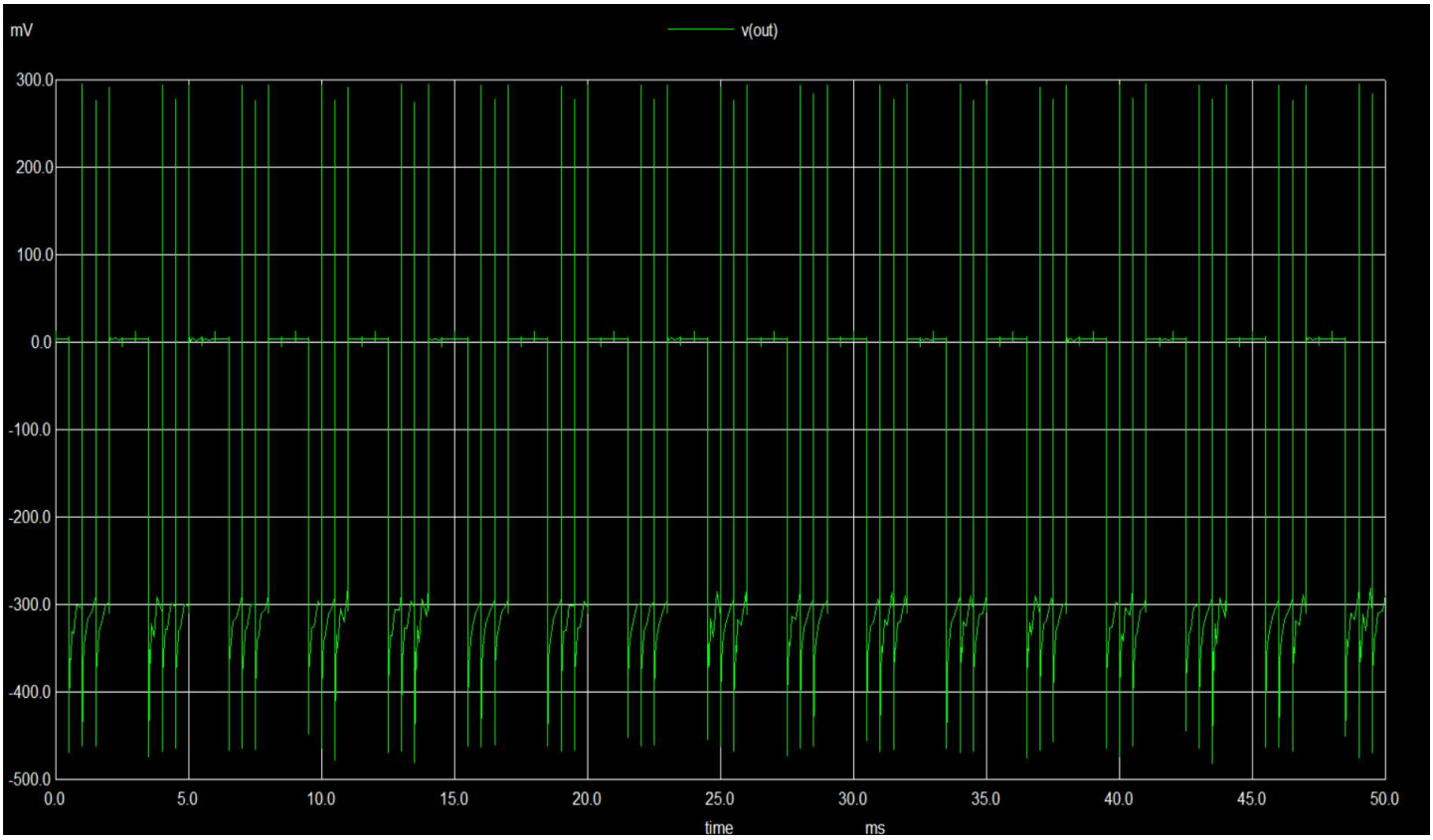
- ***Ngspice Plots :***



Ngspice Input-1 Plot



Ngspice Input-2 Plot

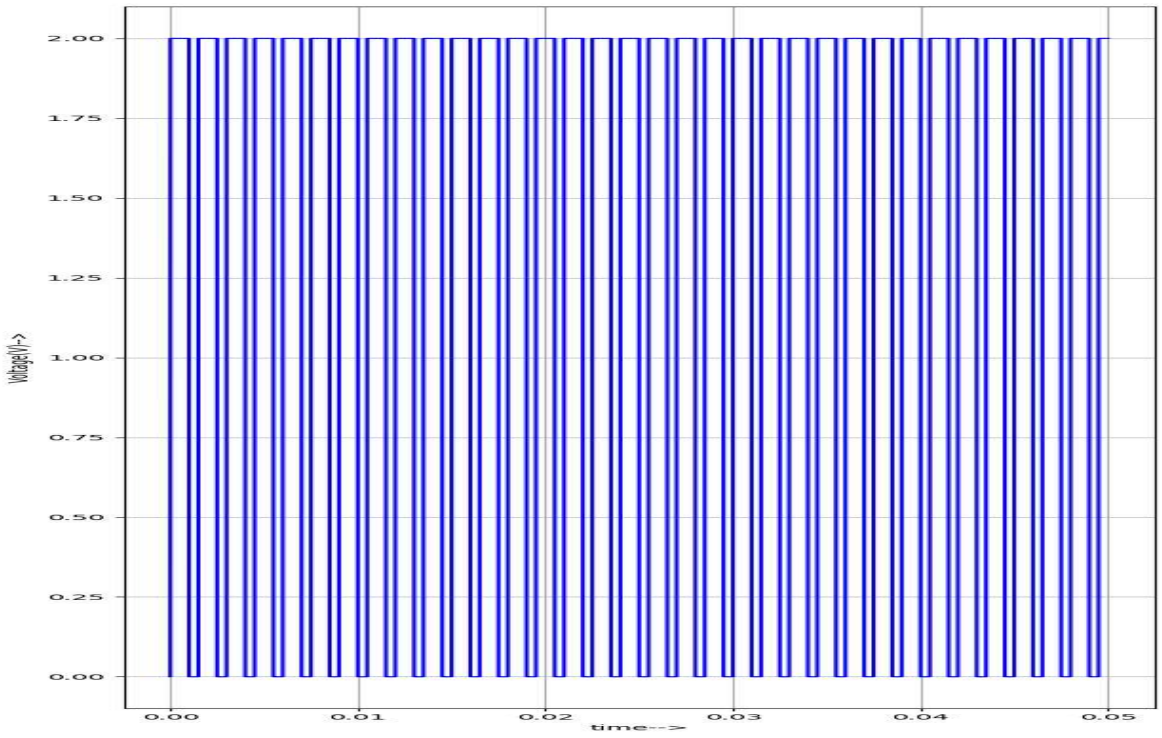


Ngspice Output Plot

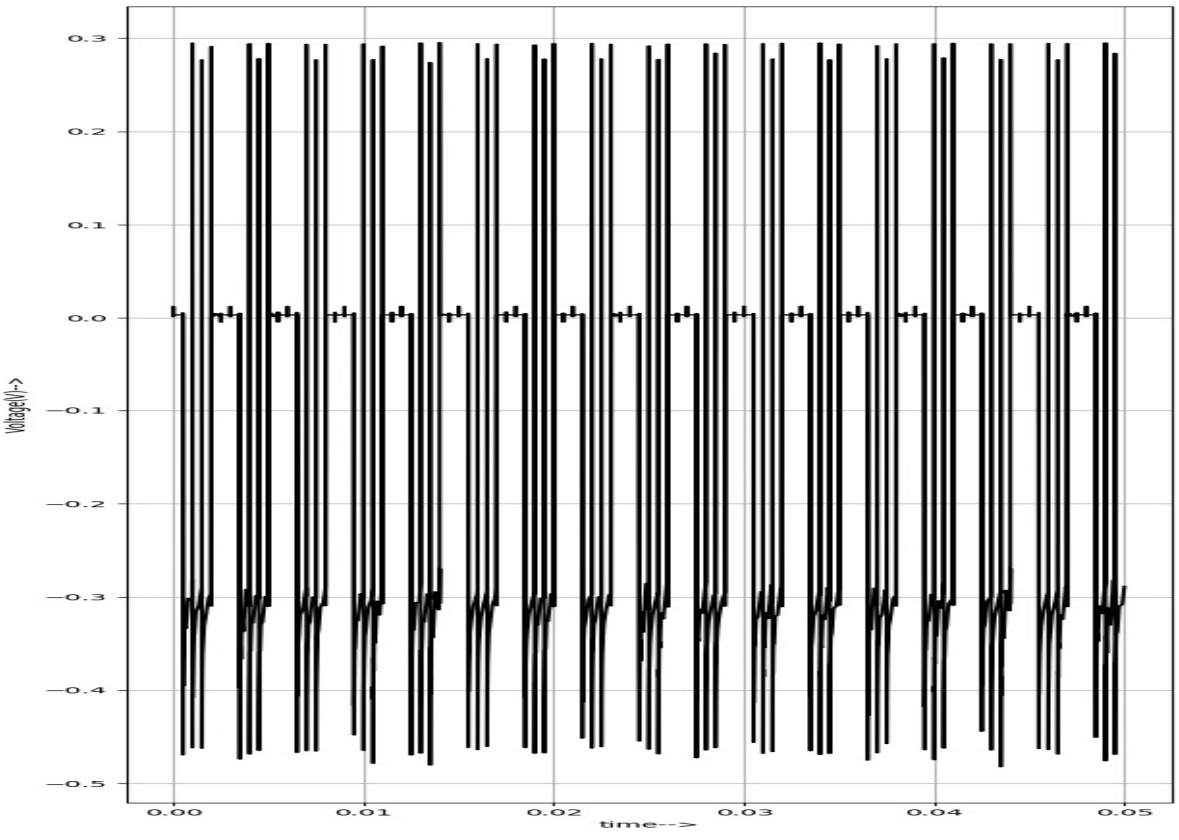
- **Python Plot:**

Python Plot Input-1

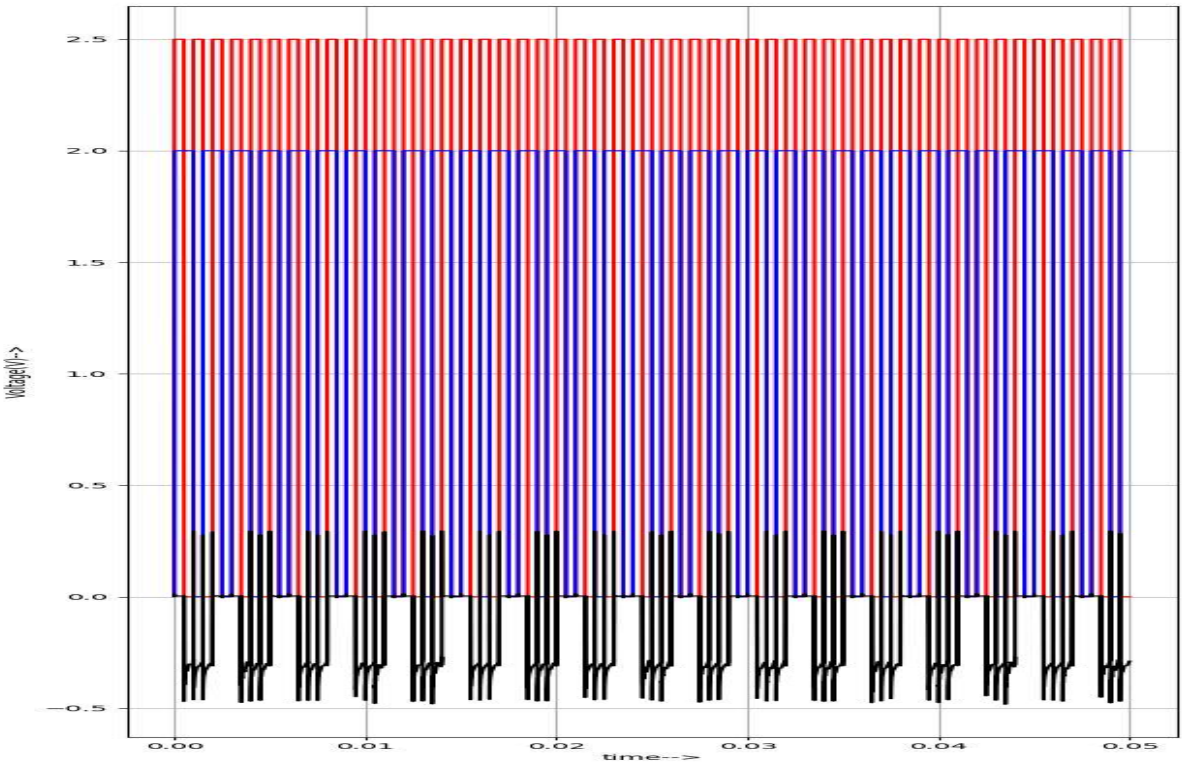
Python Plot Input-1



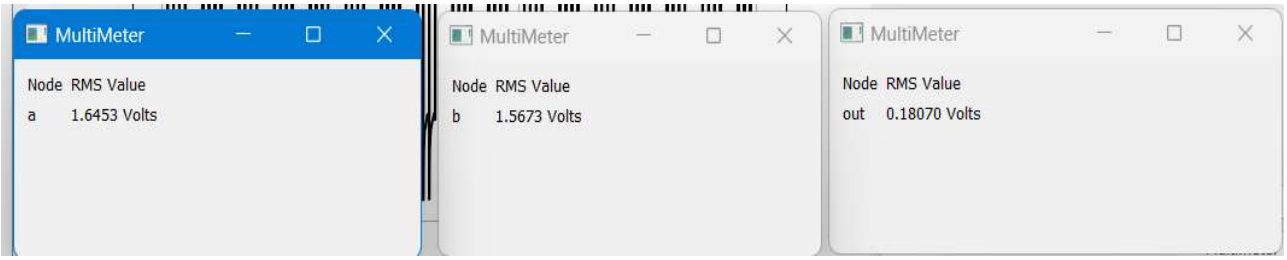
Python Plot Input-2



Python Plot Output



Python Plot of XOR Gate



Conclusion :-

Thus, we have studied the Implementation Of two Input Exclusive-OR Gate Using Emitter Coupled Logic using eSim and we get the appropriate waveform.

References :-

- Digital Logic and Computer Design by M. MORRIS MANO
- https://faculty-web.msoe.edu/johnsontimoj/CE3101/files3101/emitter_coupled_logic_implementation.pdf
- https://www.geeksforgeeks.org/emitter-coupled-logic/
- ECL NOR/OR GATE
- Lecture - 19 Quantitative analysis of ECL 10k Series gates