

# Circuit Simulation Project

<https://esim.fossee.in/circuit-simulation-project>

**Name of the Participant:** Abhinav Tripathi

**Title of the circuit:** Design of A Self-Starting (lock-Out Free) 4-Bit Johnson Counter

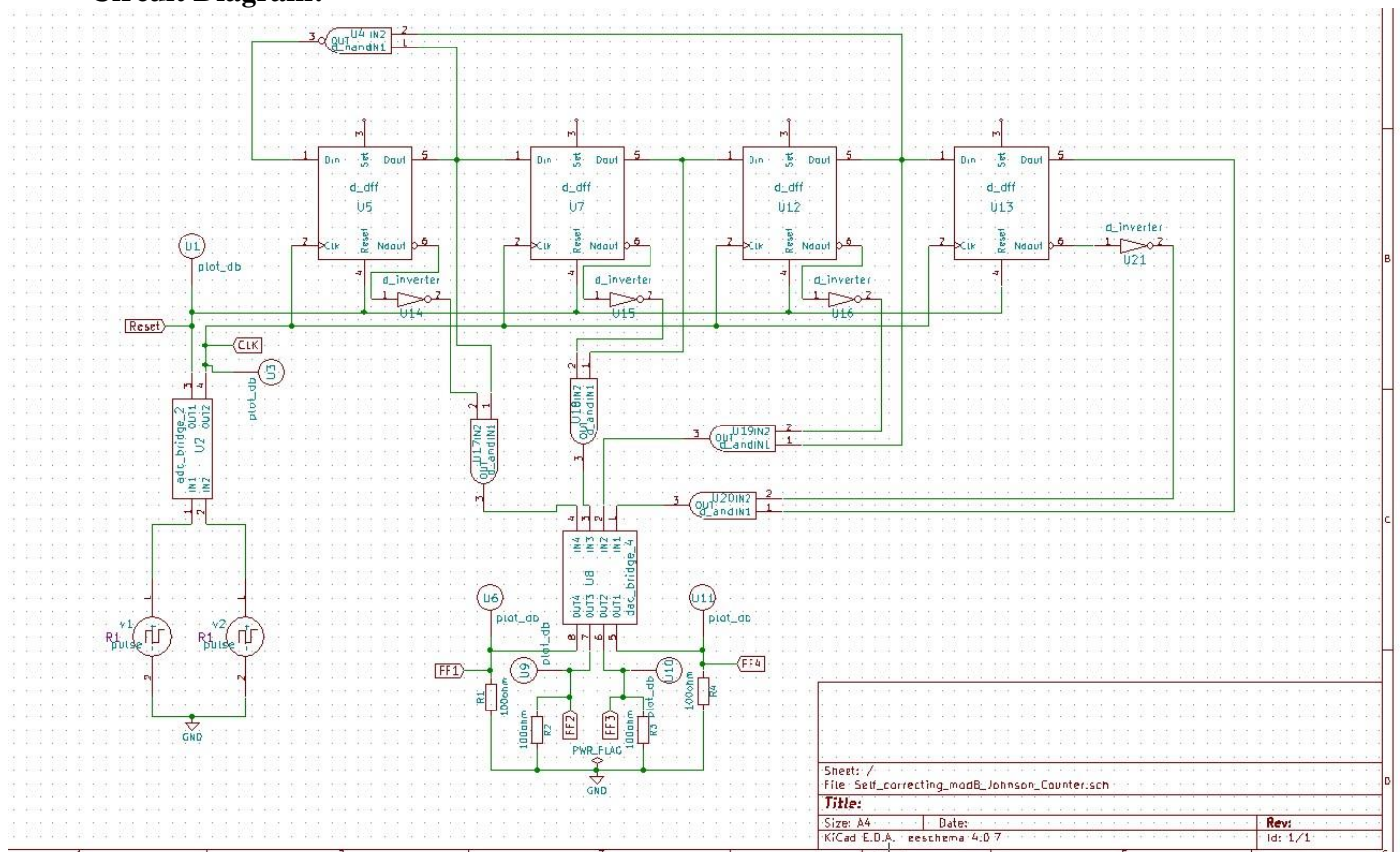
## Theory:

A Johnson counter, also known as a twisted ring counter or walking ring counter, is a shift register in which the complement of the output of the last register is given as the input of the first register and circulates a stream of ones followed by zeros around the ring. There is always a problem of lock-out in counters. We design Self-starting(self-correcting) Johnson Counters to overcome the lock-out problem. Some additional combinational circuitry is used to make the counters self-starting.

For example, after every clock cycle, the parallel output of the counter is as follows:0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000. But, for SELF-CORRECTING Johnson Counter output is different.

In this project, I have implemented a 4-bit self-correcting Johnson counter using 4 D flip-flops. The circuit is quite simple. There can be many ways to design a self-correcting Johnson Counter, here we have taken the Q2.Q0 to D0 and hence we prevent the lockout at the given state.

## Circuit Diagram:



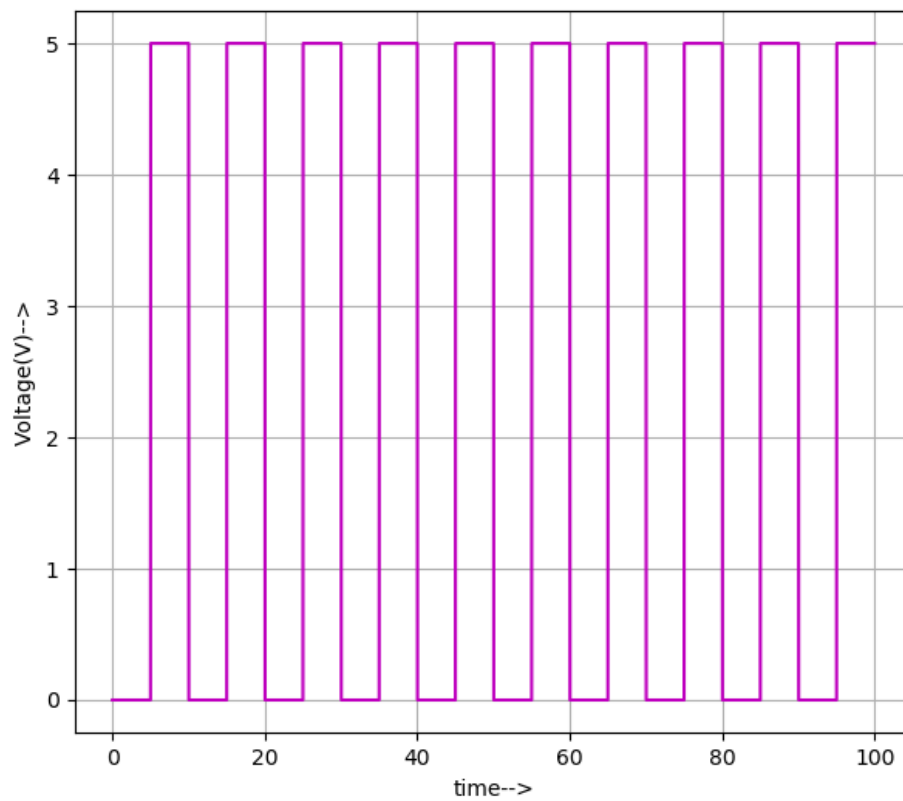
## Results:

Add parameters for pulse source v2	
Enter initial value (Volts/Amps):	0
Enter pulsed value (Volts/Amps):	5
Enter delay time (seconds):	5
Enter rise time (seconds):	0
Enter fall time (seconds):	0
Enter pulse width (seconds):	5
Enter period (seconds):	10

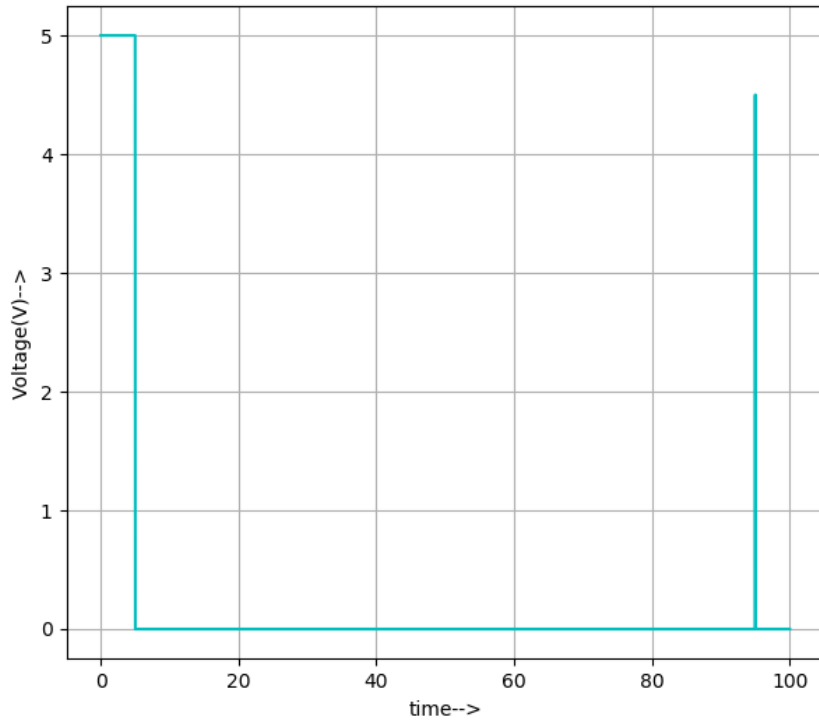
  

Add parameters for pulse source v1	
Enter initial value (Volts/Amps):	5
Enter pulsed value (Volts/Amps):	0
Enter delay time (seconds):	5
Enter rise time (seconds):	0
Enter fall time (seconds):	0
Enter pulse width (seconds):	0
Enter period (seconds):	90

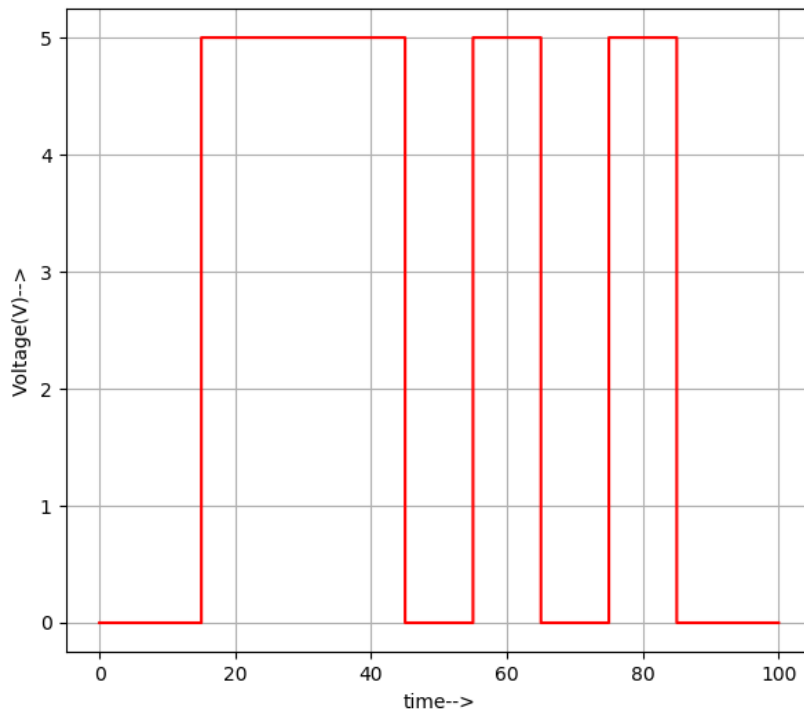
**Fig 1: Source Details**



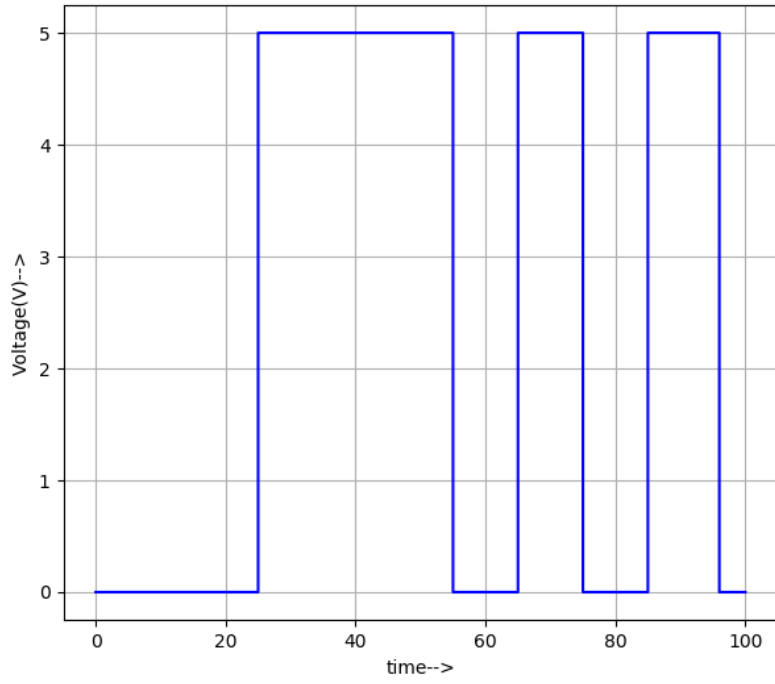
**Plot 1: Clock Signal**



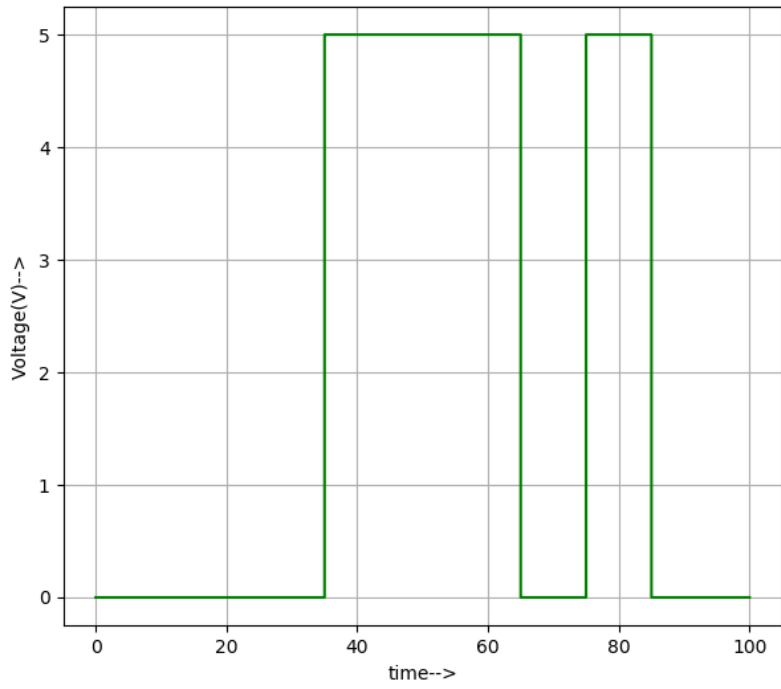
**Plot 2:** Orientation Signal



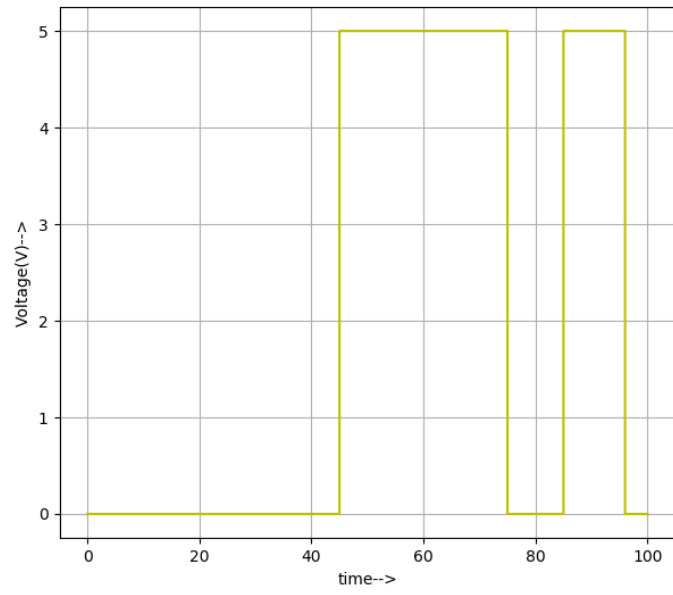
**Plot 3:** Output of Flip Flop 1



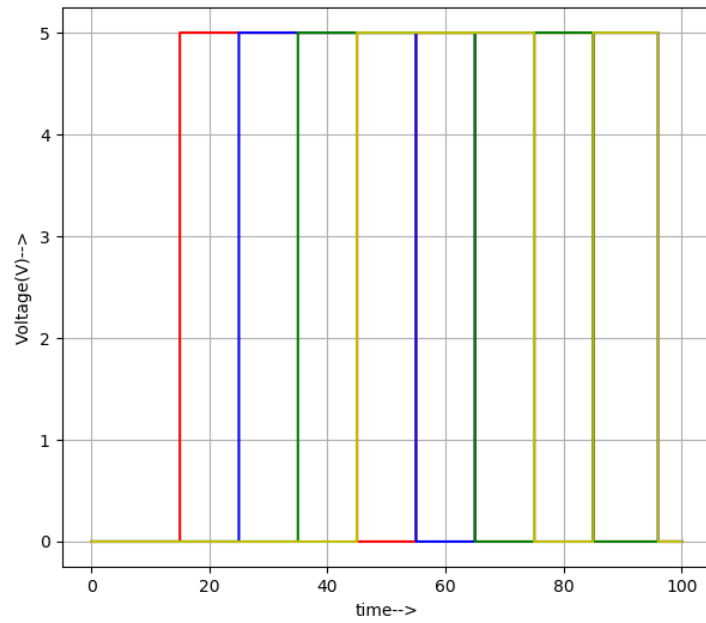
**Plot 4:** Output of Flip Flop 2



**Plot 5:** Output of Flip Flop 3



**Plot 6:** Output of Flip Flop 4



**Plot 7:** Output of All the Flip Flops

**Source/Reference(s):**

- 1. Made Easy Digital Electronics Theory Book for GATE**