Design And Analysis Of An Array Multiplier Using An Area Efficient Full Adder Cell (using 10t Full Adder)

Kanchan Kumar Kaity , Kalyani Government Engineering College

14th April , 2023

Abstract

The project is to implement Design And Analysis Of An Array Multiplier Using An Area-Efficient Full Adder Cell (using a 10t Full Adder). Circuit design and simulation have been done using esim and Skywater's 130nm PDK. Full adders are the main components for performing arithmetic operations with various types of multipliers. Hence, in most of the multipliers, full adders affect the overall speed of the system. So in this project, 10 MOSFET have been used to design an effective full adder. The main task is to improve the performance of the array multiplier by implementing this 10-bit full adder. Because of its low noise, low power, and low propagation delay, CMOS is used as the primary component in this application. I have designed both 2 bit and 4 bit array multiplier.

I. Circuit Details

This full adder cell has less power. consumption as it has no direct path to the ground. The elimination of a path to the ground reduces power consumption. But there is a problem: because it has multiple thresholds, it cannot be cascaded at low power supplies.

This adder is based on the XNOR gate. A high output (1) occurs if both of the inputs to the gate are the same. If one but not both inputs are high (1)then output will be low.

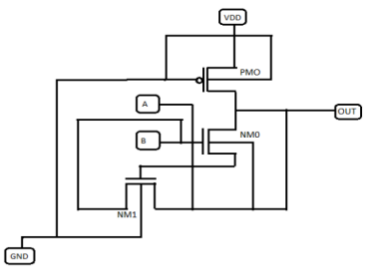


Fig 3: Proposed 3T XNOR Gate

At first some and gate has been designed . Then according to the array multiplier circuit full adder blocks and 'And gate's has been connected. For 2 bit multiplier 4 and gates and 2 full adders have been used (so total 6*4 + 10*2 = 44 MOSFET). For 4 bit system 16 and gates and 12 full adder blocks have been used (so total 16*6 + 10*12 = 216 MOSFET).

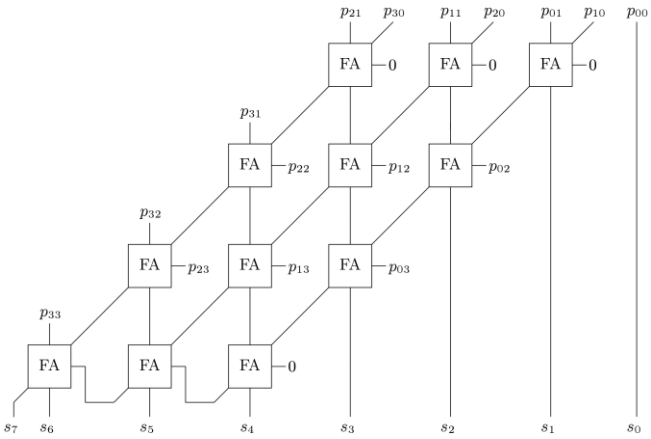
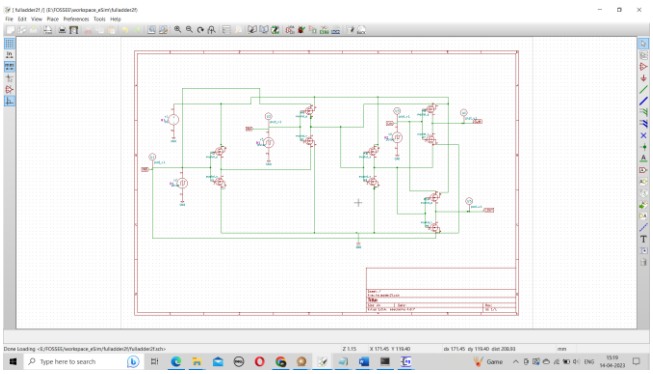


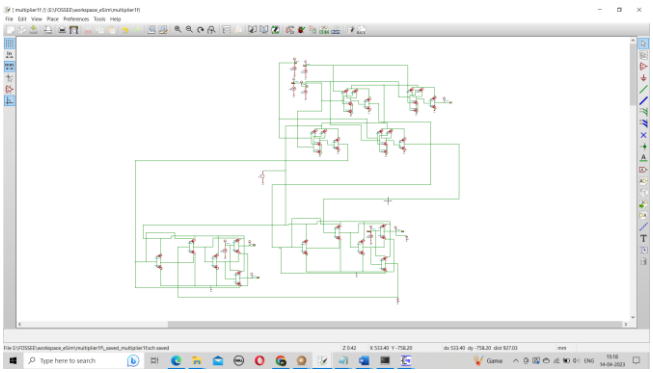
fig :4 bit array multiplier

.

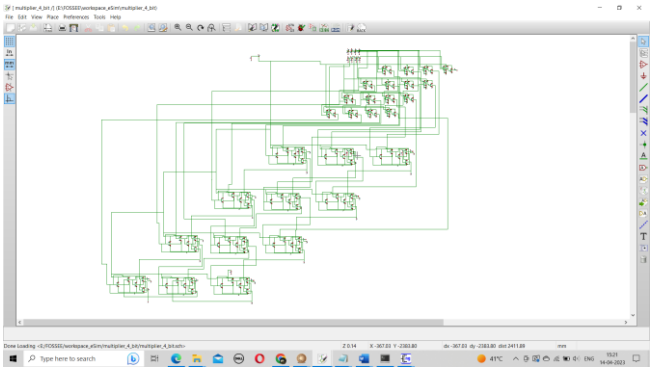
II. Implemented Circuit



Full adder (10T)



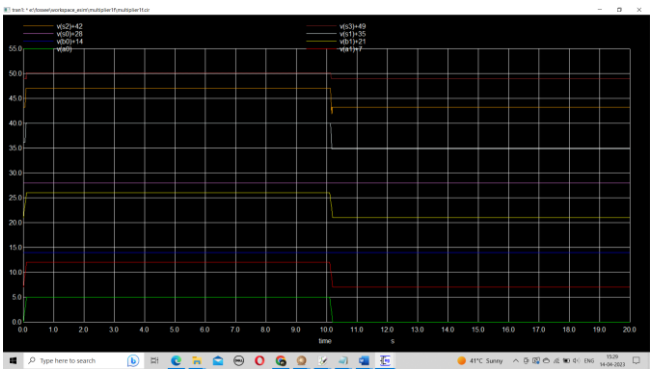
2 bit array multiplier



4 bit array multiplier

III. IMPLEMENTED WAVEFORMS

A. For 2 bit (A = 11 , B = 10 , Sum = 0110)



B. For 4 bit (A = 1110 , B = 0110 , Sum = 01010100)

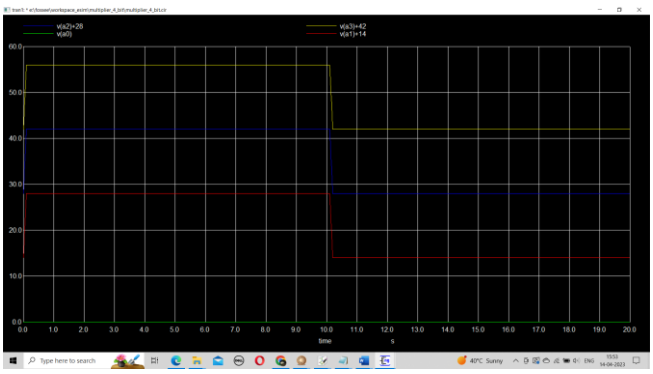


Fig: Input A (1110)

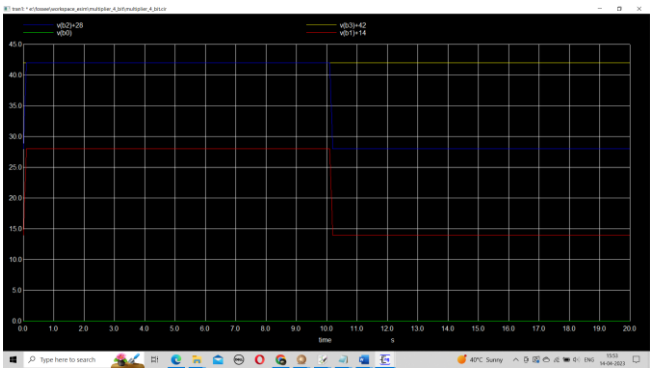


Fig: Input B (0110)

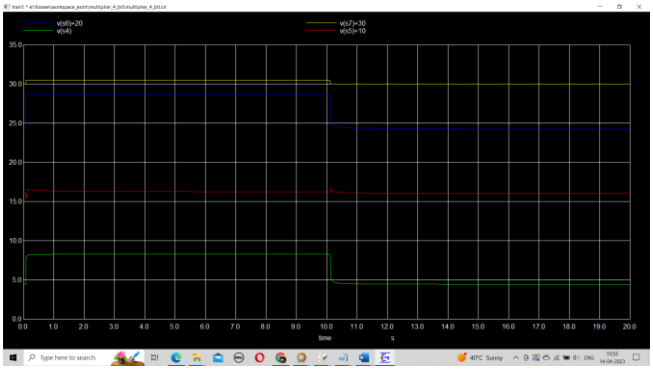


Fig: Output (s7 s6 s5 s4)

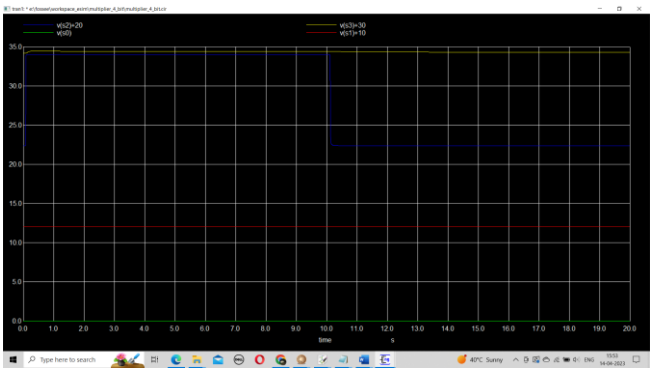


Fig: Output (s3 s2 s1 s0)

REFERENCES

[1] Design And Analysis Of An Array Multiplier Using An Area Efficient Full Adder in 32 nm CMOS Technology By Kripa Mathew , S.Asha Latha, T. Ravi , E. Logashanmugam

https://theijes.com/papers/v2i3/Part.Vol.%202.3%20(2)/B023208016.pdf

[2] Design of Low Power and High Speed Full Adder Cell Using New 3TXNOR Gate by Pramod Aladale

IJCSMC, Vol. 7, Issue. 6, June 2018, pg.31 – 36