Title of the Circuit Simulation Project:

Design Of Voltage-Controlled Oscillator In 180 nm CMOS Technology.

Theory:

Voltage Controlled Oscillator is the heart of the many modern electronics as well as communication system. Hence there is necessity of VCO to operate in the GHz frequency range. This project describes a design and implementation of Five Stage Current Starved CMOS Voltage Controlled Oscillator for Phase Locked Loop. Current starved VCO is simple ring oscillator consisting of cascaded inverters.

Schematic Diagram:

The circuit schematic of VCO in eSim is shown below:

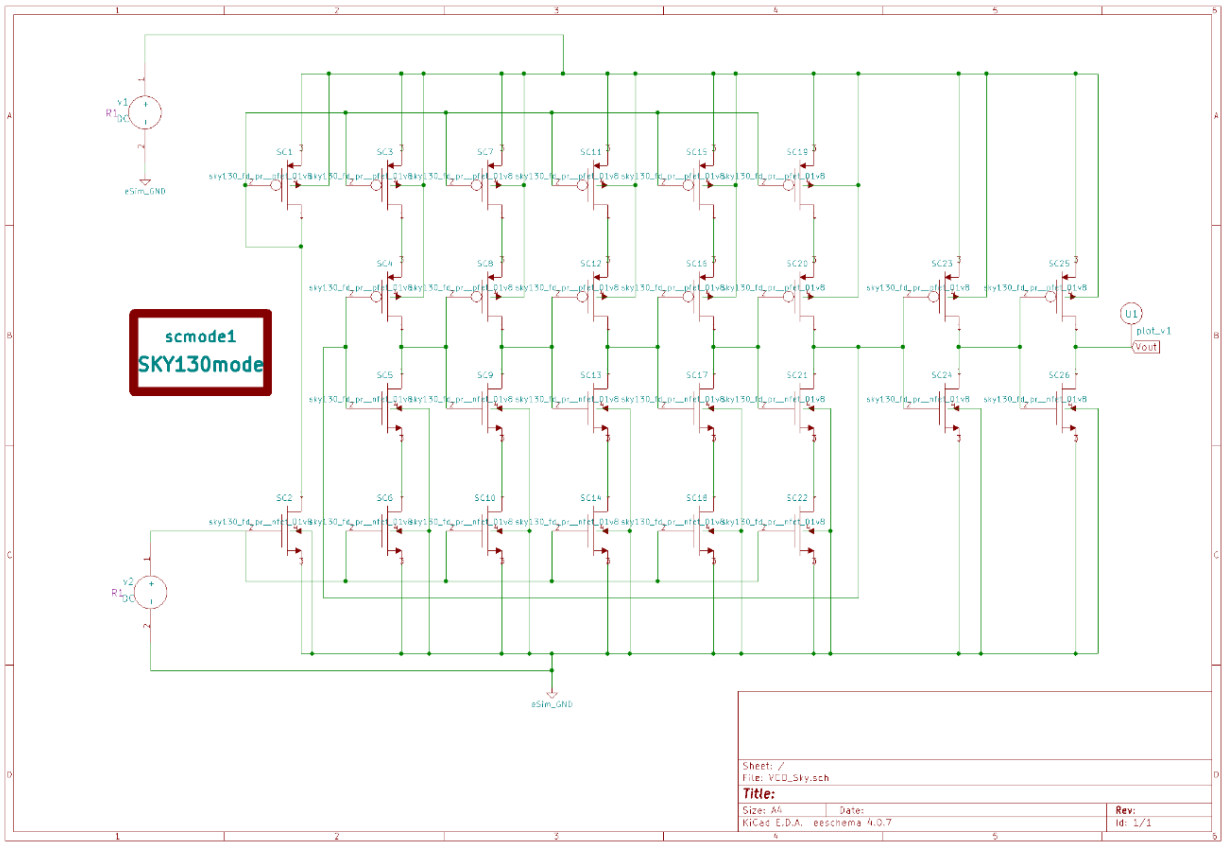

Figure 1: VCO using sky130 FETs in eSim.

Simulation Results:

Ngspice Plots:

1) For Vcntrl=0.9V and VDD=2V.

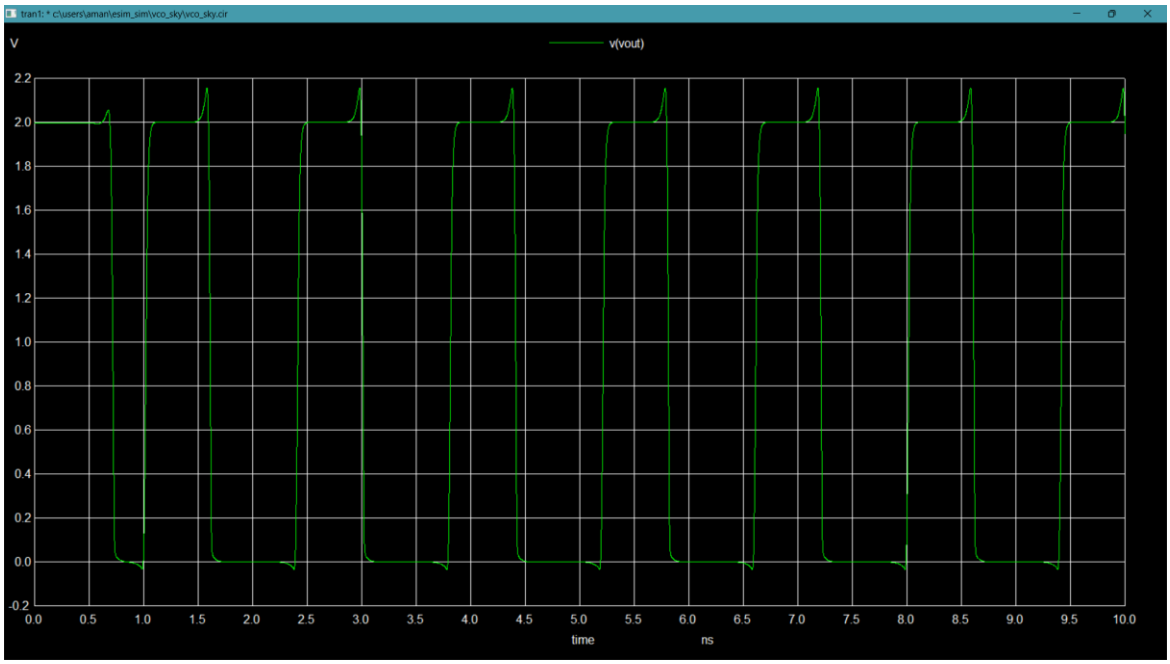

Figure 2: Vout for Vcntrl =0.9V.

2) For Vcntrl=1.8V and VDD=2V.

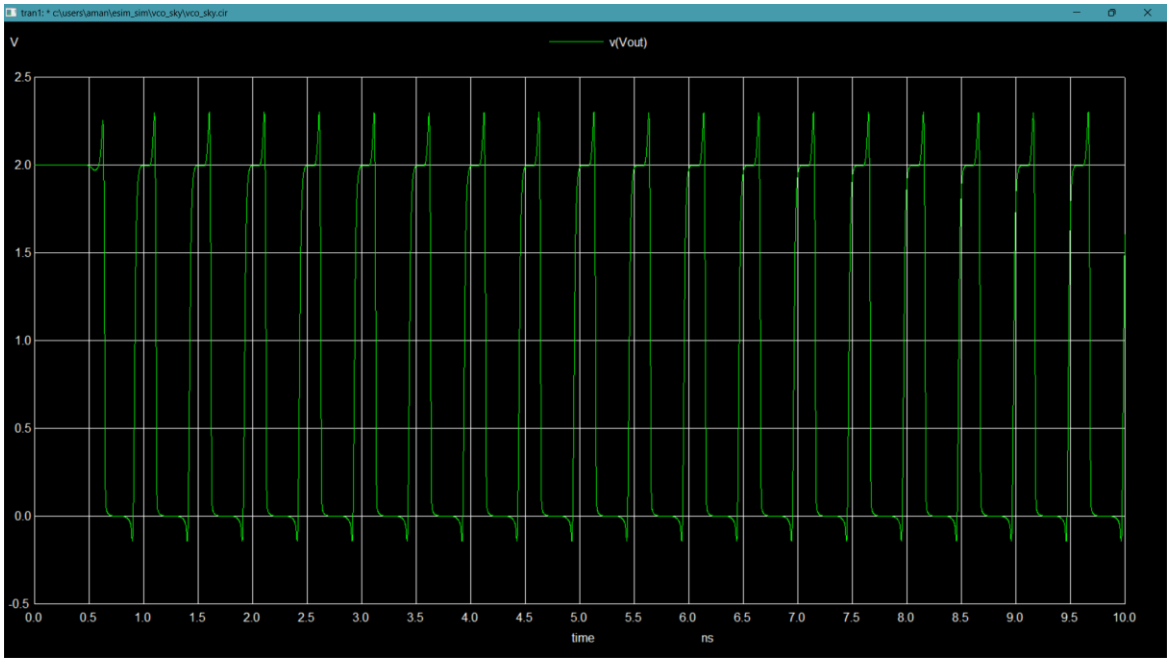

Figure 3: Vout for Vcntrl =1.8V

Conclusion:

In current starved voltage-controlled oscillator (VCO) generates 1.2GHz frequency at input control voltage (Vin) of 1.8V. Since Phase locked loop (PLL) is widely used in wireless communication systems. We can generate any desire frequency based on application requirement.

Reference:

https://www.irjet.net/archives/V5/i3/IRJET-V5I3191.pdf