Design of Delta-sigma modulator using eSim and Sky130

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***Abstract*— A Delta-sigma modulator is extensively used in digital communication to transfer data. The delay is generated using the Verilog code in Makerchip ide. Skywater 130 op-amp with other components like resistors is configured in adder and subtractor configuration. The input sampled voltage range is 0 to 1V. A 1-bit quantizer is also designed using the Verilog code in Makerchip IDE. The Verilog code is converted to Ngspice using NgVeri. The designed circuit is simulated in the eSim EDA tool developed by IIT Bombay.**

***Keywords*— op amp, Sky130, eSim, resistor, Verilog**

I. REFERENCE CIRCUIT DETAILS:

Fig 1. It shows the block diagram of Delta modulator. From block diagram 1 bit quantizer output is delta when input is greater than 0 and output is –delta when input is less than 0. The delay block output is high when previous input is low, delay block output is low when previous input is high. Delay block and 1-bit quantizer is designed using Verilog Code in Makerchip IDE

The input quantized signal Vin is passed through analog to digital converter. The digital output is passed through ashwini_delay1bit module designed in Makerchip using Verilog code. The ashwini_delay1bit generates a delay of time T in input sampled signal. The delayed output data is passed to digital to analog converter bit R-2R ladder type DAC. The DAC convert the 2-bit data to analog signal which is a delayed Vin i.e. Vin(n-T) as shown in Fig 4. The delayed Vin(n-T) and Vin is passed through subtractor and quantizer which is obtained through the Sky130 avsd_opamp in comparator configuration. The output obtained after passing through the comparator is the delta-modulated output of Vin

The output obtained at Vin[n] is plotted in eSim. The Delta modulated output is obtained at delta_out[n] as shown in Fig 5.

II. REFERENCE CIRCUIT DESIGN

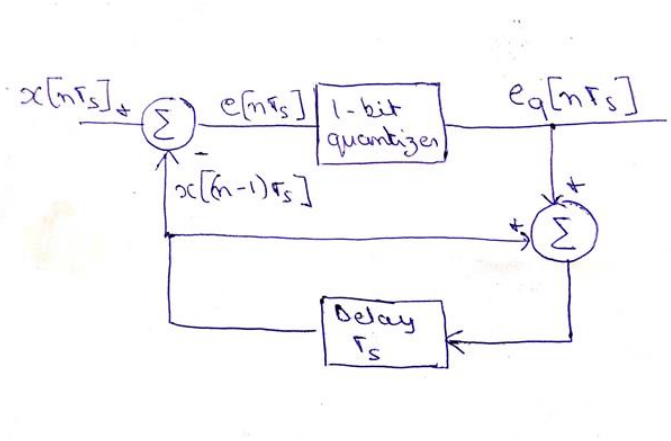

Fig. 1. Delta-Sigma modulator Block Diagram

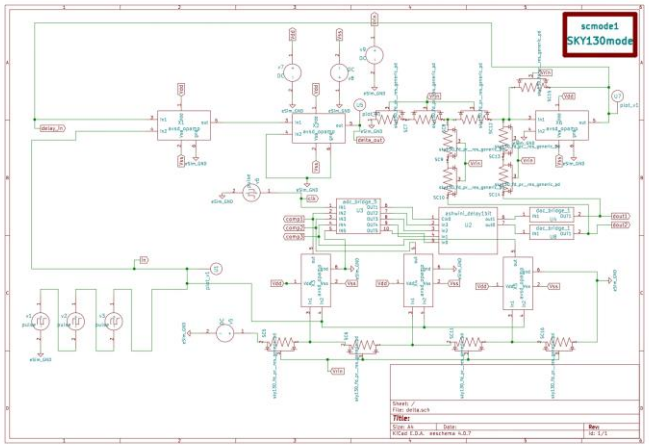

Fig. 2. eSim Circuit schematic

III. REFERENCE WAVEFORM

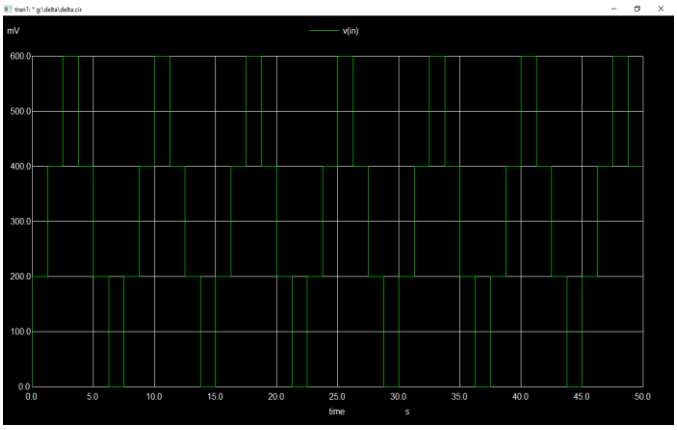

Fig. 3. Input sampled signal waveform Vin

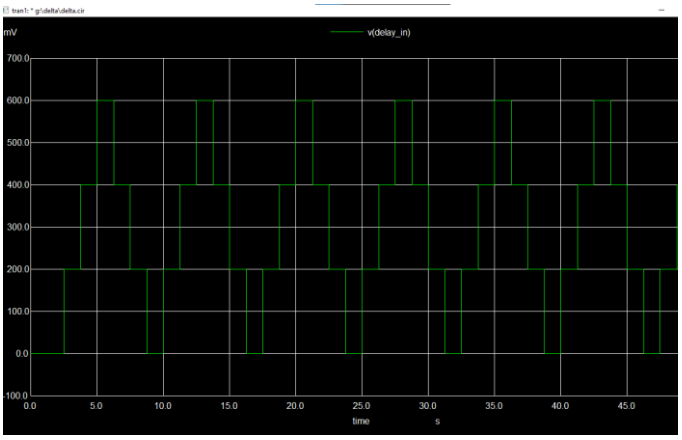

Fig. 4. T time delayed input signal waveform Vin (n-T)

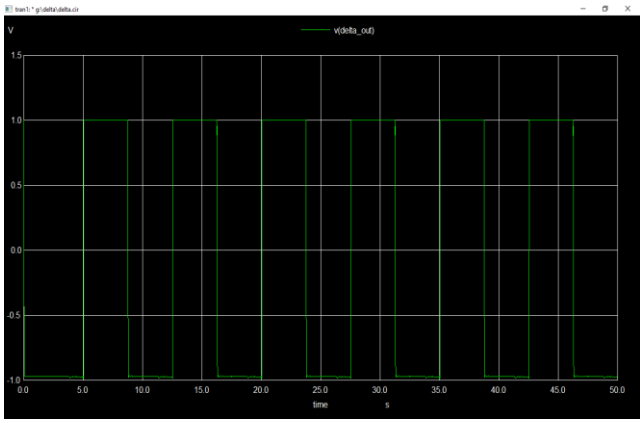

Fig. 5. Delta modulated waveform of sampled input signal Vin(n)

CONCLUSION

Delta modulated waveform of sampled input voltage is obtained and plotted. The ashwini_delay1bit module is obtained using verilog code. The verilog code can be obtained from github link: https://github.com/ashwini0921/Design-of-Delta-sigma-modulator-using-eSim-and-Sky130. The Input vaveform, delayed input waveform and output waveform is plotted in eSim.

REFERENCES

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[3] https://github.com/Eyantra698Sumanto/Two-in-One-Low-power-XOR-XNOR-Gate.git

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