Title of the Experiment:

Amplitude Shift Keying(ASK) Modulation-Demodulation

Theory:

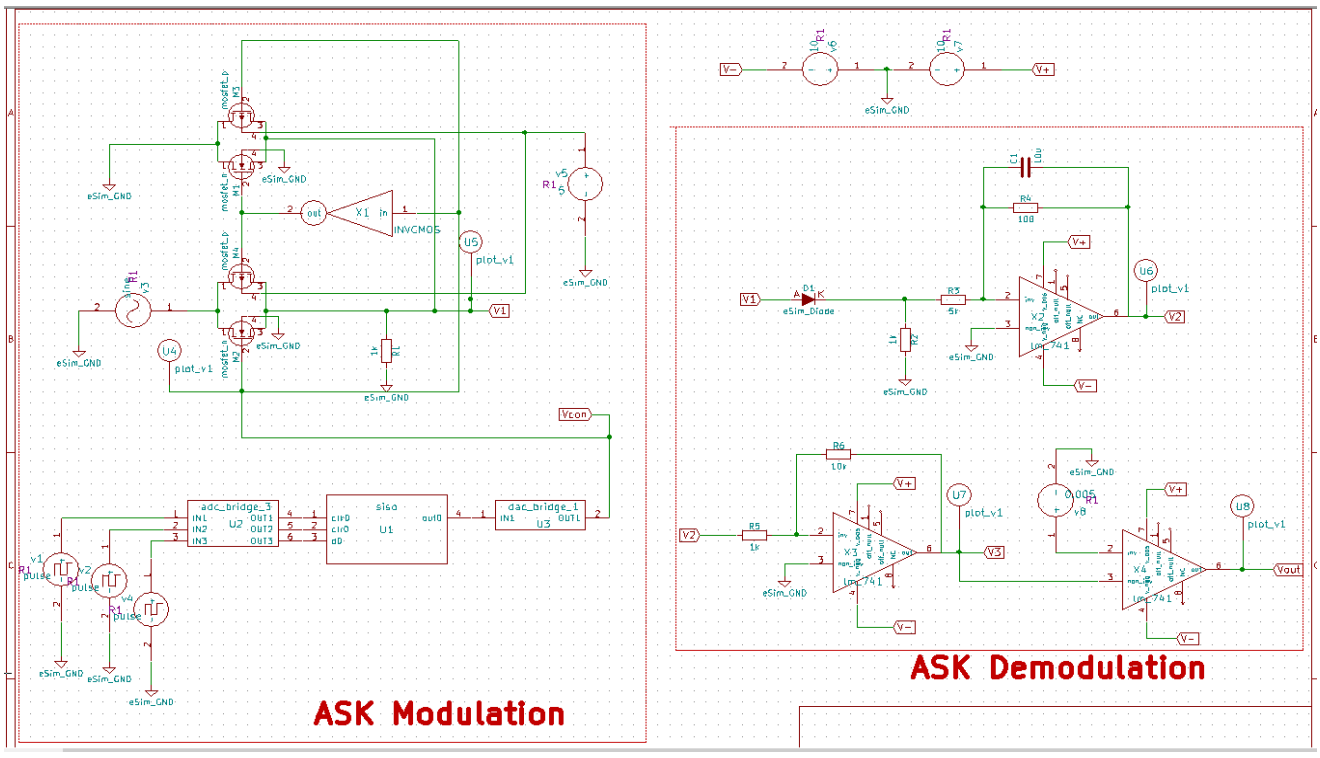
Amplitude Shift Keying(ASK) is a sort of signal modulation technique that represents binary data (in pulses) as variations in the amplitude of the modulated wave. When the pulse is logic high, the output follows an input sine wave and when pulse is logic low, the output gives zero voltage.

In this experiment, I have designed a mixed signal circuit for implementing ASK modulation and demodulation. A randomly generated series of pulse signals is achieved using a Serial-in-Serial-out (SISO) register designed using Verilog. The output of this block acts as our input control voltage to a CMOS 2:1 multiplexer. The output to this mux is the desired ASK signal.

For demodulation, I have implemented a series of circuit blocks in the following order- Rectifier -> Active Low Pass Filter -> Amplifier -> Comparator. The final output gives back the input pulse signal thus resulting in an ASK Demodulated wave.

Schematic Diagram:

Below is the schematic for ASK Modulation-Demodulation circuit.



Simulation Results:

1. NgSpice Plots:

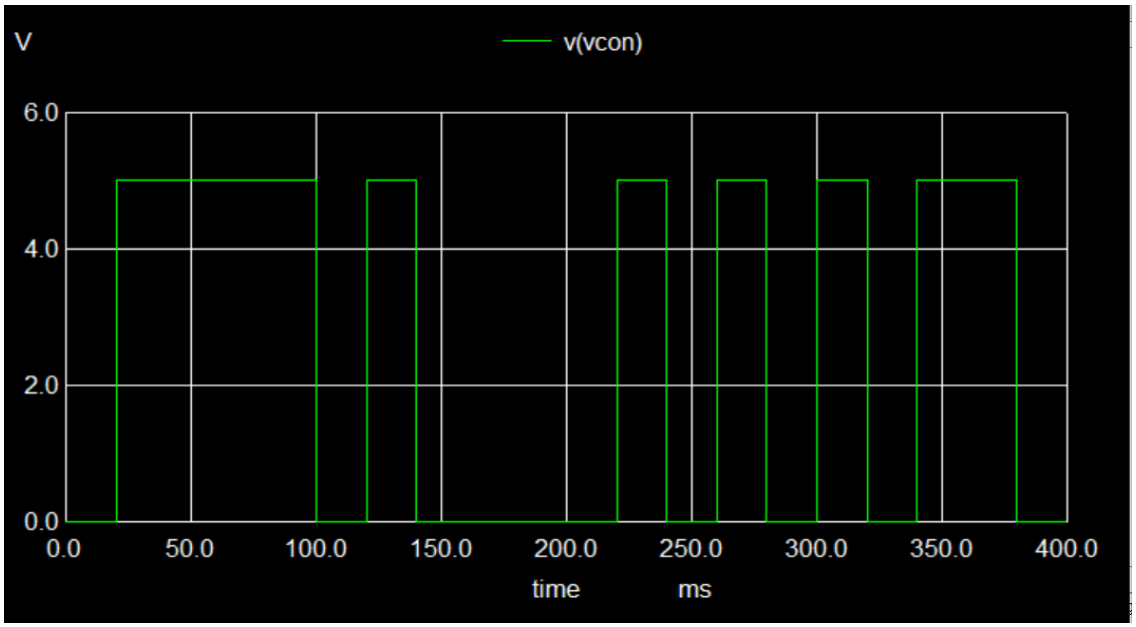


Figure 1: Input pulse wave from SISO register

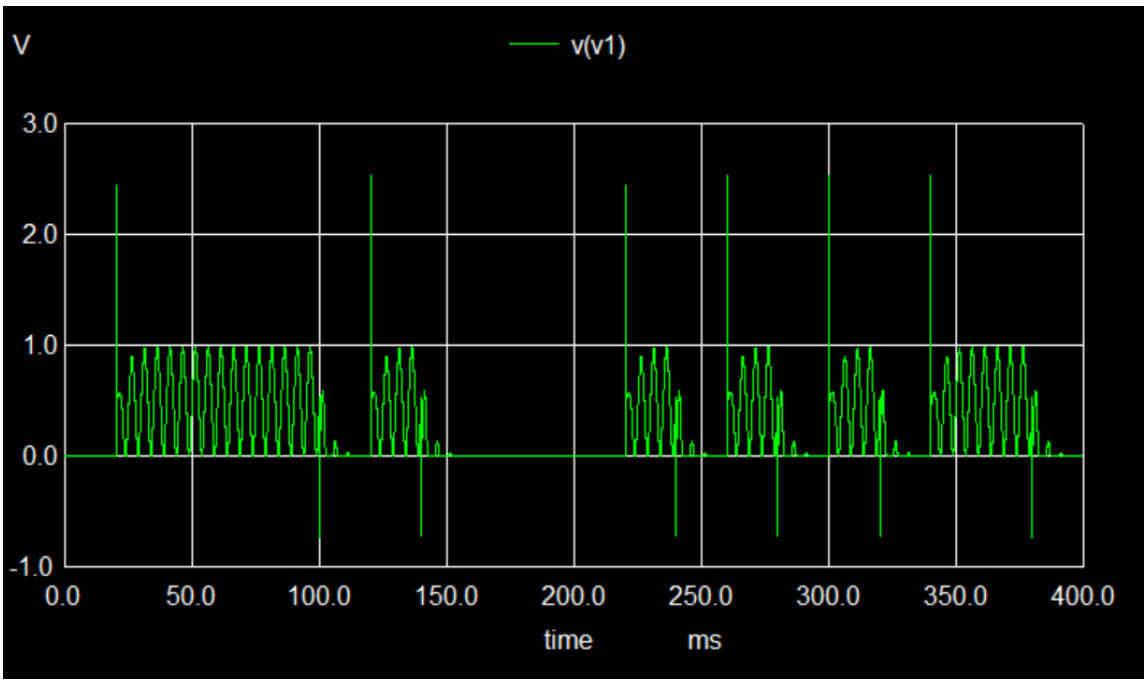


Figure 2: Amplitude Shift Keying(ASK) signal

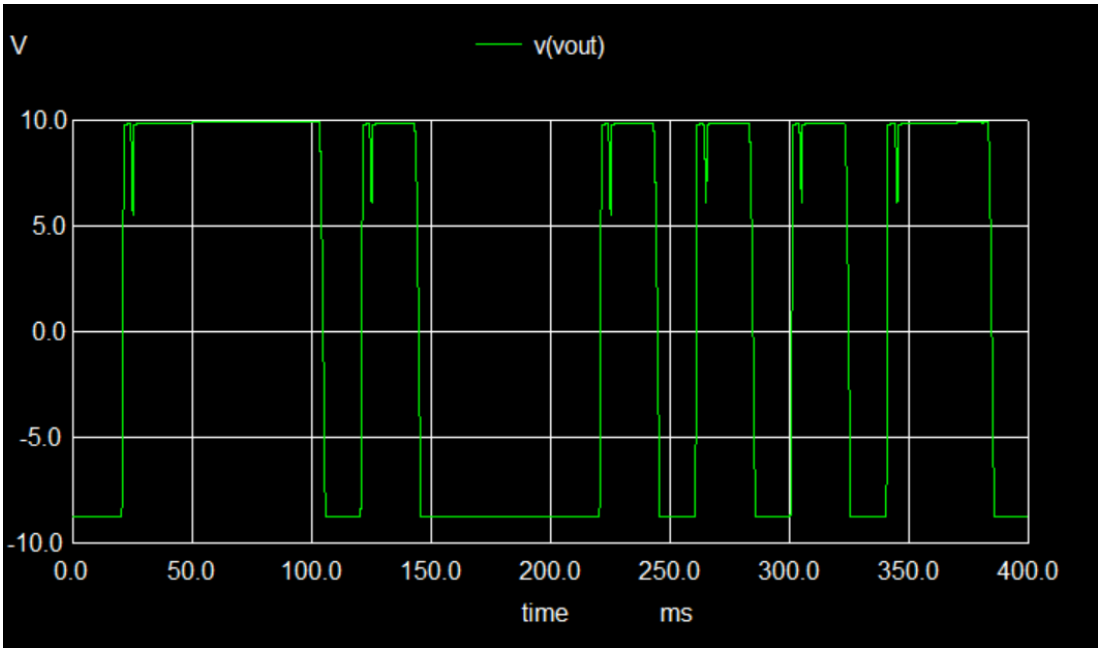


Figure 3: ASK Demodulated signal output

2. Python Plots:

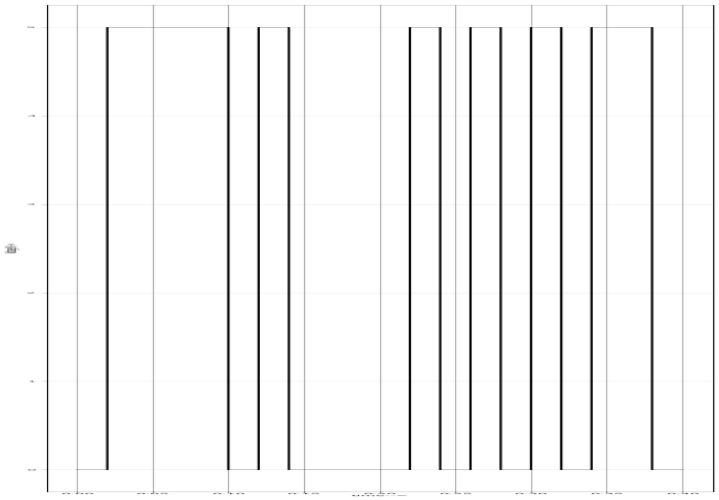


Fig 4: Input pulse from SISO register

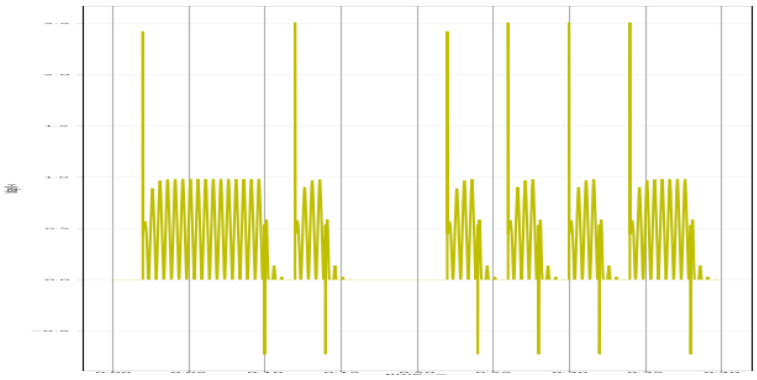


Fig 5: ASK signal output

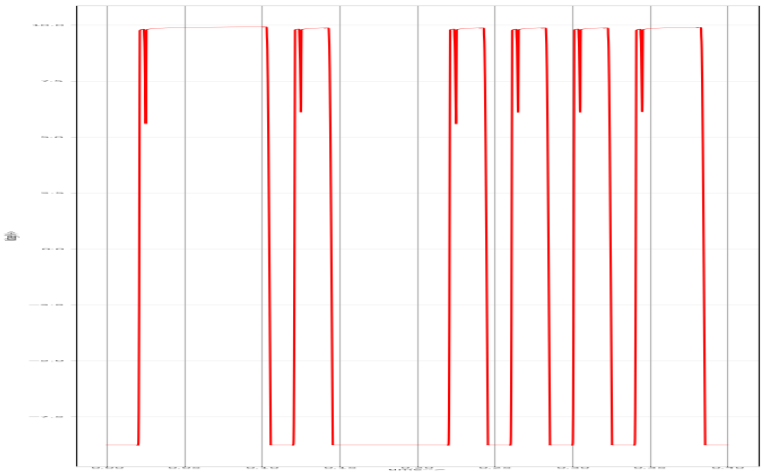


Fig 6: ASK demodulated signal output

Conclusion:

From the above simulations, we have thus understood the generation of an Amplitude Shift Keying(ASK) signal using a mixed signal circuit consisting of a SISO register and a CMOS mux along with its demodulation using a Low Pass Filter followed by a comparator.

References:

1. https://www.tutorialspoint.com/digital_communication/digital_communication_amplitude_shift_keying.htm