Title of the experiment:

Mod 5 Counter Using Mixed Signal And Sky130

Theory:

We are presenting the MOD-5 counter using Mixed Signal and SKY130. Flip Flops are widely used in electronic circuits as they have frequency division property. Counters are sequential logic devices that are activated or triggered by an external timing pulse or clock signal. The design we are going to use is the and and the not gate will be made using analog block and the D flip flop will be made of digital block. The Astable Multivibrator Circuit will generate an input clock.

We will see that the circuit of our design is made of D flip flops and logic gate (AND and NOT). We can generate the output state of 101 (5) to give us a signal to clear the counter back to zero with the help of a 3-input AND gate and a NOT gate which acts as an inverter. The clock signal will be converted into a digital signal after being generated using the Astable Multivibrator circuit.

Schematic Circuit Diagram:

In Fig.1 we see the implementation of the 3 input AND Gate will be implemented using 2 AND using CMOS. This part of our circuit will be the analog circuitry block. The circuit is designed using SKY130. The D flip Flop combined block i.e 3 blocks is merged into a single counter block using Verilog Hardware Description Language. The Astable Multivibrator Circuit is used to generate the clock signal.

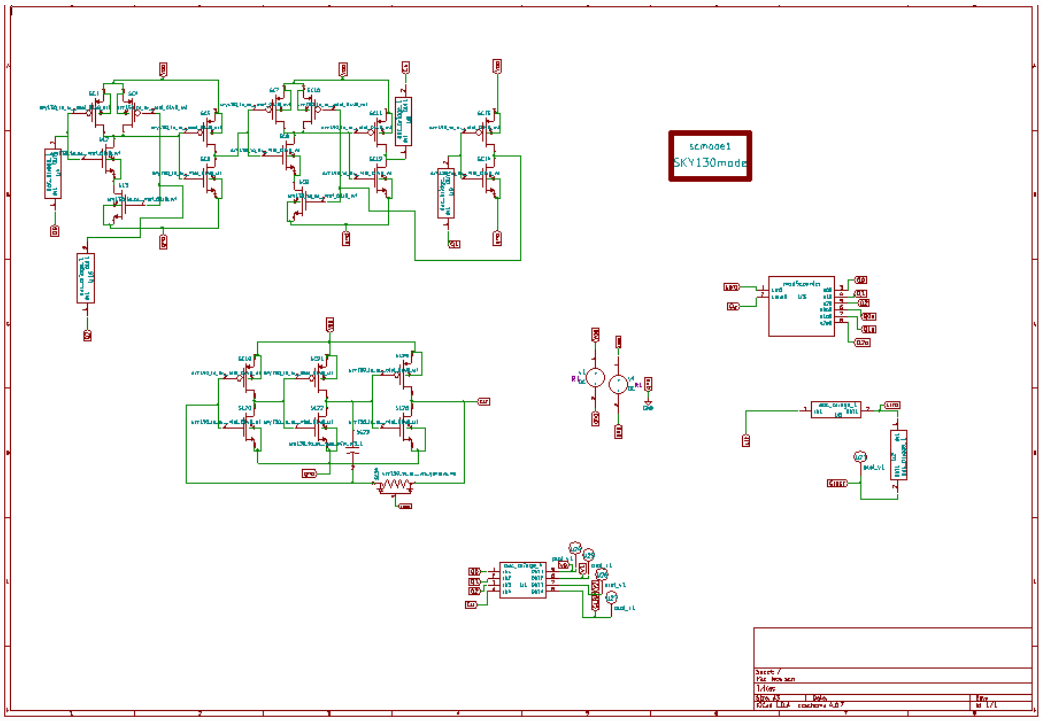

Fig 1. Schematic of MOD5 Counter

Simulated Waveform (Ngspice Plots):

The waveform generated by MOD 5 counter is shown below.

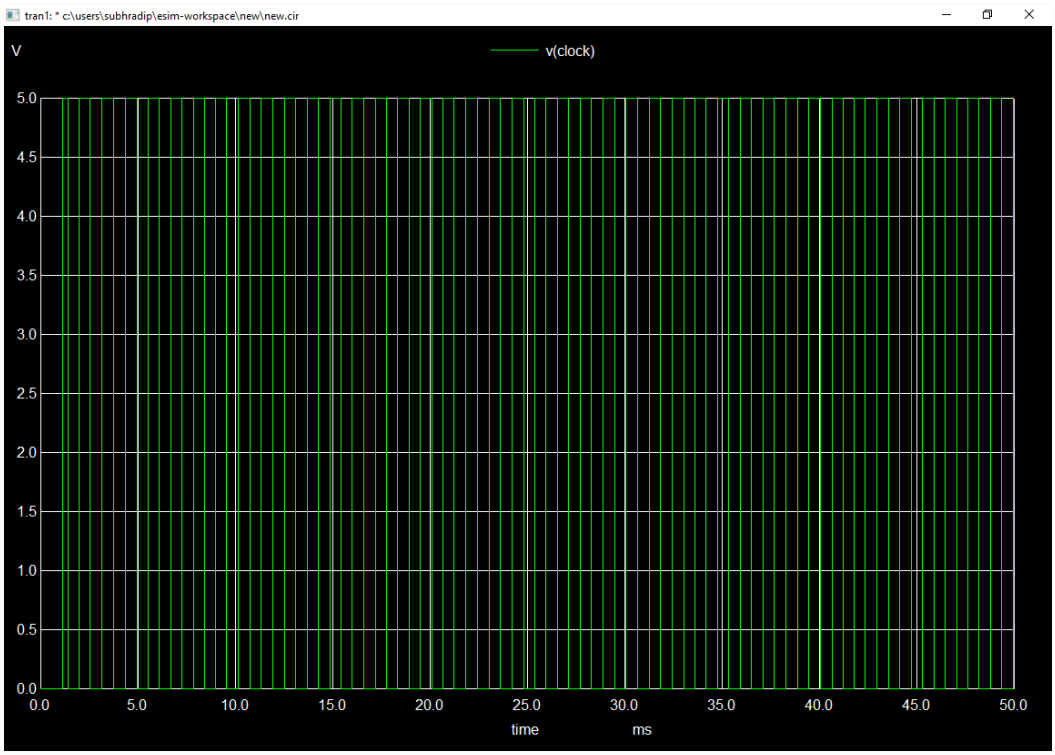

Fig 2. Clock Signal

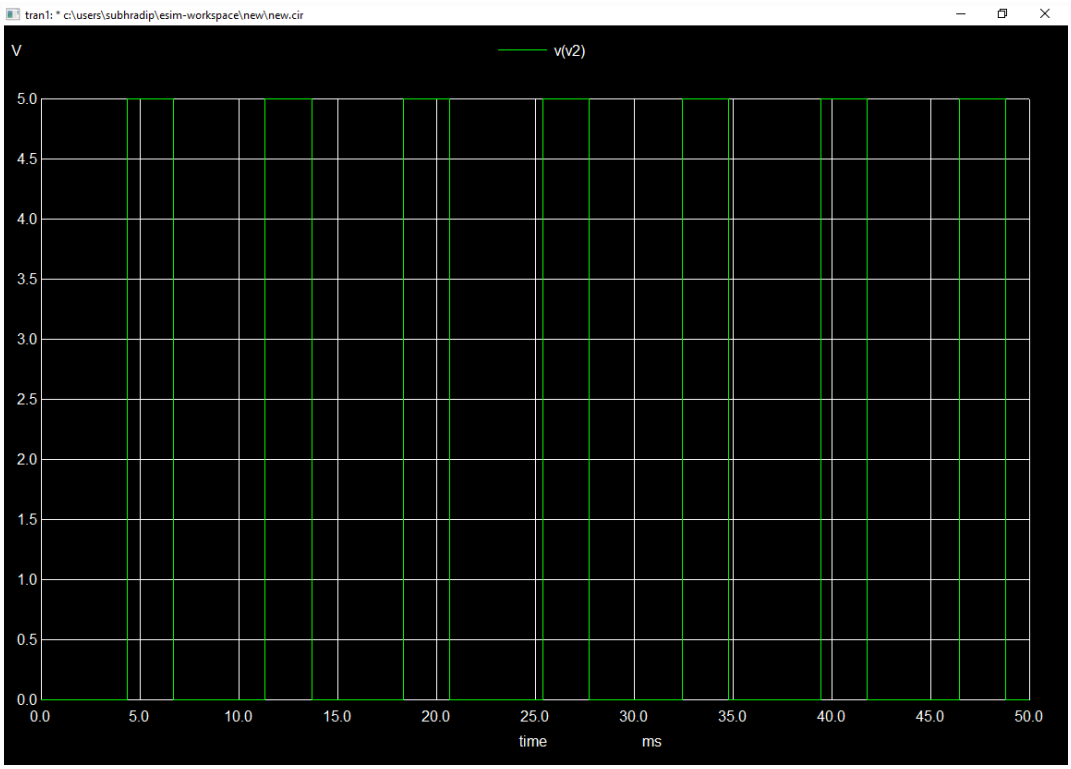

Fig 3. MSB Bit

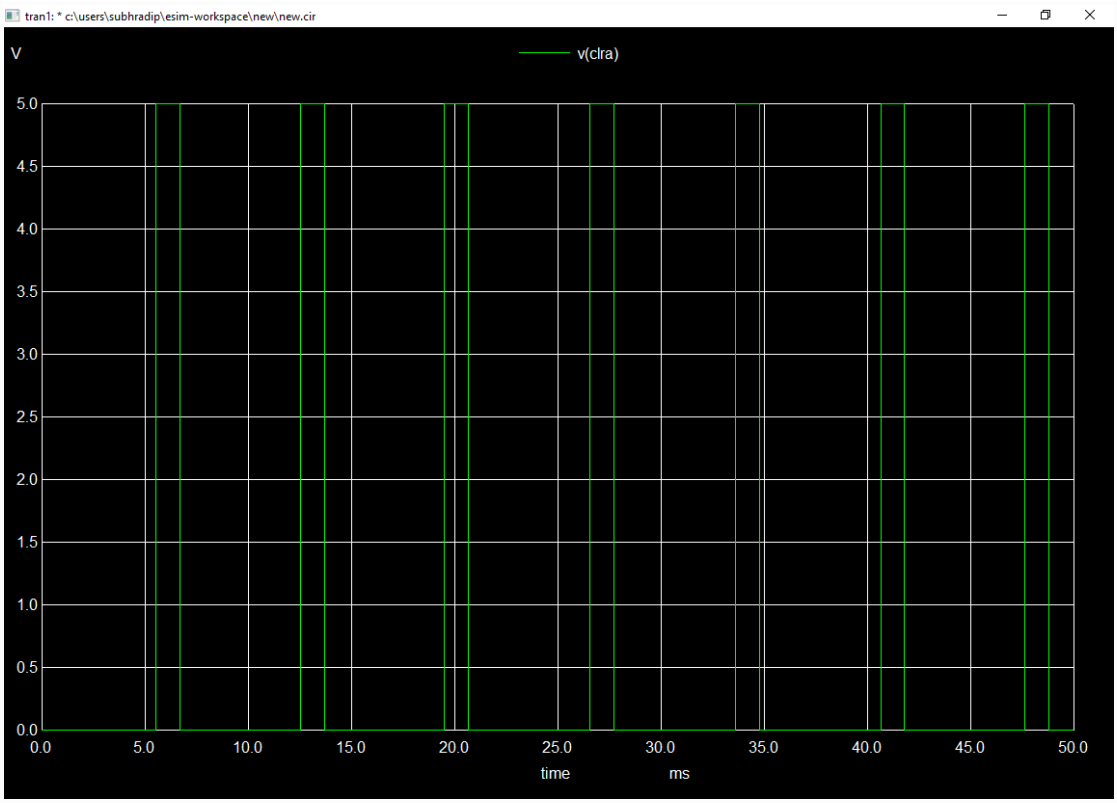

Fig 4. Clear Signal

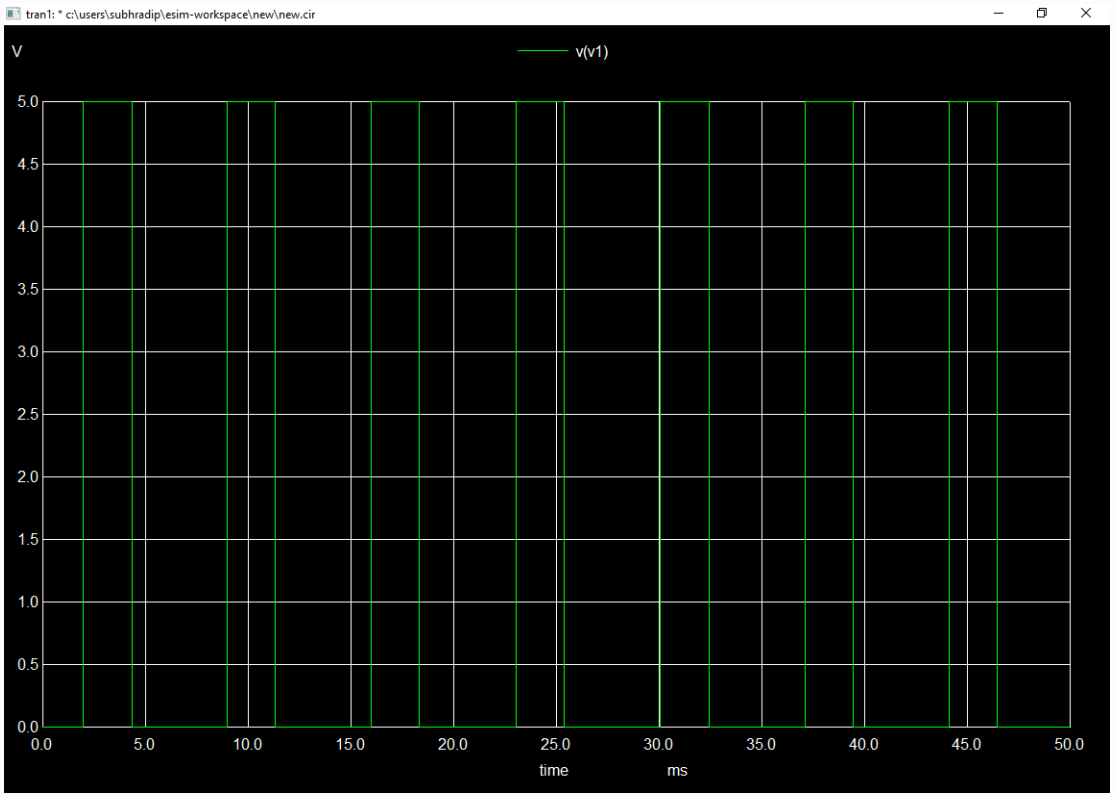

Fig 5. Middle Bit

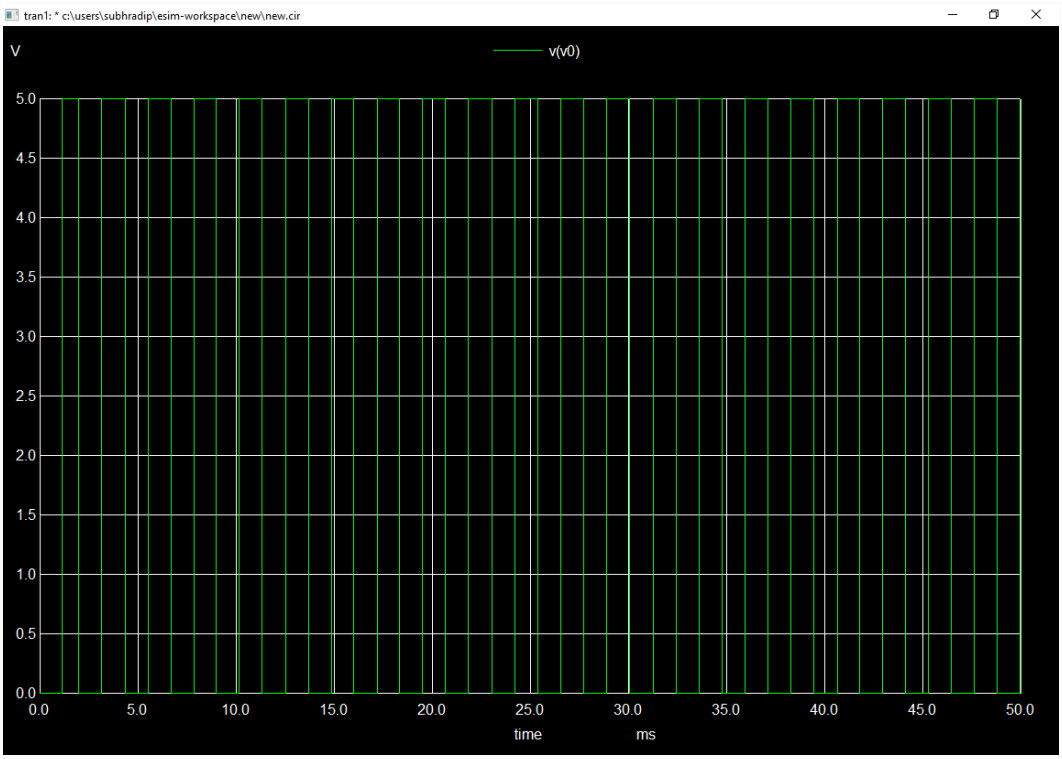

Fig 6. LSB Bit

Combined Plot:

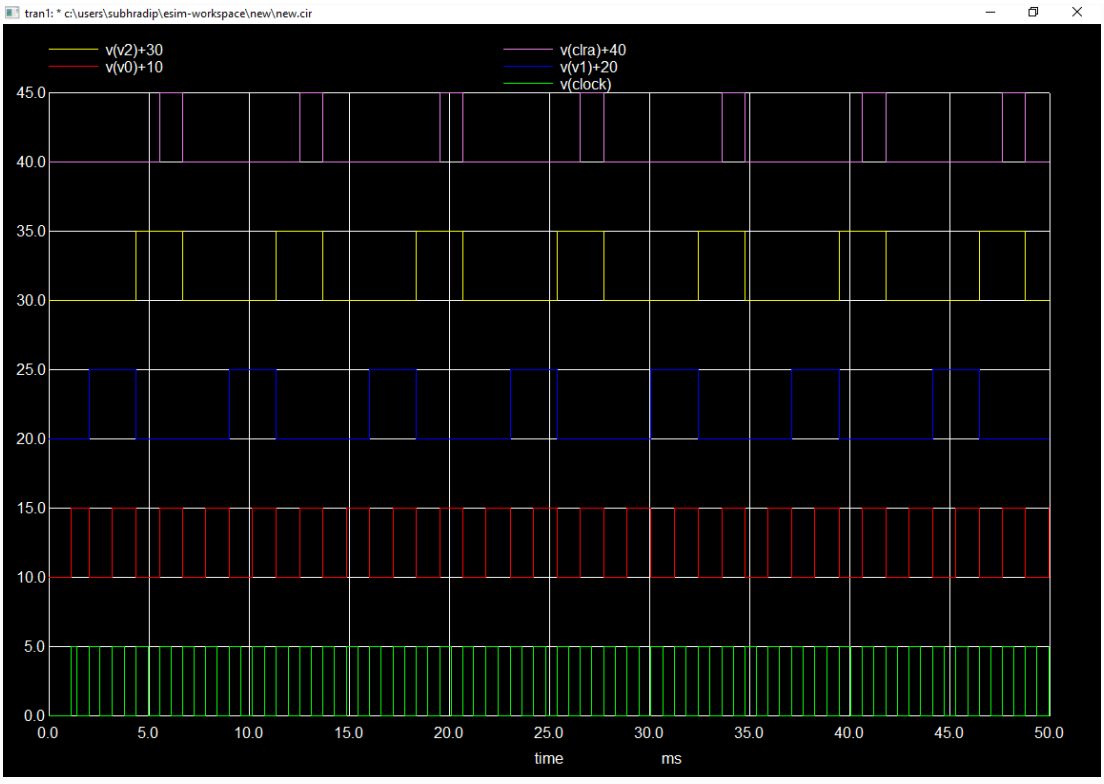

Fig 7. Combined Waveform

Conclusion:

Thus, we have studied the waveform of the MOD5 counter using Mixed Signal and SKY130 implemented on eSim and we were able to generate the appropriate waveforms.

References:

- https://www.electronics tutorials.ws/counter/mod-counters.html
- https://www.homemade-circuits.com/cmosastable-bistable-monostable-circuits-explained/
- Singh, Balraj Kumar, Mukesh Ubhi, Jagpal. (2017). Analysis of CMOS based NAND and NOR Gates at 45 nm Technology