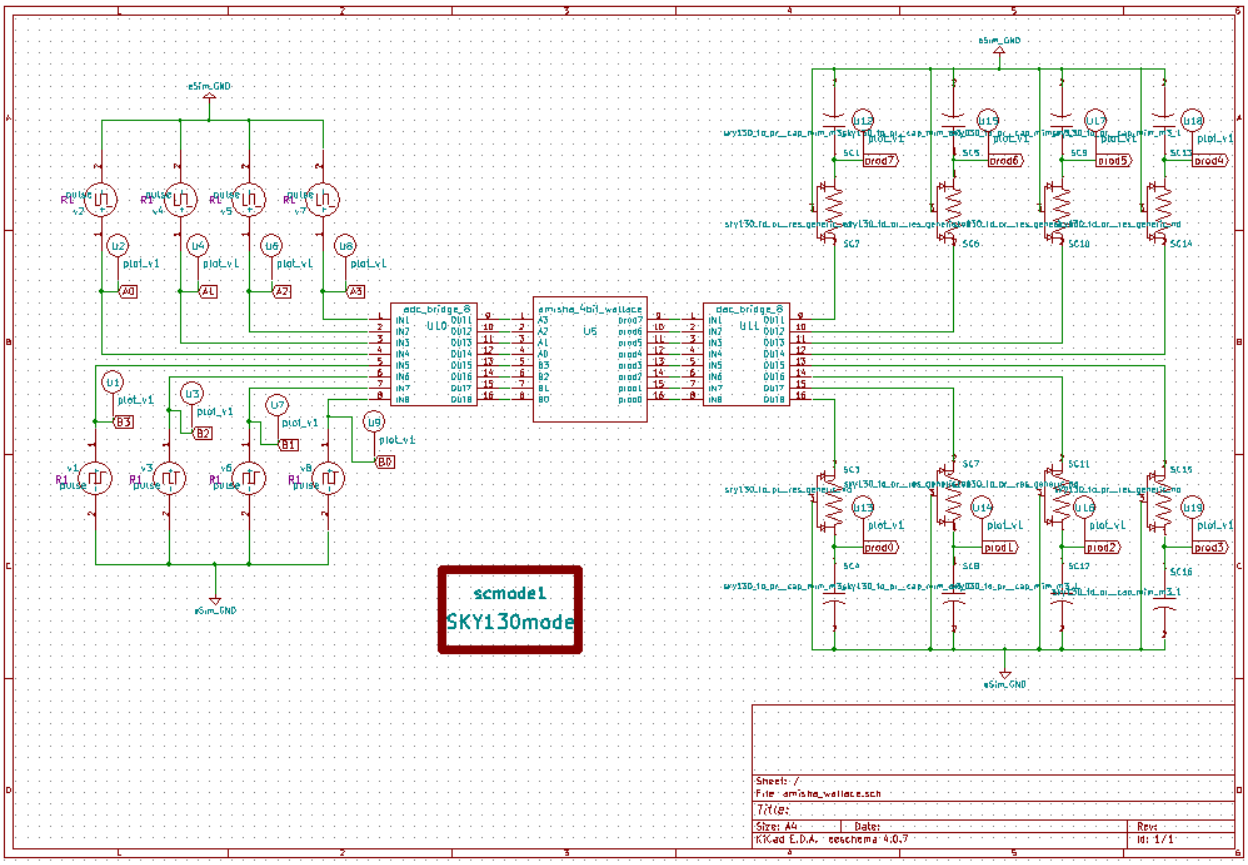
4-BIT WALLACE TREE MULTIPLER

THEORY:

One of the main components of the majority of high performance digital systems, including microprocessors, signal processing circuits, FIR filters, etc., is the multiplier. The demand of fast multipliers with low power consumption is increasing day by day. A Wallace multiplier is a hardware implementation of a binary multiplier, a digital circuit that multiplies two binary numbers. The input is 4-bit numbers which will be multiplied using the Wallace tree algorithm and it will produce an 8-bit product. It uses a selection of full and half adders (the Wallace tree or Wallace reduction) to sum partial products in stages until two numbers are left. Wallace multipliers reduce as much as possible on each layer. Initially, every bit is multiplied with every bit of the other number, and then these partial products which have weight equal to the product of its factors are further reduced to obtain the respective weights by using half adders or full adders based on the size. The final result is calculated by the sum of all these partial products.

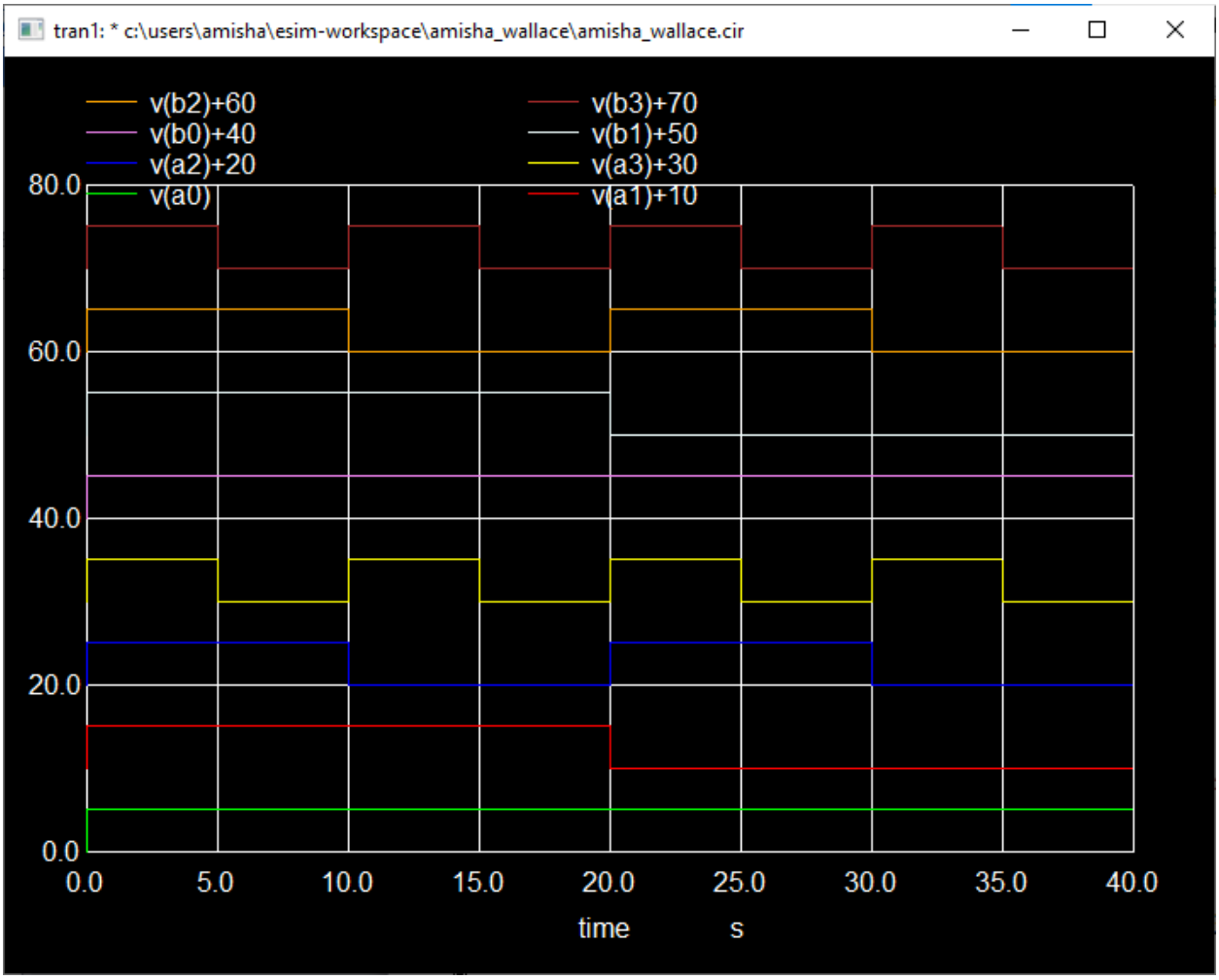
SCHEMATIC DIAGRAM:

The circuit schematic of the 4 bit Wallace Tree Multiplier using Sky130PDK in eSim is as shown below:

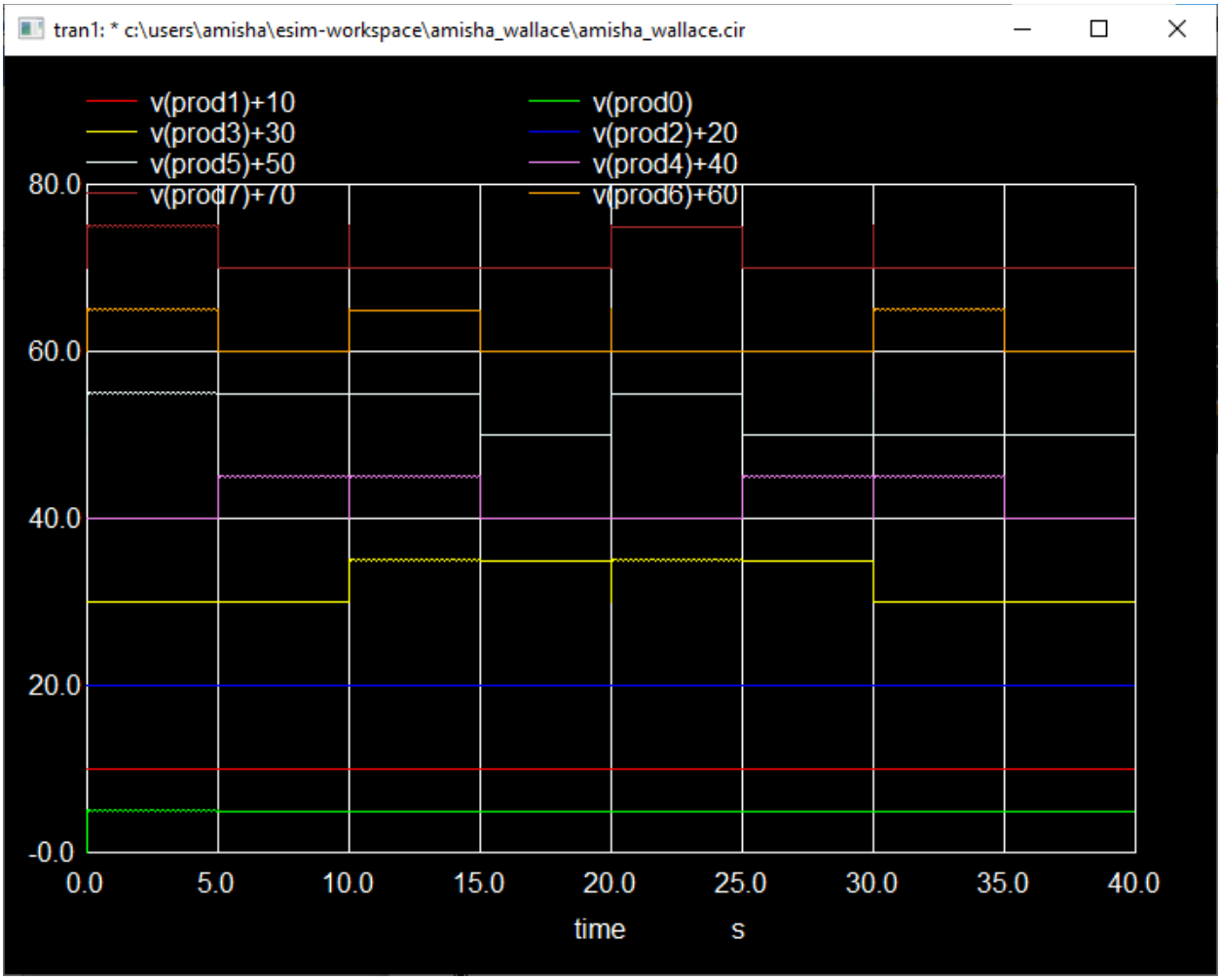


SIMULATION RESULTS:

1. Input 4-bit: A(a0, a1, a2, a3) B(b0, b1, b2, b3)



2. Output 8-bit: P(p0, p1, p2, p3, p4, p5, p6, p7)



CONCLUSION:

Thus, we have implemented 4 bit Wallace Tree Multiplier Using Sky130PDK in eSim and the appropriate waveforms are obtained.

REFERENCES:

(1) https://en.wikipedia.org/wiki/Wallace_tree

(2) https://www.coursehigh.com/downloads/solved-2-multiplication-two-4-bit-numbers-shown-figure-1-implemented-wallace-tree-multiplier-show-q34936053/