MIXED SIGNAL 16 BIT ADDER USING SKY130PDK

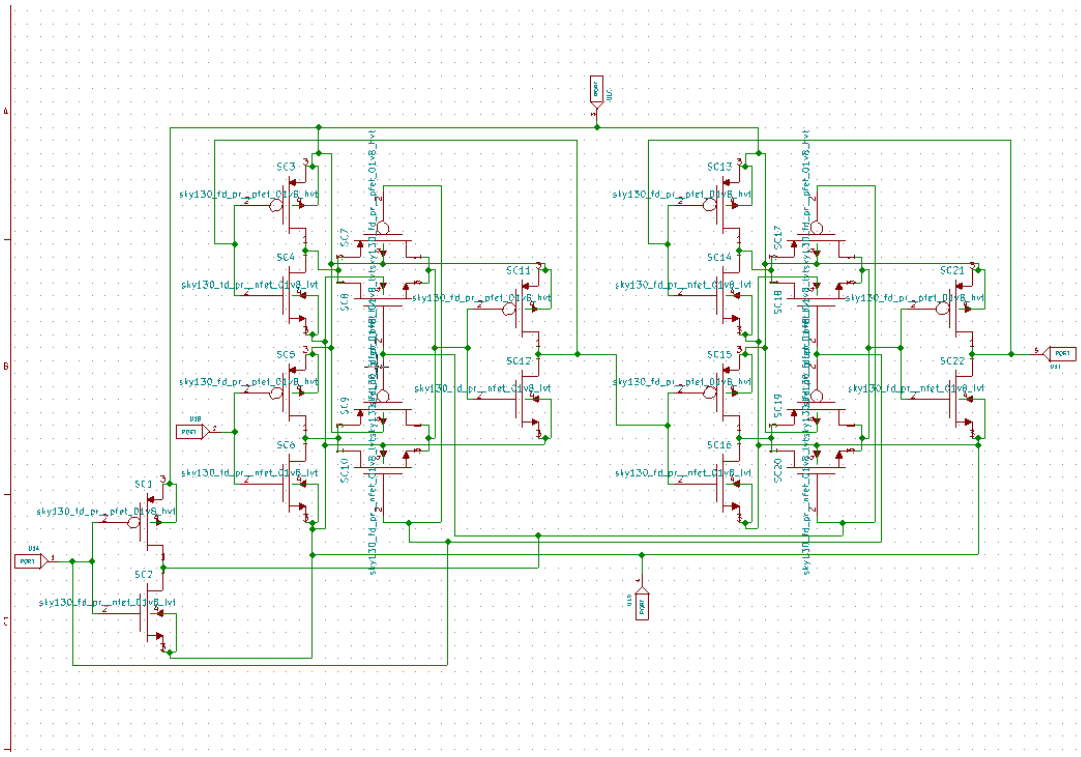
Theory:

The Mixed Signal 16 Bit Adder consists of digital part which is a ripple carry adder designed using Verilog and analog part consists of register array made up of negative-edge triggered D type master-slave flip-flop. The master flip-flop is a mux type constructed using the transmission gates. The transmission gate is a bidirectional circuit which is made by connecting the pfet and nfet in parallel. Four ripple carry adders are used and for each adder the 4 input bits each out of 16 are given starting from the LSB to MSB. The carry from the first ripple carry adder is delayed by one clock cycle and given as the carry input to the second stage ripple carry adder. Each stage ripple carry adders are pipelined in such a way that the final output is obtained at the 3rd clock cycle.

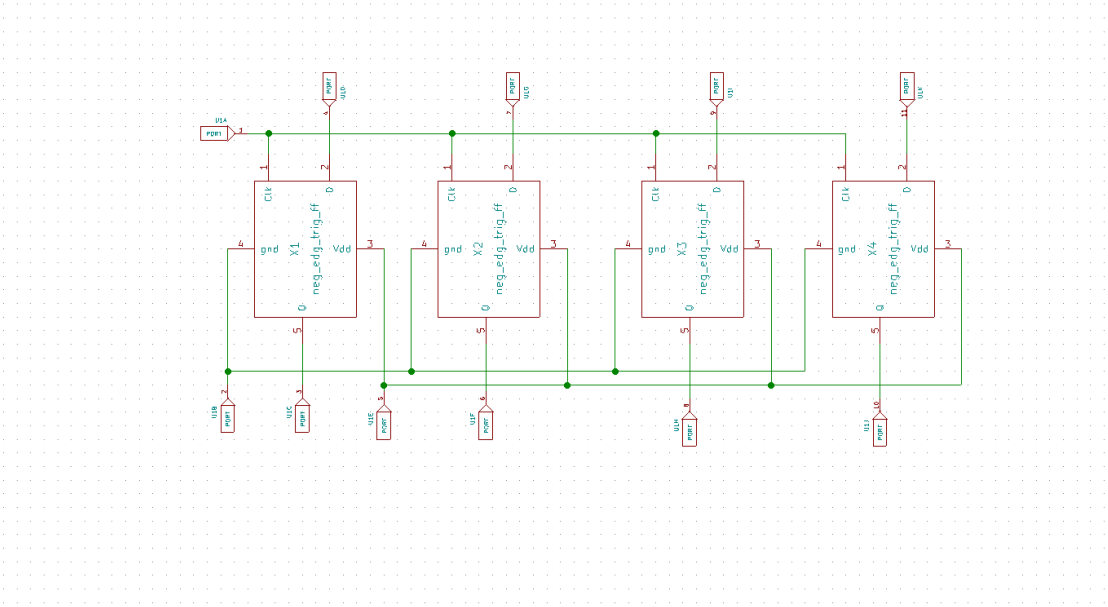
Schematic Diagram:

The circuit schematic of the mixed signal 16 bit adder using sky130pdk in eSim is as shown below:

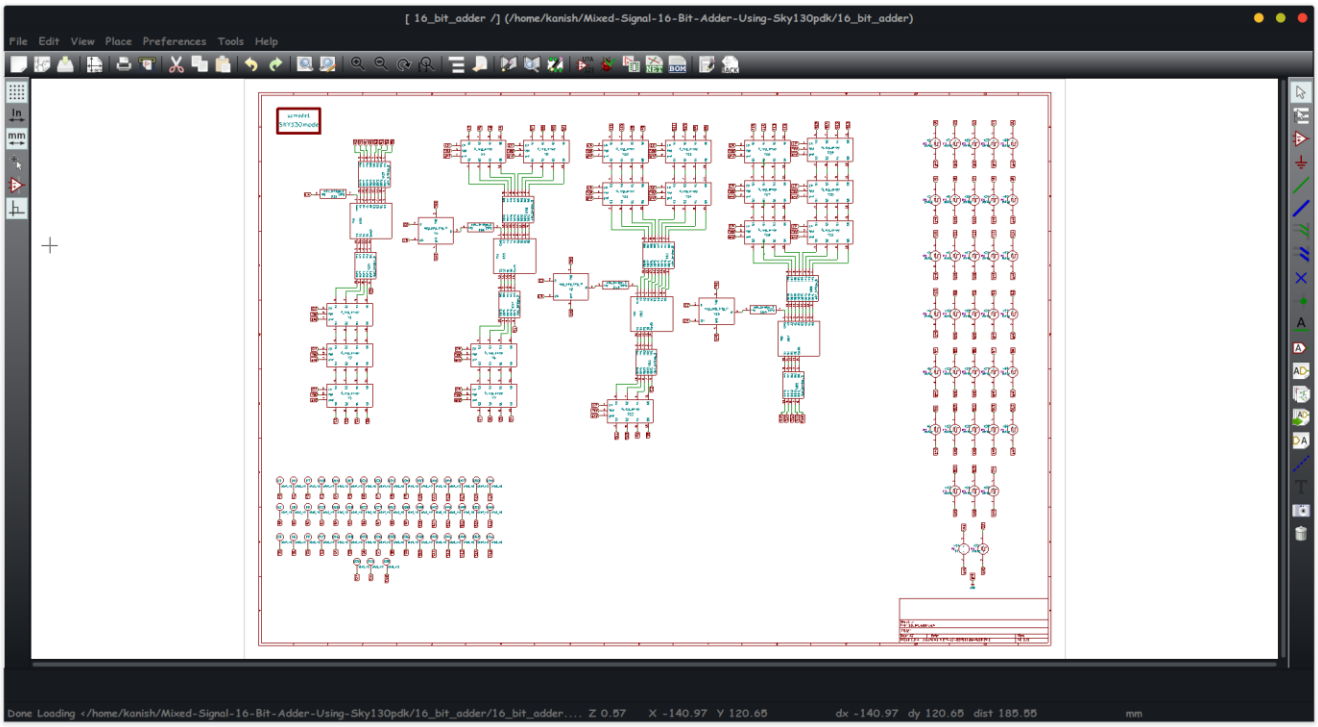
1. **Negative edge triggered master slave flip-flop sub circuit**



2. 4 bit register sub circuit

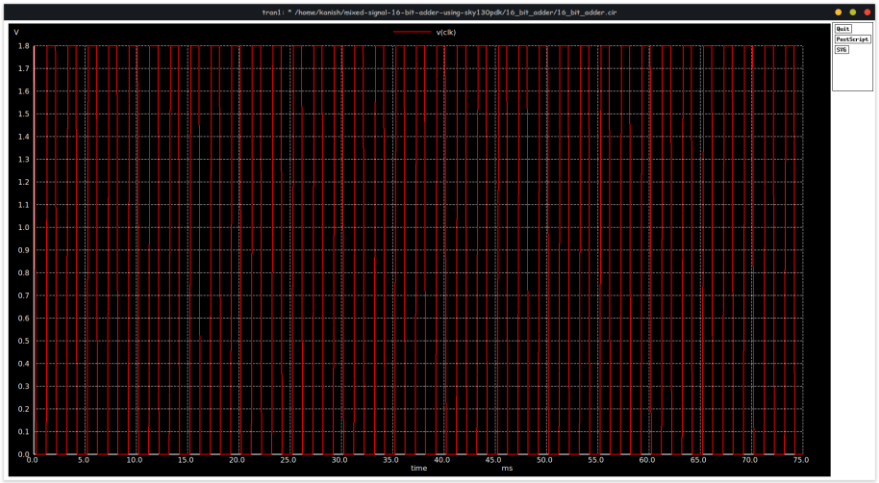


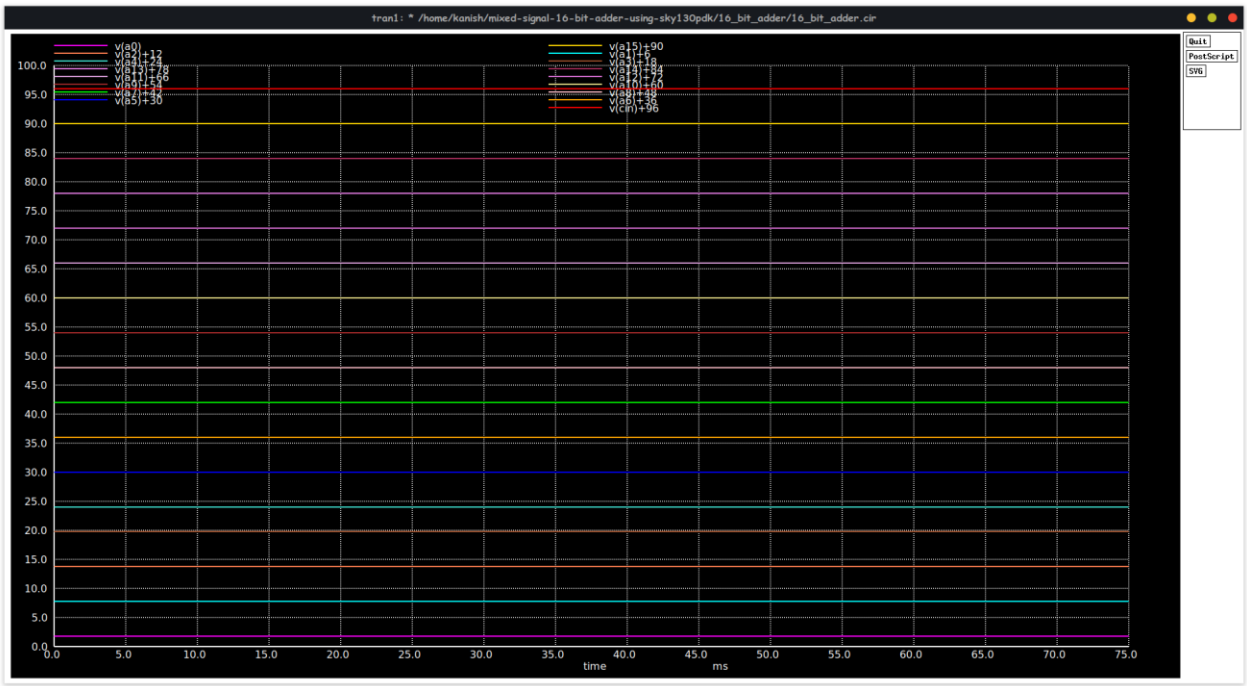
3. Mixed Signal 16 bit adder

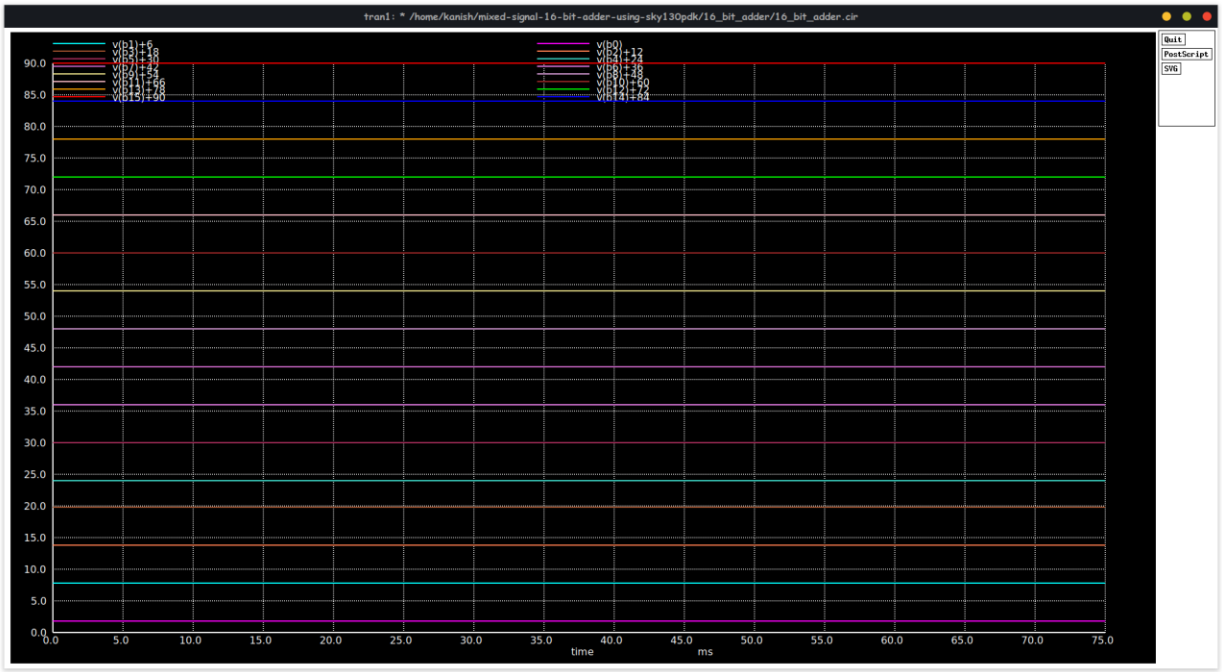


Simulation Results:

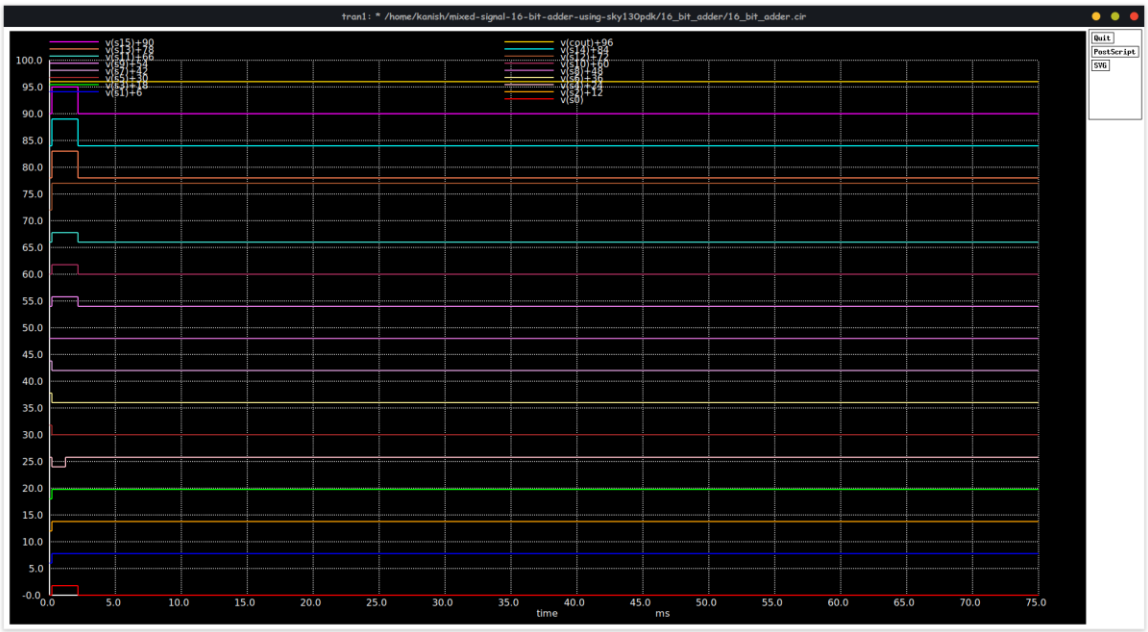
1. Inputs A, B, Cin and Clock







2. Output Sum and Cout



Conclusion:

Thus, we have implemented Mixed Signal 16 Bit Adder Using Sky130PDK in eSim and the appropriate waveforms are obtained.

References:

1. Morris Mano & Michael D Ciletti, “Digital Design: With an Introduction to Verilog HDL, 5th Edition, Pearson Education, 2013.
2. Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective
3. https://wrww.sciencedirect.com/topics/computer-science/master-slaveflip#:~:text=A%20negative%2Dedge%20triggered%20D,edge%20of%20the%20clock%20pulse.
4. https://skywater-pdk.readthedocs.io/en/main/