FET Based Master Slave Negative Edge Triggered Flipflop Using Sky130PDK

Theory:

A negative-edge triggered D type master-slave flip-flop consists of a pair of D-latches, positive latch (master) and negative latch (slave) connected in series. The latches are designed using mux by giving feedback from output to one of the inputs of 2:1 mux in. The mux is constructed using the transmission gates. The transmission gate is a bidirectional circuit which is made by connecting the pfet and nfet in parallel. The clock is given to the select lines of the mux so that the entire circuit behaves as the master slave negative edge triggered flipflop. During the high level of the clock, the master samples the input and the slave retains the previous output through feedback. At low level of the clock, the slave will go to transparent mode and samples the output of the master and the master will go to the hold mode, retaining the previous value. Thus, the output of master slave negative edge triggered flipflop changes once in one clock cycle during the high to low transition of clock. The transistors for designing all the circuits were used form the **SKY130PDK library** in eSim.

Schematic Diagram:

The circuit schematic of the FET based master slave negative edge triggered flipflop using sky130pdk in eSim is as shown below:

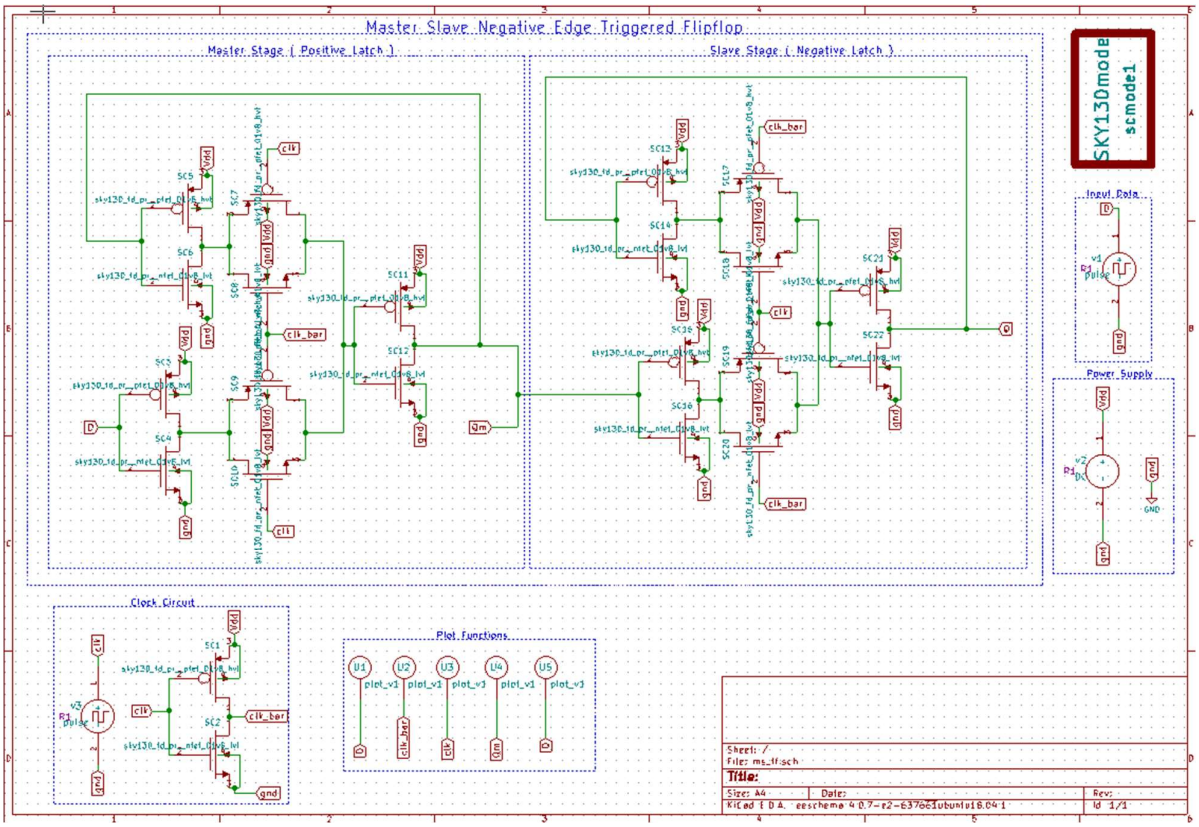

Figure 1: Schematic of the Master Slave Negative Edge Triggered Flipflop

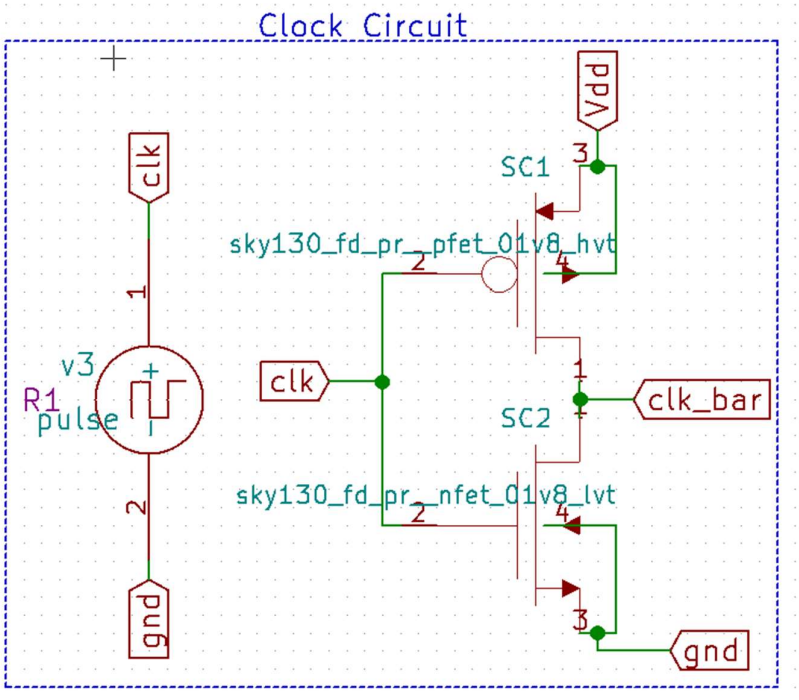

Figure 2: Clock Circuit

Simulation Results:

1. Ngspice Plots:

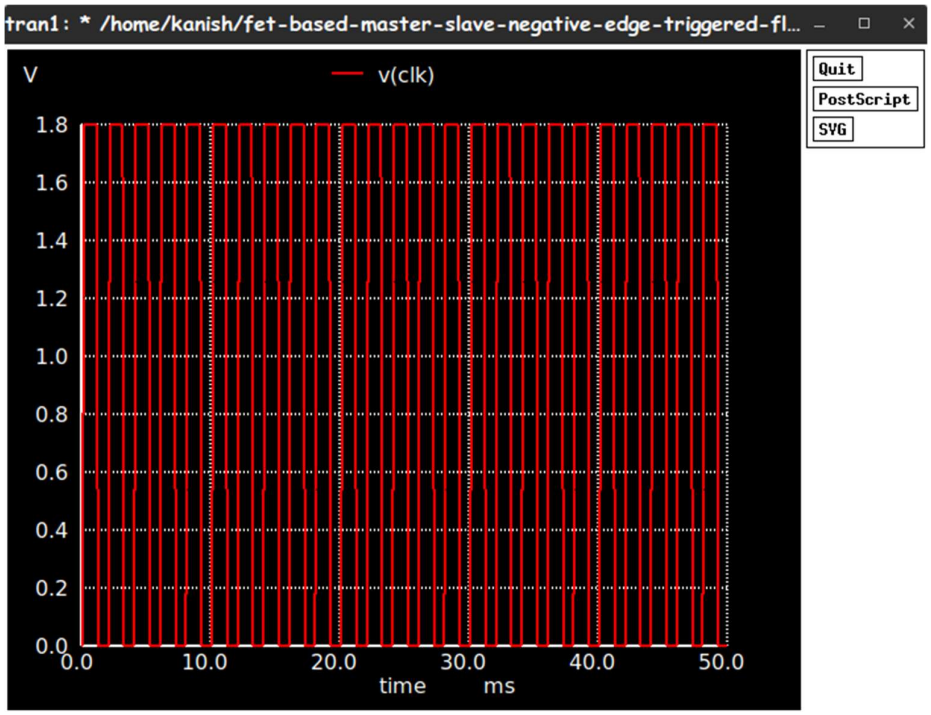

Figure 3: Clock Signal

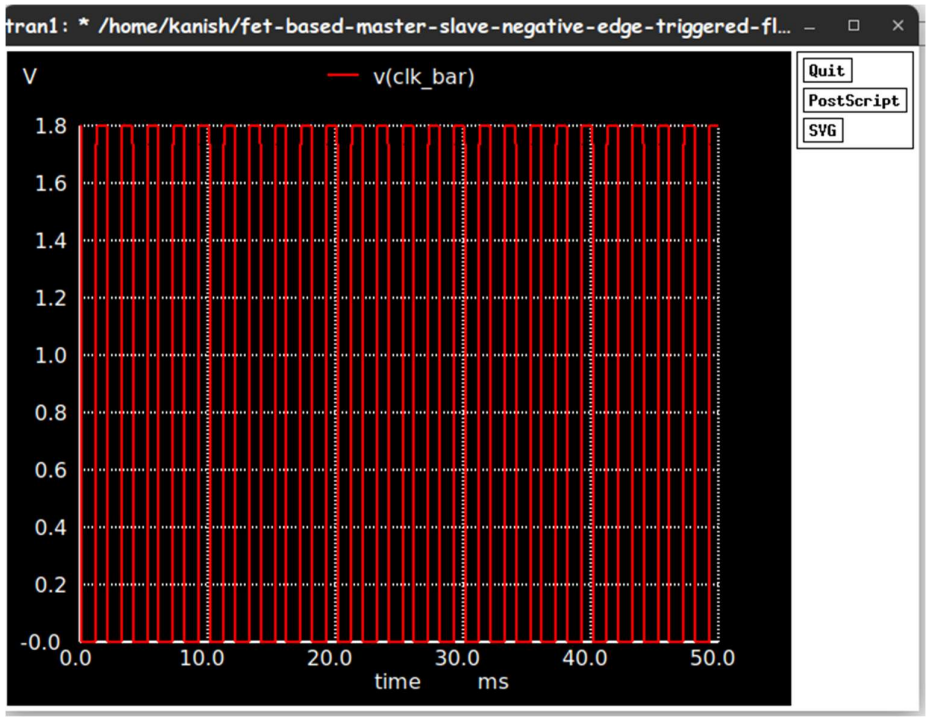

Figure 4: Clock bar Signal

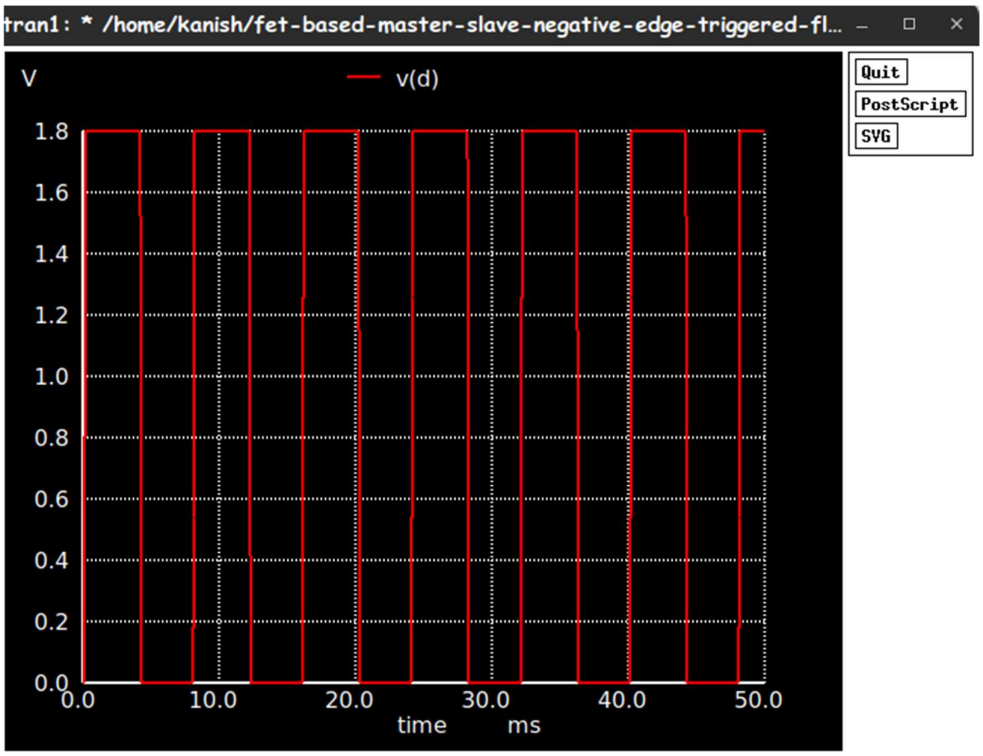

Figure 5: Input Data (D)

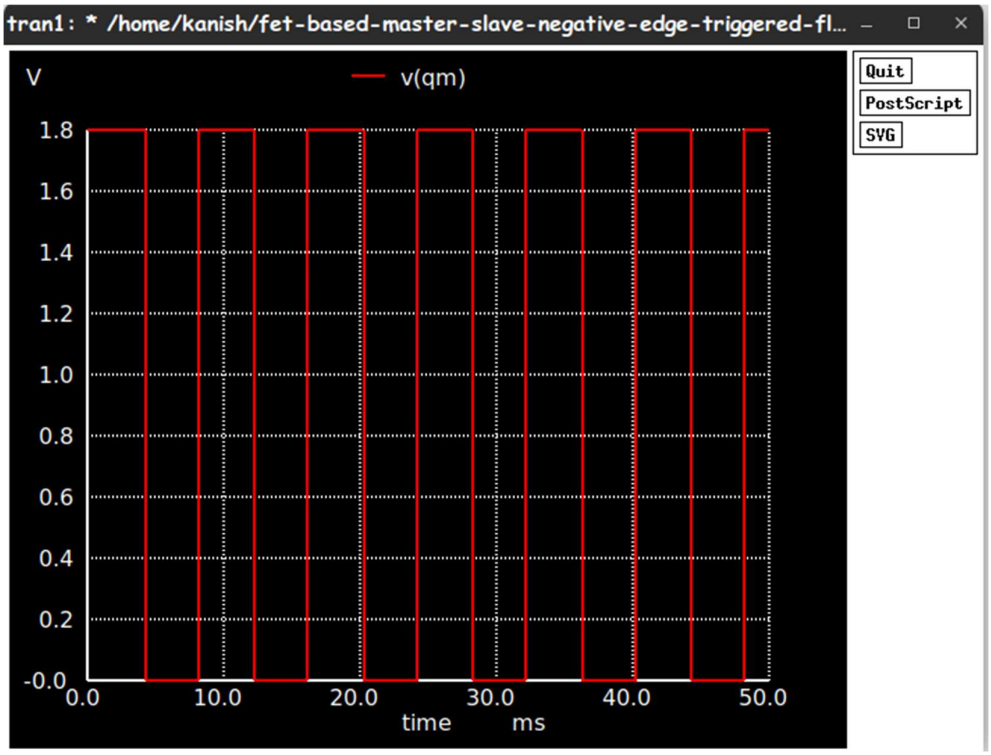

Figure 6: Master Output

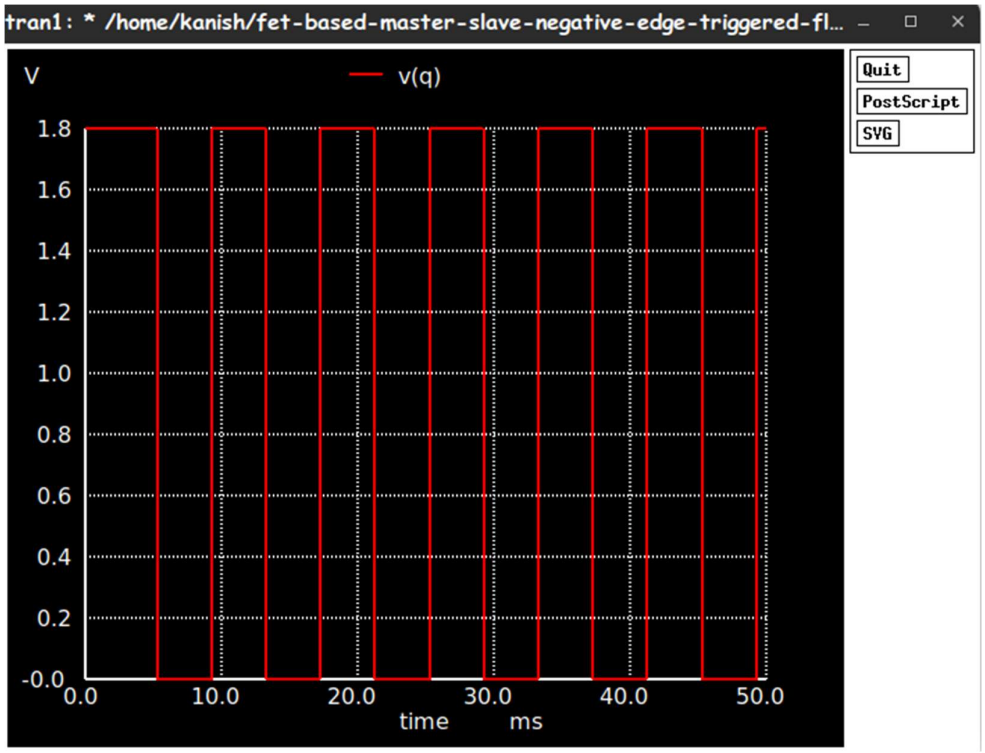

Figure 7: Master Slave Negative Edge Triggered Flipflop Output

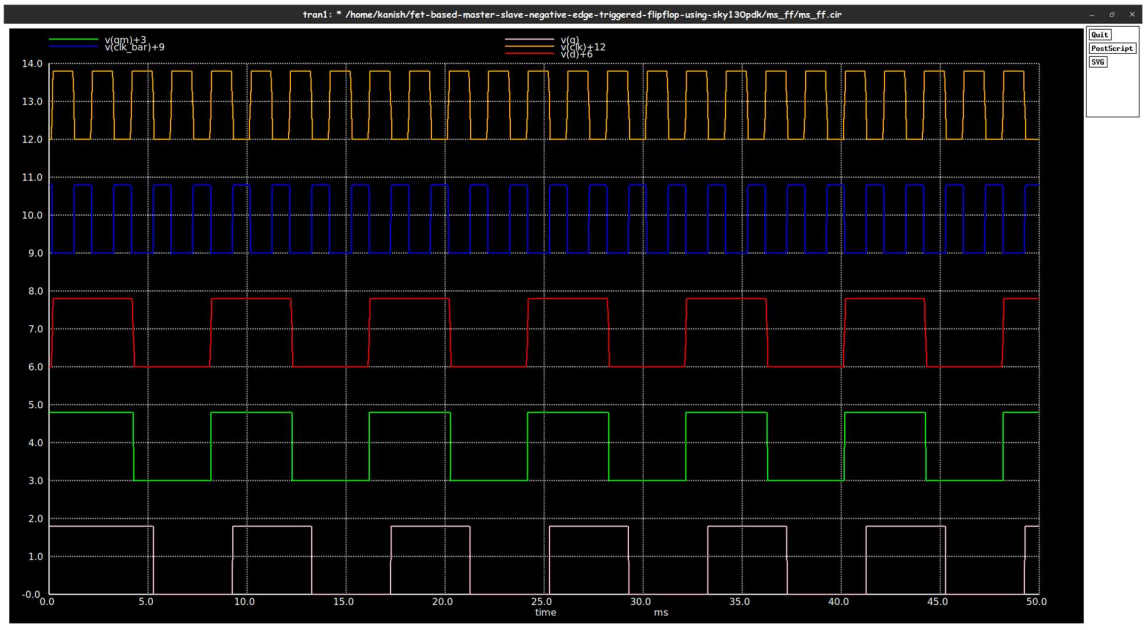

Figure 8: Combined Waveforms of the Master Slave Negative Edge Triggered Flipflop using SKY130PDK

2. Netlist

ms_ff.cir.out

```
* /home/kanish/fet-based-master-slave-negative-edge-triggered-flipflop-using-sky130pdk/ms_ff/ms_ff.cir
.include "/usr/share/local/sky130_fd_pr/models/sky130_fd_pr__model__linear.model.spice"
.include "/usr/share/local/sky130_fd_pr/models/sky130_fd_pr__model__diode_pd2nw_11v0.model.spice"
.lib "/usr/share/local/sky130_fd_pr/models/sky130.lib.spice" tt
.include "/usr/share/local/sky130_fd_pr/models/sky130_fd_pr__model__inductors.model.spice"
.include "/usr/share/local/sky130_fd_pr/models/sky130_fd_pr__model__diode_pw2nd_11v0.model.spice"
.include "/usr/share/local/sky130_fd_pr/models/sky130_fd_pr__model__r+c.model.spice"
.include "/usr/share/local/sky130_fd_pr/models/sky130_fd_pr__model__pnp.model.spice"
v2 vdd gnd  dc 1.8
v3  clk gnd pulse(0 1.8 0.1m 0.1m 0.1m 1m 2m)
xsc1 clk_bar clk vdd vdd sky130_fd_pr__pfet_01v8_hvt
xsc2 clk_bar clk gnd gnd sky130_fd_pr__nfet_01v8_lvt
xsc17 net-_sc17-pad1_ clk_bar net-_sc13-pad1_ vdd sky130_fd_pr__pfet_01v8_hvt
xsc19 net-_sc17-pad1_ clk net-_sc15-pad1_ vdd sky130_fd_pr__pfet_01v8_hvt
xsc7 net-_sc10-pad3_ clk net-_sc5-pad1_ vdd sky130_fd_pr__pfet_01v8_hvt
xsc9 net-_sc10-pad3_ clk_bar net-_sc10-pad1_ vdd sky130_fd_pr__pfet_01v8_hvt
xsc8 net-_sc5-pad1_ clk_bar net-_sc10-pad3_ gnd sky130_fd_pr__nfet_01v8_lvt
xsc10 net-_sc10-pad1_ clk net-_sc10-pad3_ gnd sky130_fd_pr__nfet_01v8_lvt
xsc18 net-_sc13-pad1_ clk net-_sc17-pad1_ gnd sky130_fd_pr__nfet_01v8_lvt
xsc20 net-_sc15-pad1_ clk_bar net-_sc17-pad1_ gnd sky130_fd_pr__nfet_01v8_lvt
xsc4 net-_sc10-pad1_ d gnd gnd sky130_fd_pr__nfet_01v8_lvt
xsc3 net-_sc10-pad1_ d vdd vdd sky130_fd_pr__pfet_01v8_hvt
xsc6 net-_sc5-pad1_ qm gnd gnd sky130_fd_pr__nfet_01v8_lvt
xsc5 net-_sc5-pad1_ qm vdd vdd sky130_fd_pr__pfet_01v8_hvt
xsc11 qm net-_sc10-pad3_ vdd vdd sky130_fd_pr__pfet_01v8_hvt
xsc12 qm net-_sc10-pad3_ gnd gnd sky130_fd_pr__nfet_01v8_lvt
xsc21 q net-_sc17-pad1_ vdd vdd sky130_fd_pr__pfet_01v8_hvt
xsc22 q net-_sc17-pad1_ gnd gnd sky130_fd_pr__nfet_01v8_lvt
xsc15 net-_sc15-pad1_ qm vdd vdd sky130_fd_pr__pfet_01v8_hvt
xsc16 net-_sc15-pad1_ qm gnd gnd sky130_fd_pr__nfet_01v8_lvt
xsc13 net-_sc13-pad1_ q vdd vdd sky130_fd_pr__pfet_01v8_hvt
xsc14 net-_sc13-pad1_ q gnd gnd sky130_fd_pr__nfet_01v8_lvt
v1  d gnd pulse(0 1.8 0.1m 0.1m 0.1m 4m 8m)
* u1  d plot_v1
* u2  clk_bar plot_v1
* u3  clk plot_v1
* u4  qm plot_v1
* u5  q plot_v1
* s c m o d e
.tran 1e-03 50e-03 0e-00
* Control Statements
.control
run
print allv > plot_data_v.txt
print alli > plot_data_i.txt
plot v(d)+6 v(clk_bar)+9 v(clk)+12 v(qm)+3 v(q)
write ms_ff.raw all
.endc
.end
```

Save and Exit

Figure 9: Netlist

3. GAW - Gtk Analog Wave viewer Plot

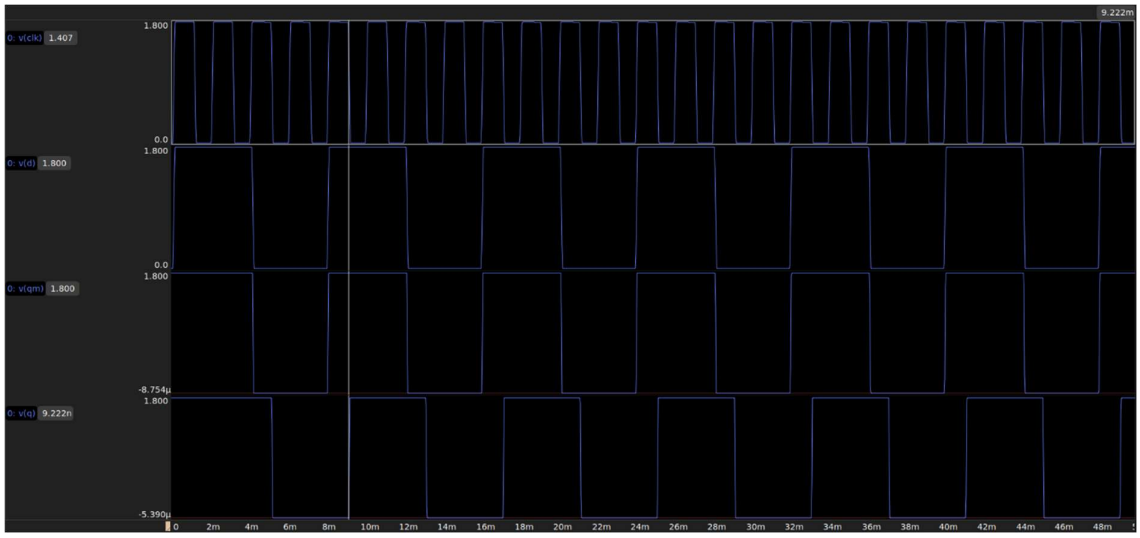

Figure 10: Combined Waveform in GTK Analog Viewer

Conclusion:

Thus, we have implemented the FET based master slave negative edge triggered flipflop using Sky130PDK in eSim and the appropriate waveforms are obtained.

References:

1. Morris Mano & Michael D Ciletti, "Digital Design: With an Introduction to Verilog HDL, 5th Edition, Pearson Education, 2013
2. Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective.
3. https://www.sciencedirect.com/topics/computer-science/master-slave-flip#:~:text=A%20negative%2Dedge%20triggered%20D,edge%20of%20the%20clock%20pulse.
4. https://skywater-pdk.readthedocs.io/en/main/