Design And Implementation Of Radiation-Hardened SRAM:

Theory:

A Radiation –Hardened SRAM is a Circuit with has High Tolerance to Noises By adding redundant Transistors. In the Figure 1 Shown below the Transistors “SC1” and “SC14” are controlled by a Word line (wl), are pass Transistors for access, which controls the connection between Bit lines(BL and BLBar) at the Storage Nodes q and qb. The Nodes q1 and q1b are redundant nodes i.e of the Stored value is “1” then logic values at q,qb,q1 and q1b are “1”,”0”,”1” and “0”. The Transistors SC10 and SC5 are Pre-charge Transistors. Assume Initially write is enabled Q=”1” and QL=”0” and BL=”0” and BLBar=”1”;Then the Values in “Q” and “QL” Changed to “0” and “1”. After that, once WL is discharged to “0,” the new state of the memory cell is stored. And When in read mode the Transistors the Bit Lines BL and BLBar are Pre-Charged to ‘1’.And When the Write line WL is Activated the SC1 and SC14 are Pulled High and BLBar is Discharged through the transistors SC9 and SC14. As a result, the differential voltage of the BLs will be generated and amplified by the sense amplifier.

Schematic Diagram:

The Schematic Diagram of Rad-Hard 14T SRAM:

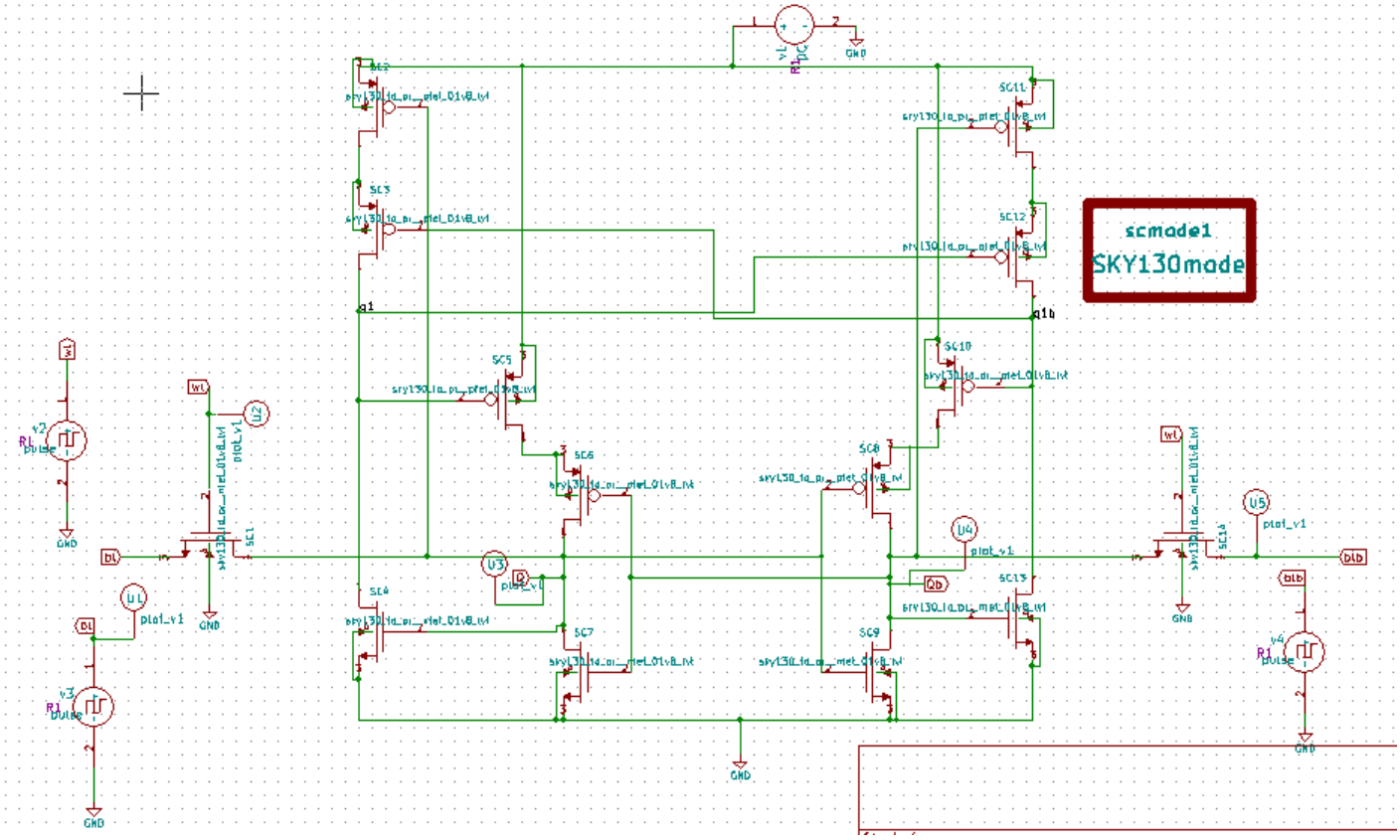

Figure 1: Schematic Diagram

Simulation Results:

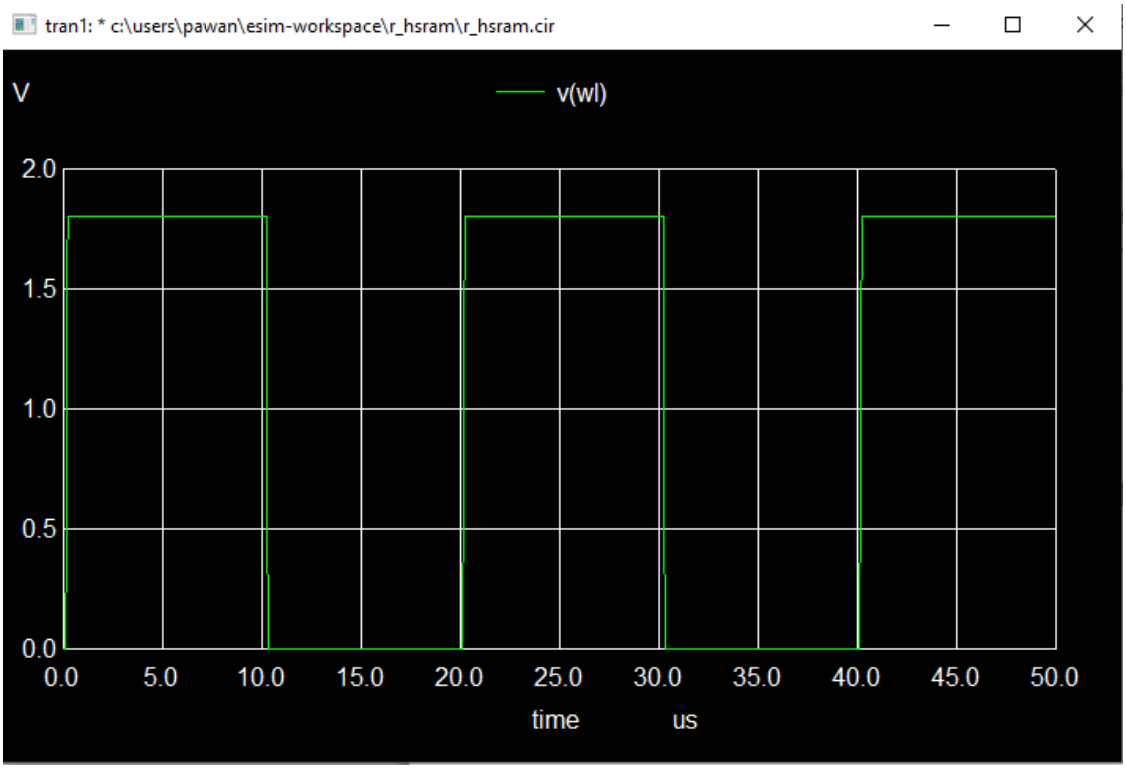

Figure 2:Write Line

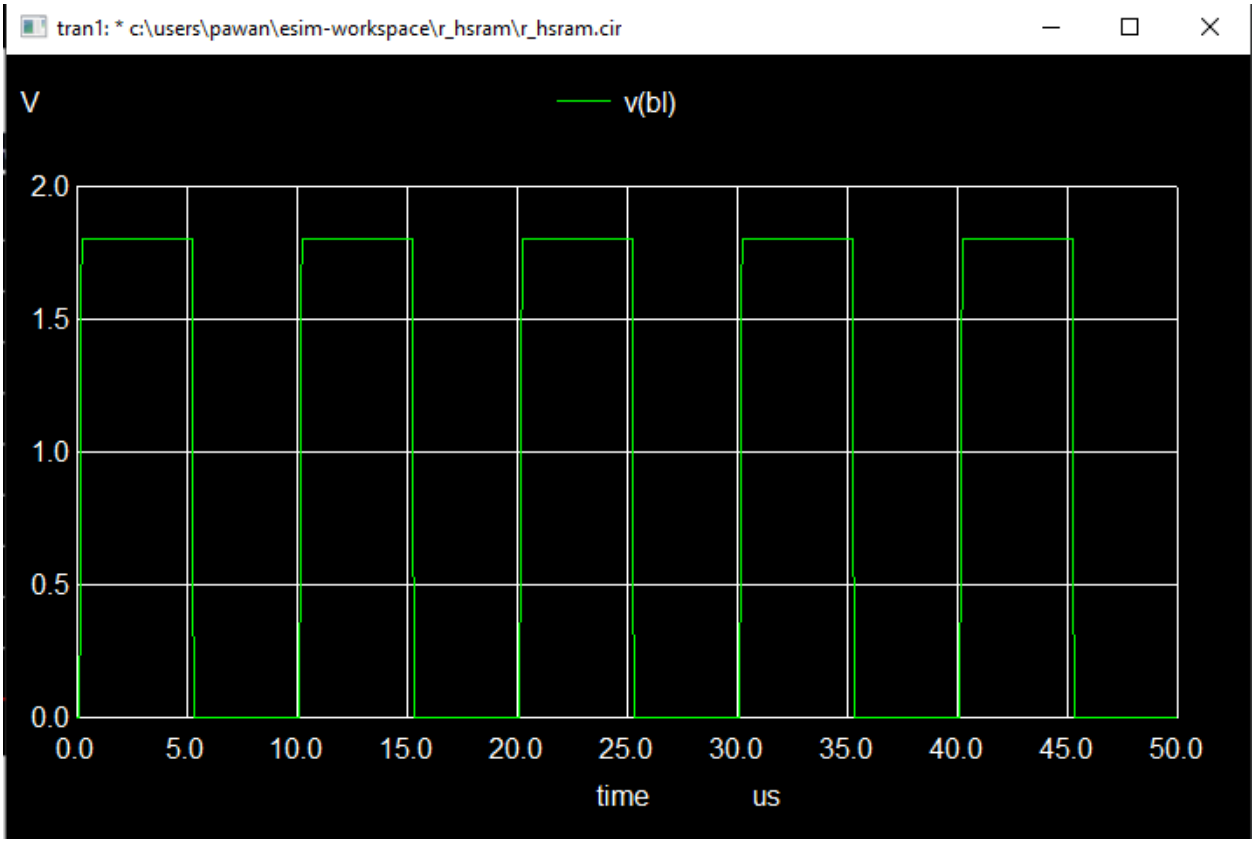

Figure 3:Bit Line

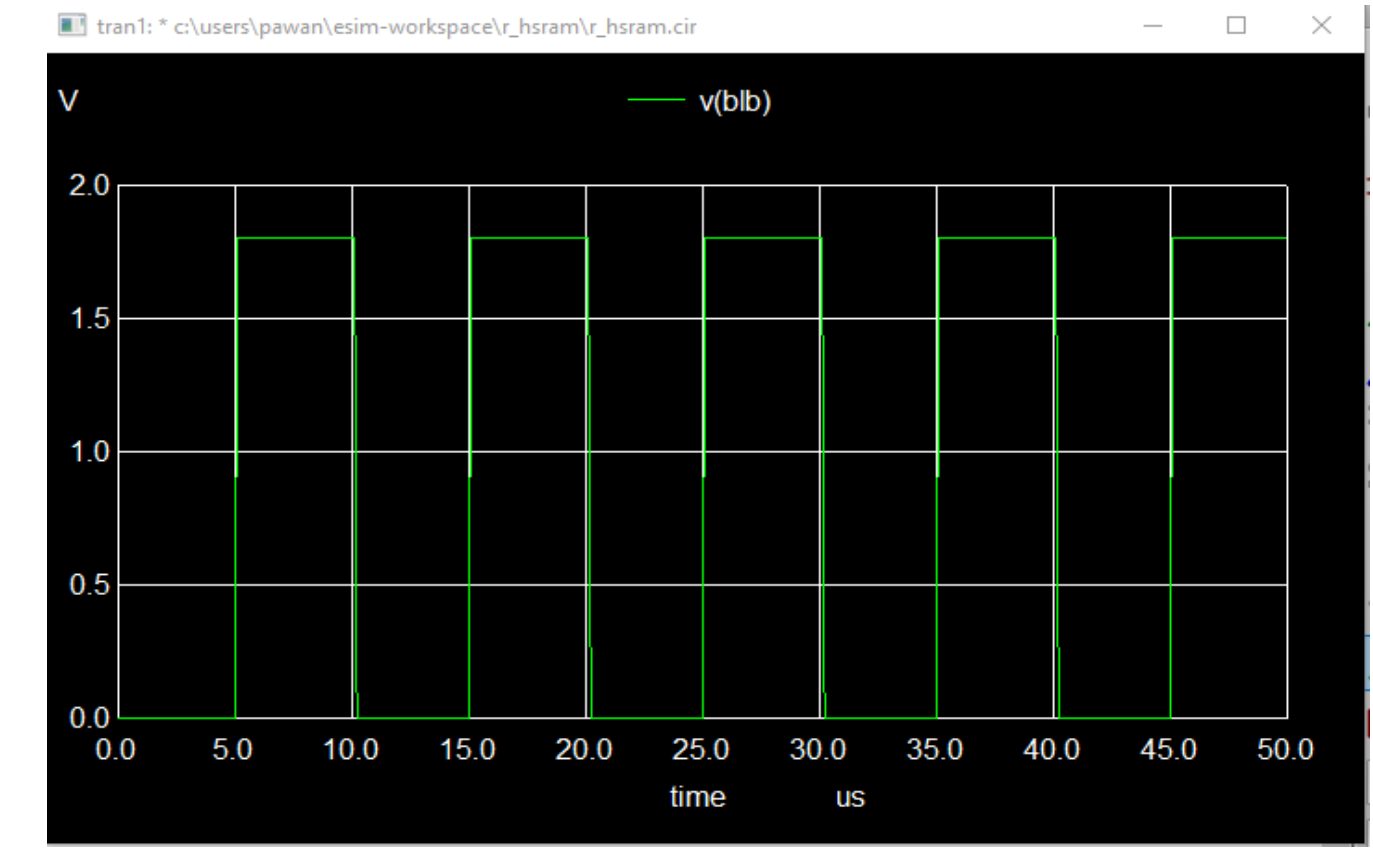

Figure 4:Bit Line Bar

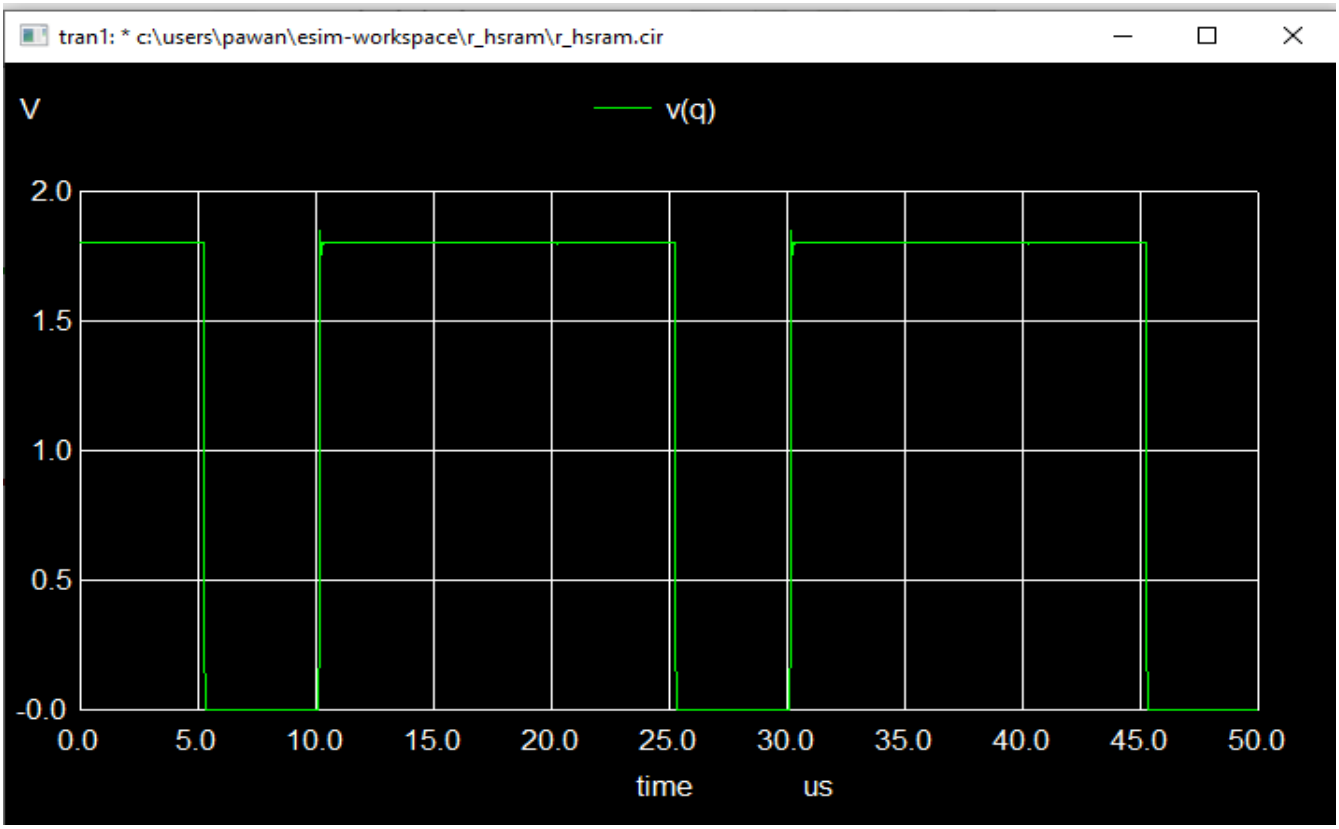

Figure 4: Q Output Bit

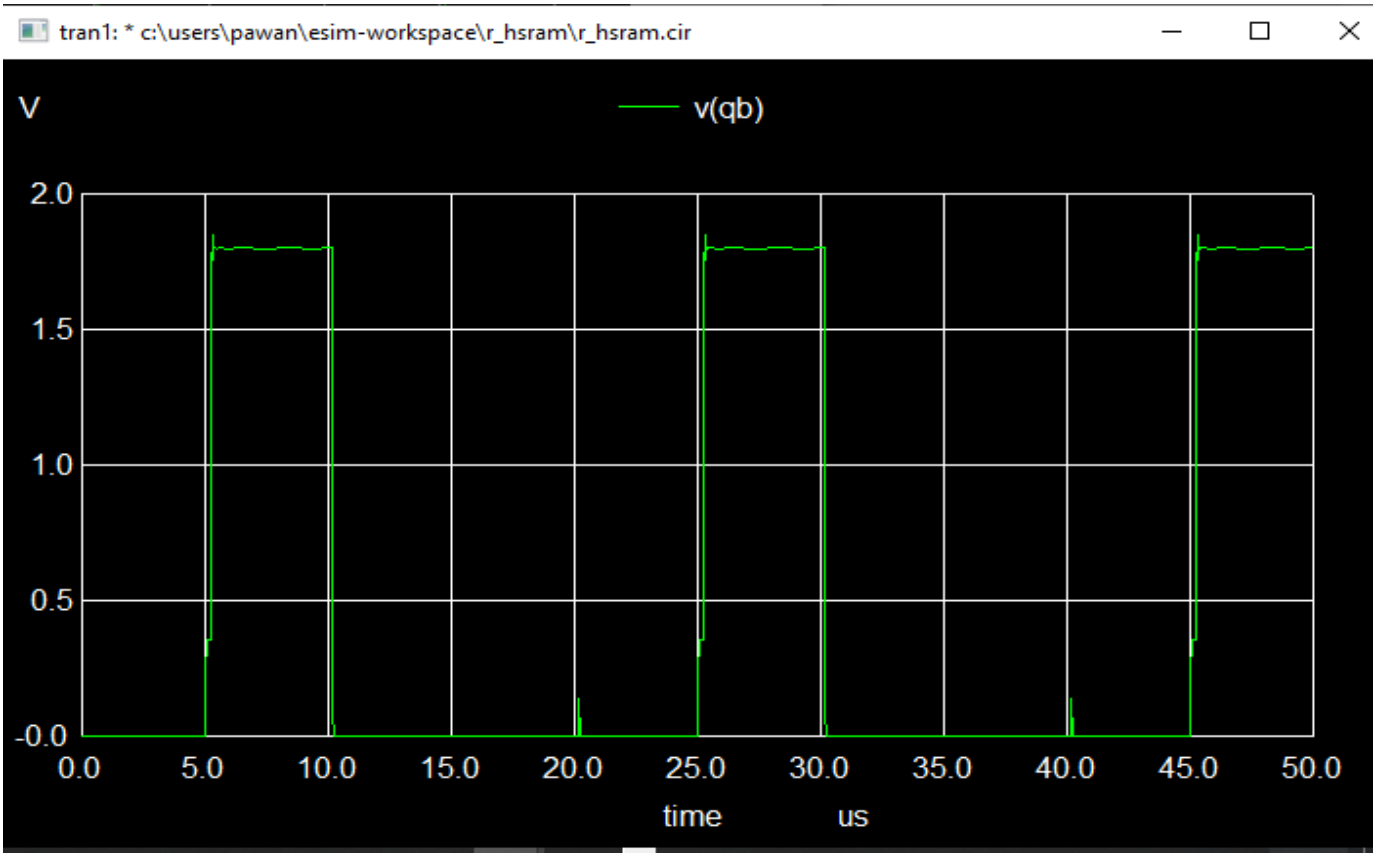

Figure 6: Qb Output Bit

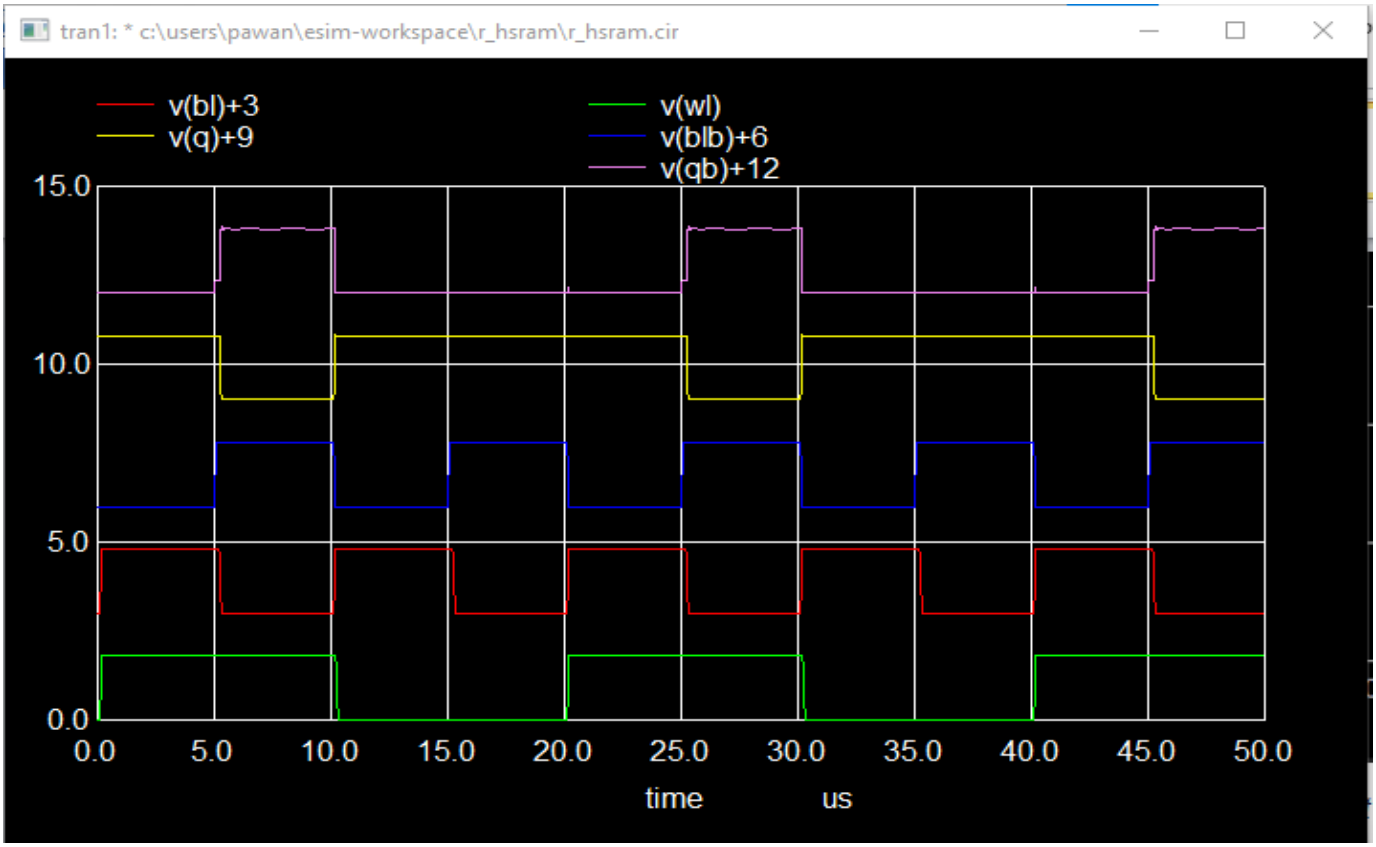

Figure 7:Combined Ouput..

Conclusion :

Thus ,we have Designed and Analysed the Radiation Hardened 14T SRAM using eSim and get the approximate waveforms.

References:

"*Radiation-Hardened 14T SRAM Bitcell With Speed and Power Optimized for Space Application*" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.