Title:

Implementation OF 4-bit Binary Counter Mixed-Signal Circuit performed in eSim

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ABSTRACT

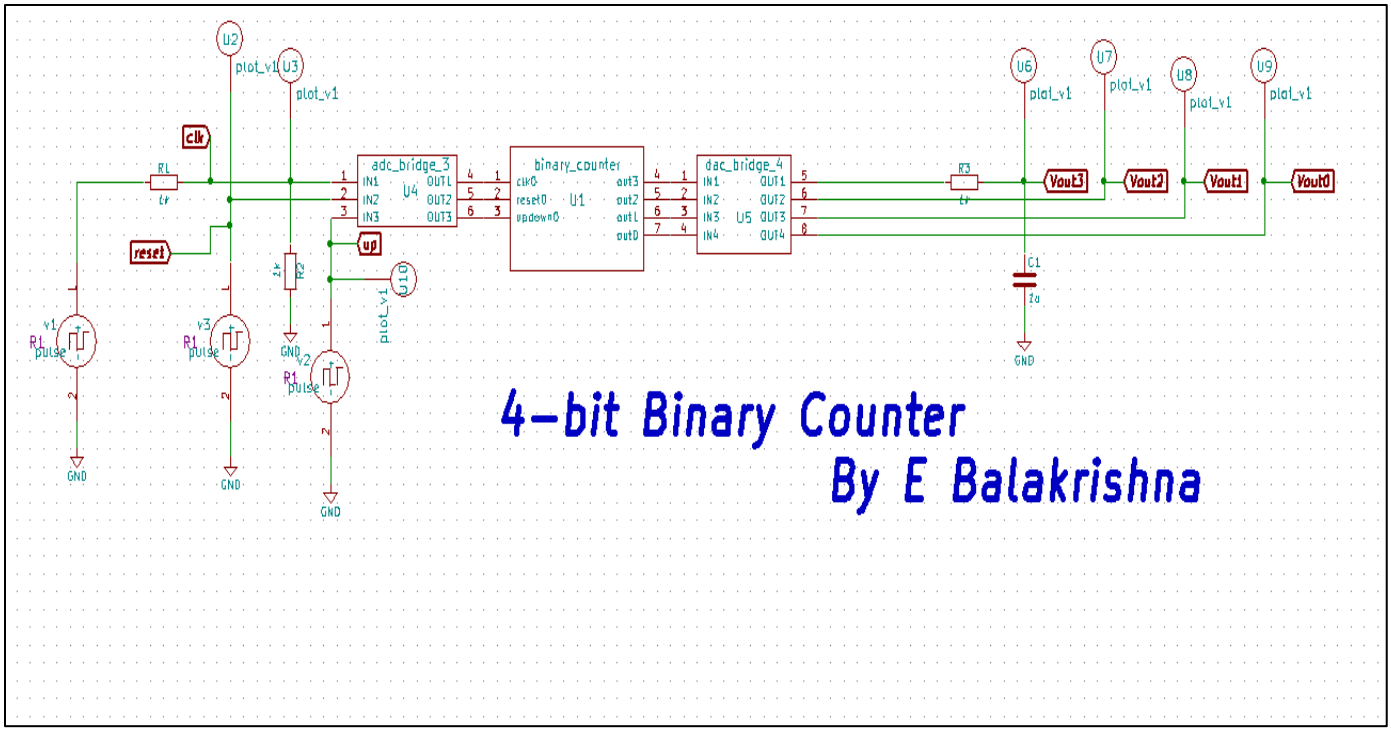
Counter is one of the essential and important additives utilized in maximum of the digital devices. Design of electricity green counter design has come to be important for the researchers. It is widely used in LED lightning, in LED watches that is digital watches. The block of 4-bit binary counter using makerchip and Ngveri tool will be created using behavioral model of Verilog which convert the Verilog code into the respective block or circuit block of binary counter. The proposed design of counter is implemented using eSim tool which is an open source, EDA Tool.

Theory

A sequential circuit that is going via a prescribed series of states upon the utility of clock or enter pulses is referred to as a counter. In a counter, the series of states may also observe a binary rely or every other series of states. A counter that follows the binary series is referred to as a binary counter. An counter encompass n-turn flops and may rely in binary from zero to 2^(n)-1. For example: 4bit binary counter. We design a 4-bit binary counter. Our counter has an output “Vout” with 4 bits. During accurate operation, the counter begins off evolved at “0000” after which binary counts as much as output “0001”, “0010”, “0011”, and so forth till it outputs “1111”, and then it resets to “0000” and begins off evolved again. The implementation of our 4bit binary counter has simplest one input: a clock sign Clk. The clock sign is supplied with the aid of using the external (to the FPGA) clock generator. We use the output Q to power the primary 4 LEDs ON THE Development board.

The block diagram of the simplest/primary structural implementation of this type of binary counter is proven in the subsequent figure. This implementation is referred to as a ripple counter.

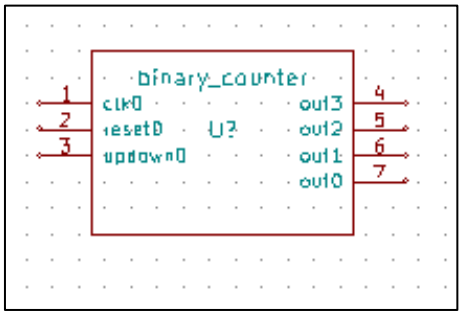
Schematic Diagram



Verilog Behavioral Code of Binary Counter

```
module binary_counter (input clk,
                       input reset,
                       input updown,
                       output reg[3:0] out);

// This always block will be triggered at the rising edge of clk (0->1)
// It checks if the reset is 0, then change out to zero
// It checks if reset is 1, then the design should be allowed to count updown, so increment and decrement the counter

  always @ (posedge clk) begin
    if (reset)
      out <= 0;
    else
       if(updown==1)
```

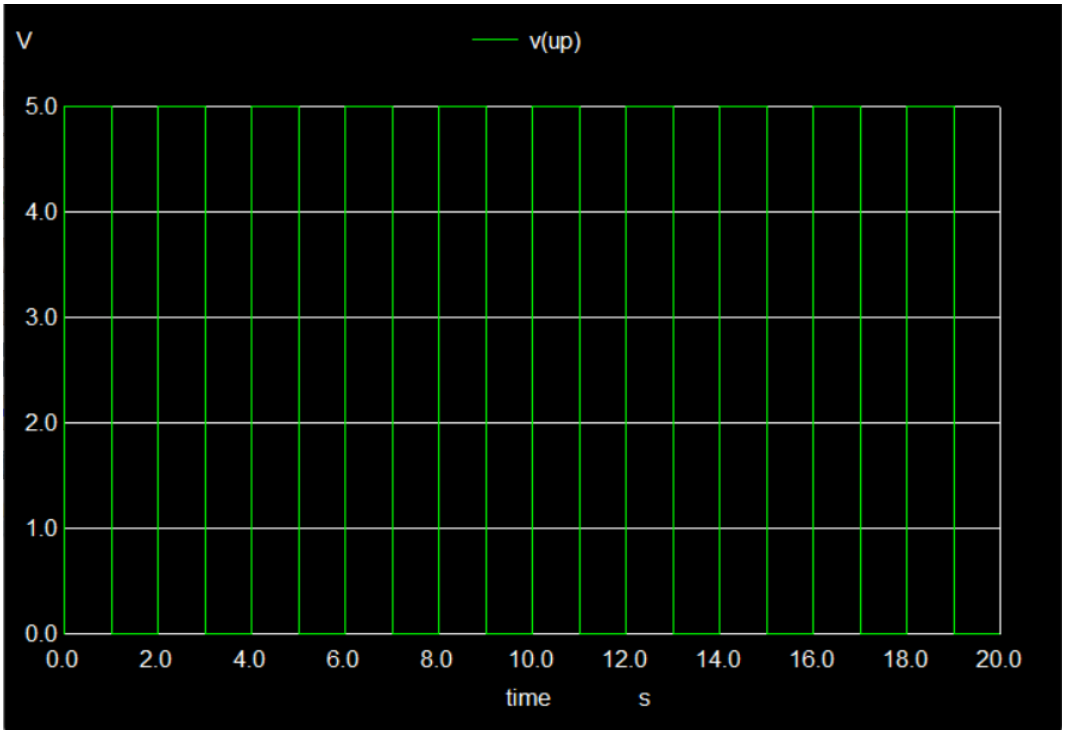
```
        if(out==15)
            out <= 0;
        else
// Here, value increment by 1 for up counter

            out <= out + 1;
      else
        if(out==0)
            out<=15;
        else
// Here, value decrement by 1 for down counter

            out<= out-1;
  end
endmodule
```

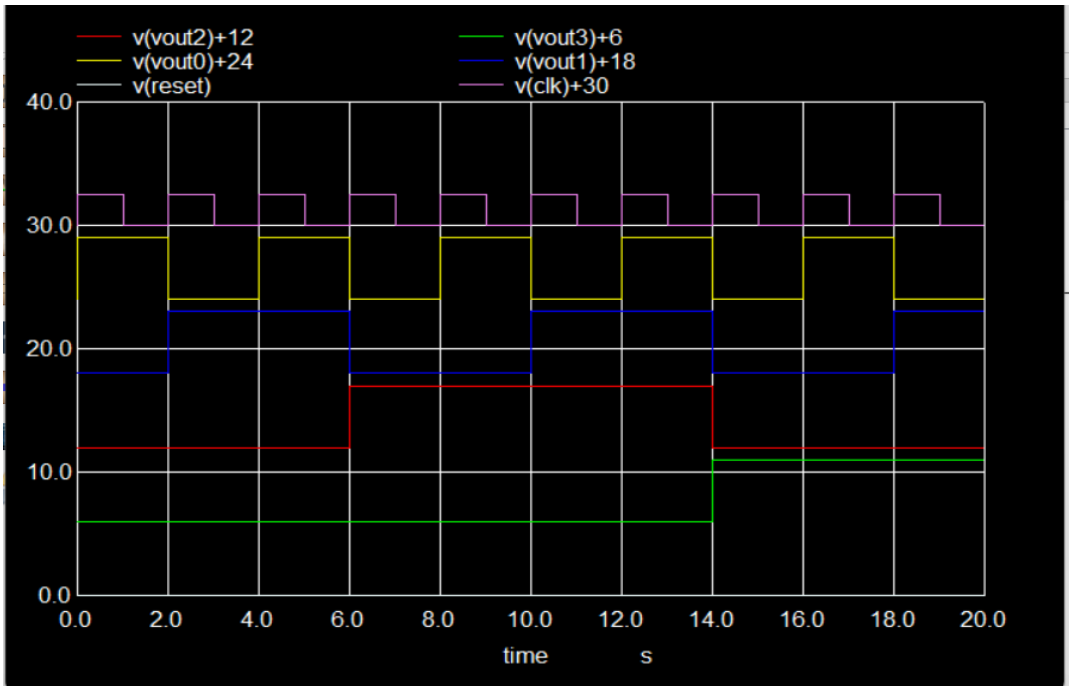


Simulations

In the given simulation, it is performing UP counting it means that this binary counter behaves as a UP counter.

Ngspice plot waveform





Result

Simulation of 4 bit binary counter mixed signal circuit is performed at 20 sec by performing transient analysis.

Conclusion

Hence, the implementation of 4-bit binary counter has been successfully created and simulated and it's waveform has also been verified respectively.

References

1. http://www.ijcttjournal.org/2017/Volume50/number-2/IJCTT-V50P118.pdf
2. https://www.ti.com/lit/ds/symlink/sn74hc163-q1.pdf?ts=1649877482086&ref_url=https%253A%252F%252Fwww.google.com%252F