Title:

Design and Implementation of 4-bit Magnitude Comparator Mixed Signal Circuit performed in eSim

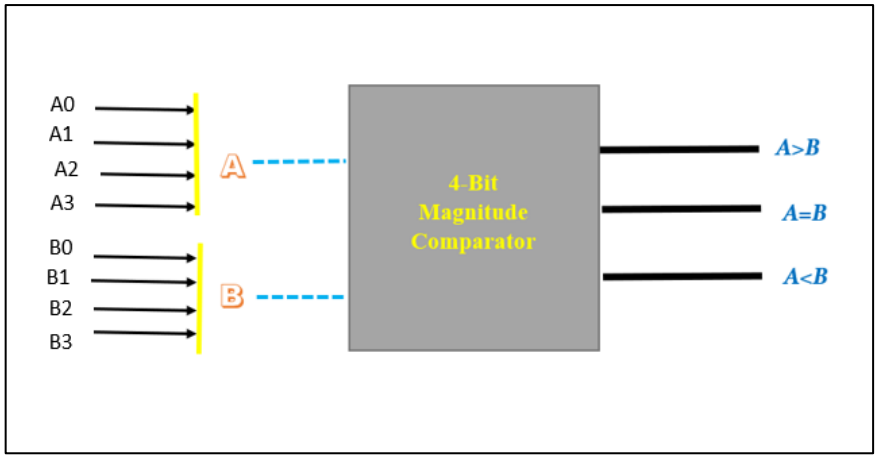
Abstract:

This paper presents design and implementation of 4 bit magnitude comparator mixed signal circuit . A Verilog code in behavioral mode (also known as RTL code) is used to create the block of 4 bit magnitude comparator using makerchip and ngveri tool which convert the verilog code into block. The proposed design of comparator is implemented in eSim tool which is an EDA Tool.

Keyword-RTL , Behavioral, mixed signal circuit, magnitude comparator, eSim, ngveri , makerchip , EDA Tool.

Theory:

A comparator is a circuit which compares the two values. A Magnitude Comparator is a combinational circuit which compares the magnitude of two binary numbers .It determine whether a number is greater than, less than or equal to, by comparing the magnitudes of both the numbers. It is mostly used inside arithmetic operations basically in ALU(Arithmetic and Logic unit) which is situated inside CPU(Central Processing Unit). Generally if two n-bit number has to be compared then the given circuit has 2^{2n} total conditions. For example – if there are 2 bit number , there will be 4 input and 16 rows in the truth table , similarly In this given circuit , if the number of bit in each number is 4 then , it is 4 bit magnitude comparator which means that it has 8 input and total of 3 output that is greater than(A>B), less than(A<B) and equal to(A=B) if A and B be two binary numbers. Let suppose that there are 2 number A and B and each have 4 bit A0,A1,A2,A3 and B0,B1,B2,B3. Now, 4 bit magnitude comparator compares the magnitude of both number and provide the output accordingly that whether (A>B) or (A<B) or (A=B).



For equality Condition we use xNor gate . the two binary number will be equal if and only if each of the corresponding bits of both A and B are equal .

→FOR A=B,

(A3 Exnor B3)(A2 Exnor B2)(A1 Exnor B1)(A0 Exnor B0)

This is the equation of Equality

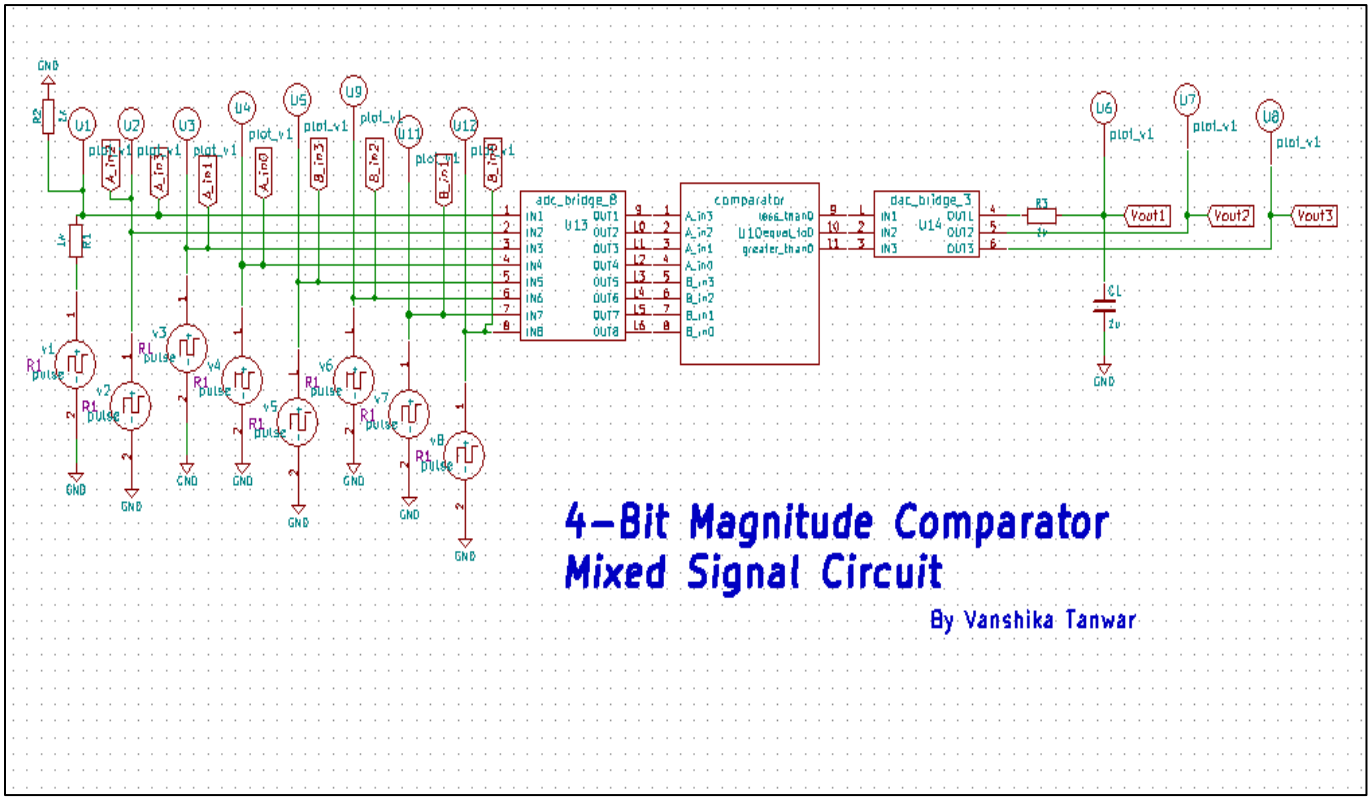
→For greater than or less than process we should have to follow these steps :

1. If in case A3=1 and B3=0 , then it means that A>B.
2. If in case A3=0 and B3=1 , then it means that A<B.
3. If in case A3=1 and B3=1 (or) A3=0 and B3=0 that is A3+B3 , then it means that now we need to go to step 1 and compare the next lower bit which is lower than MSB i.e. , A2 and B2 and in the similar way we need to compare the next further bit accordingly by following the above step process till it reaches to A0 and B0.(or till it reaches to the LSB).

Below , is the basic logic truth table of magnitude comparator

A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Schematic Diagram



Verilog code of Comparator:

Verilog Behavioral module-

```
//**************************************
// Vanshika Tanwar
//Verilog file: comparator.txt
//**************************************
module comparator(
A_in,    //Input A
B_in,          //Input B
less_than,      //When A is less than B, it is high
equal_to,       //When A is equal to B, it is high
greater_than    //When A is greater than B, it is high
);
                        //Declaration of Input Ports.
  input [3:0] A_in;
  input [3:0] B_in;
                       //Declarations of Output Ports.
  output less_than;
  output equal_to;
  output greater_than ;
                                //Internal variables
                                  //reg declarations
   reg less_than;
   reg equal_to;
   reg greater_than;
                                    //When the inputs  A or B are changed then execute this block
  always @(A_in or B_in)
 begin
                                //This block checks if A is Greater than B, Greater than is high
    if(A_in > B_in)
```

```
        begin
                less_than = 4'b0;
                equal_to =4'b0;
                greater_than = 4'b1;
        end
                                        //This block checks if A is equal to B, Equal to is high
    else if(A_in == B_in)
        begin
                less_than = 4'b0;
                equal_to = 4'b1;
                greater_than = 4'b0;
        end
                                //Otherwise -This block checks for A less than B, Less than is high
    else
        begin
                less_than = 4'b1;
                equal_to = 4'b0;
                greater_than =4'b0;
        end
end
    //End of a module
Endmodule
```

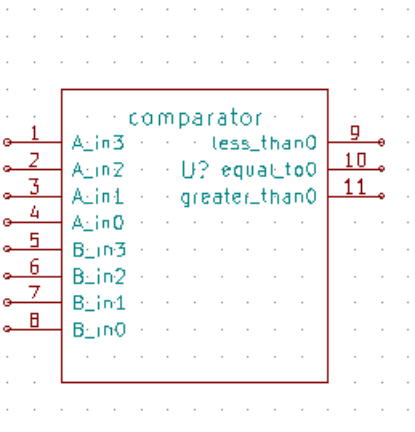


Fig. View of Comparator Block created in e Sim using Verilog code.

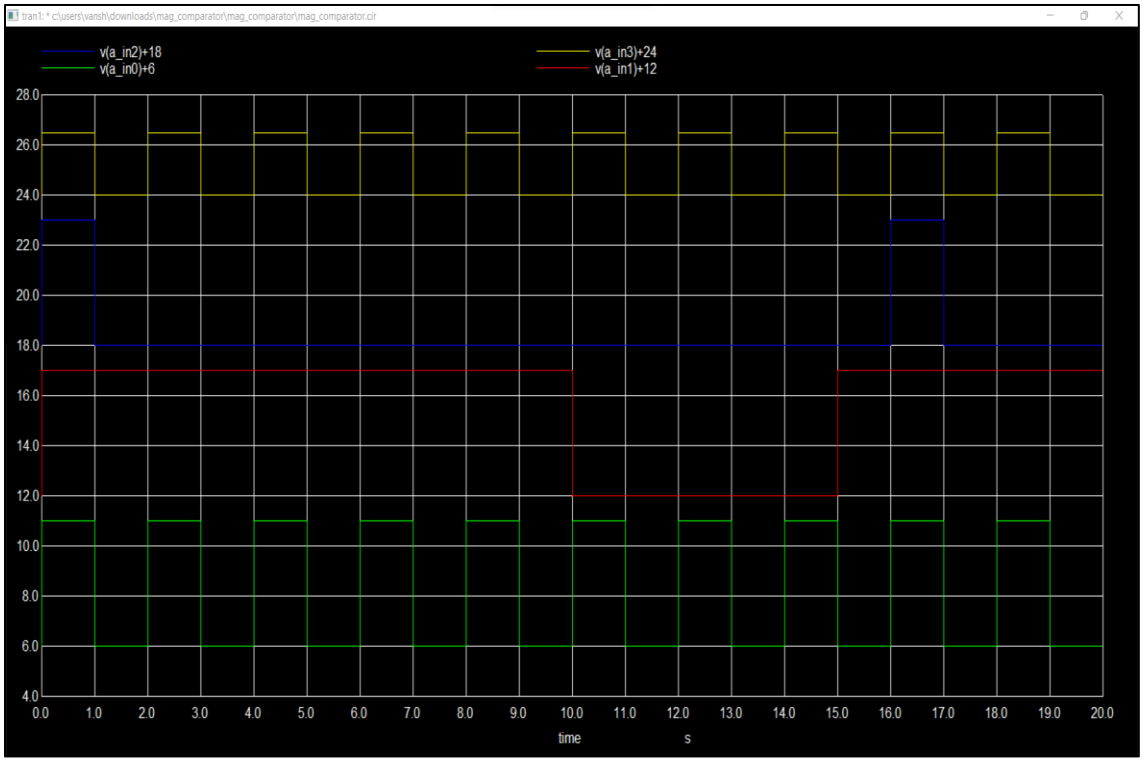
Result:

The final simulated result has been obtained by performing transient analysis at 20 sec.

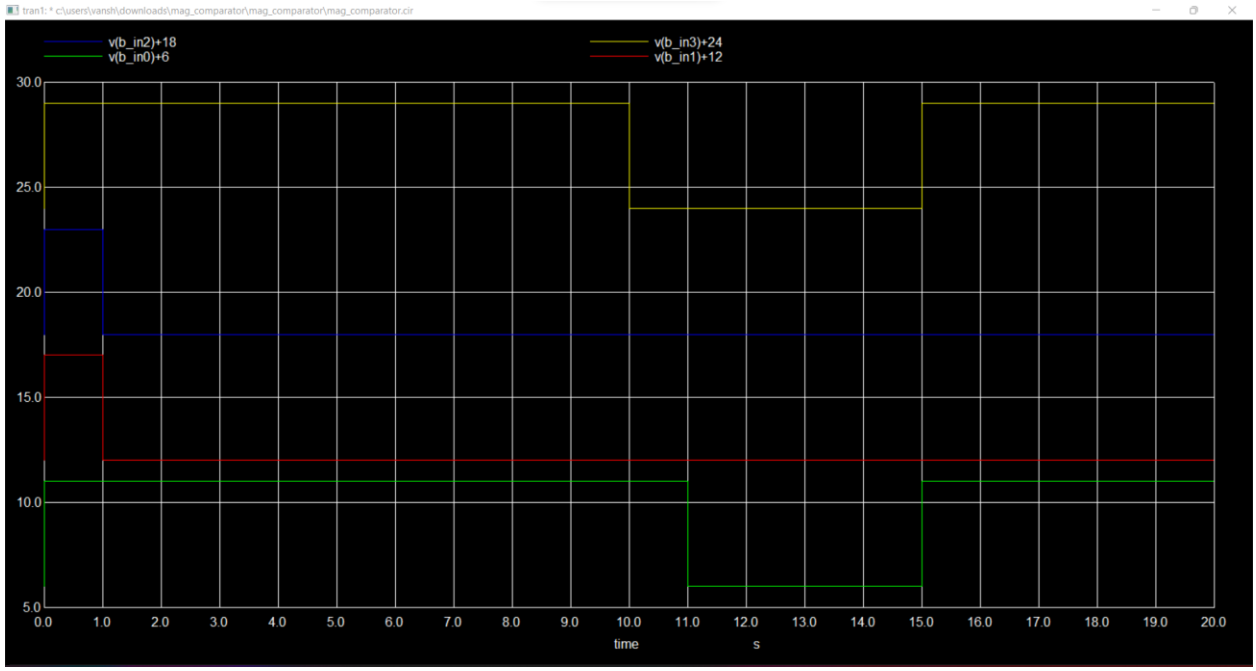
Output Waveform:

➔ ***NgSpice Plot***

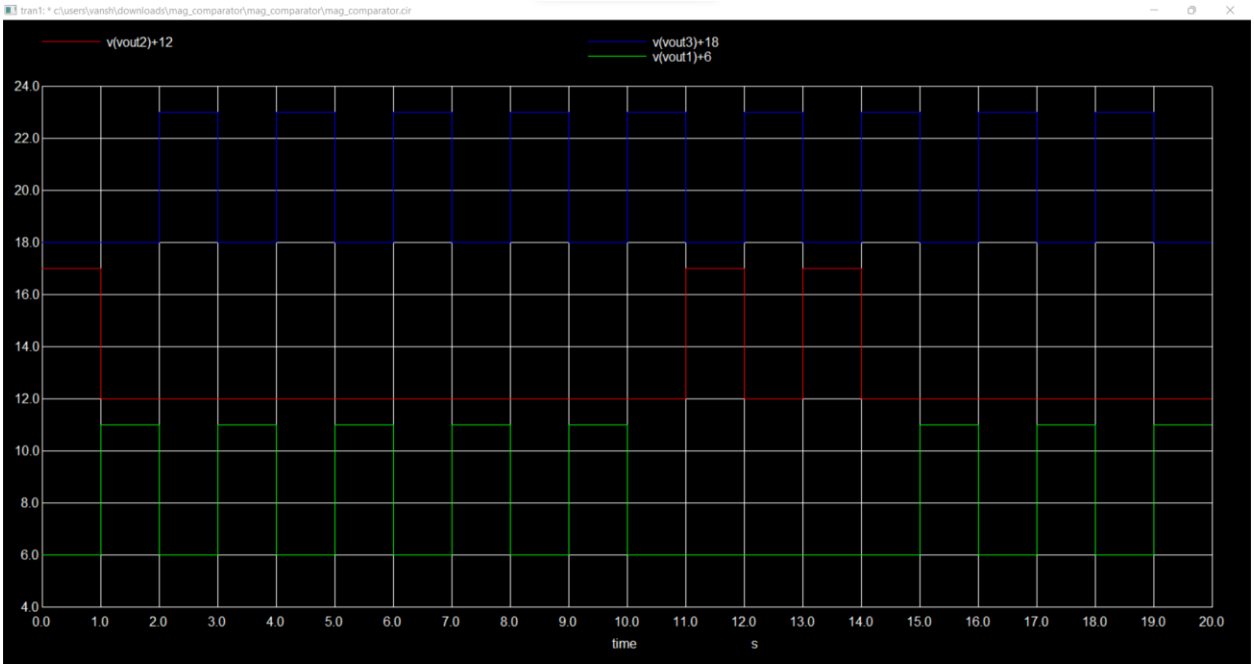
1. Ngspice plot of A input (A0,A1,A2,A3)



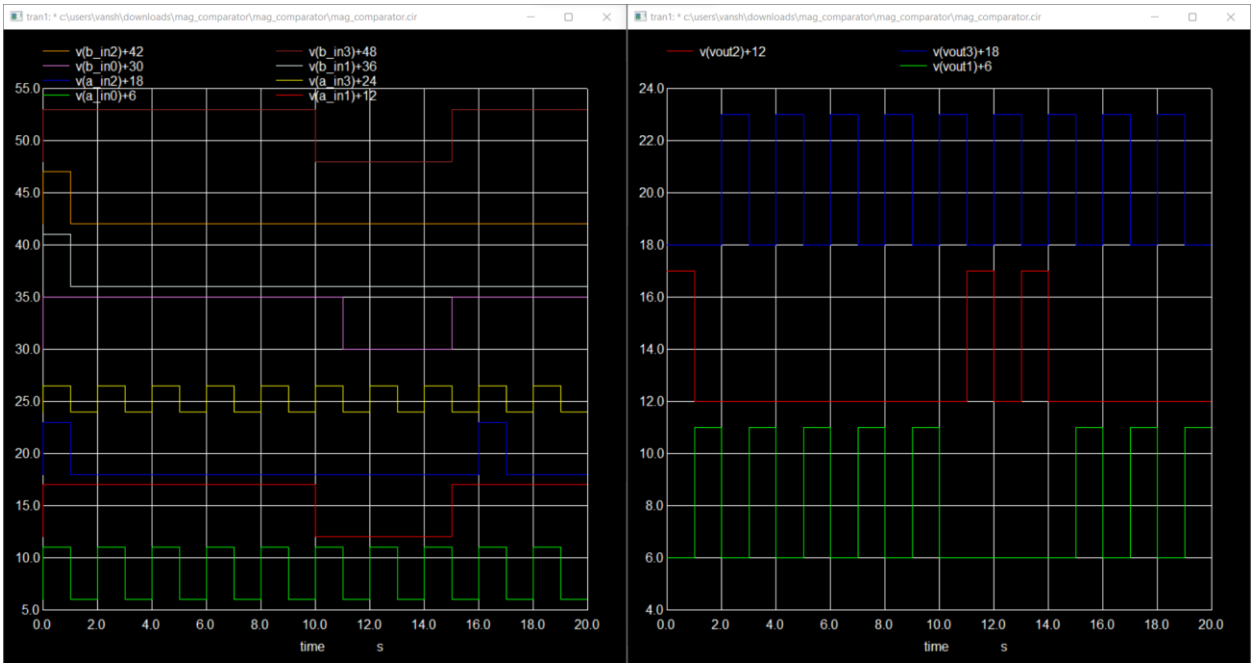
2. Ngspice plot of input B (B0,B1,B2,B3)



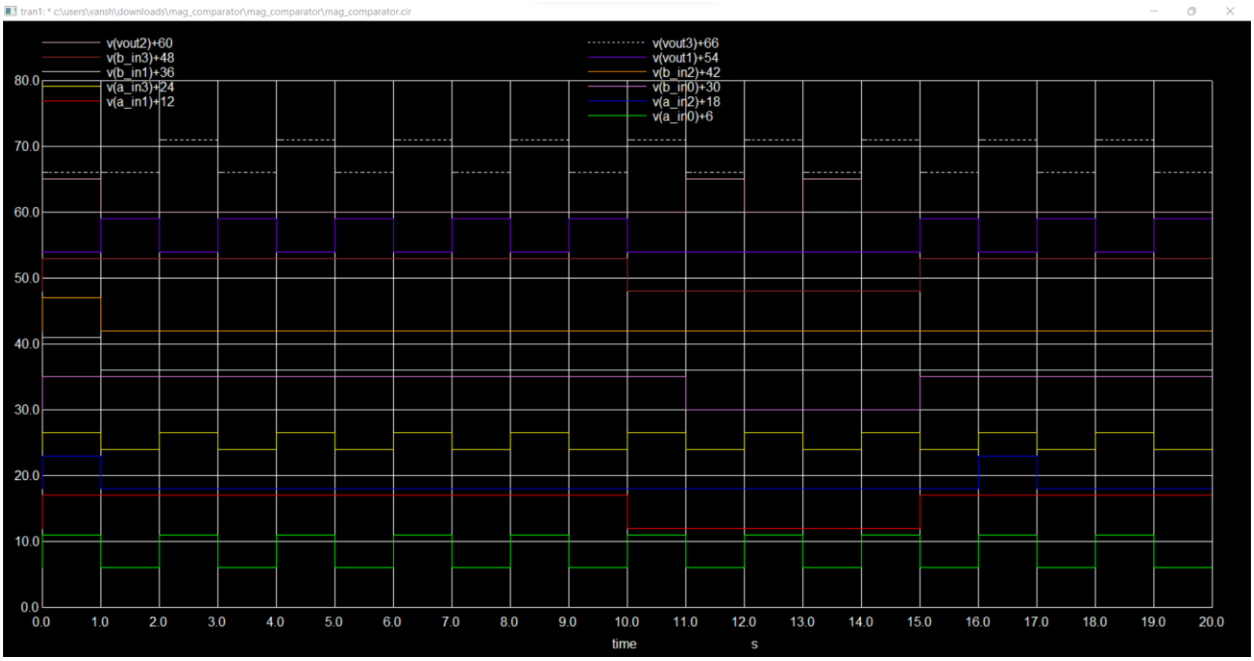
3. Ngspice plot of output (vout1,vout2,vout3)[A<B, A=B , A>B]



4.Ngspice plot of input vs output



5.Combined Ngspice plot of input and output.



So, the resultant waveform has been verified.

Conclusion

Hence, a mixed signal 4 bit magnitude comparator circuit has been designed , implemented and simulated in eSim tool and the respective waveform have been generated and verified.

References

1. https://www.researchgate.net/publication/352178954_Design_and_Simulation_of_a_Low_Design_and_Simulation_of_a_Low_Power_and_High-Speed_4-Bit_Magnitude_Comparator_Circuit_using_CMOS_in_DSch_and_Microwind
2. https://www.researchgate.net/publication/275726067_Performance_Analysis_of_Magnitude_Comparator_using_Different_Design_Techniques
3. https://eevibes.com/digital-logic-design/how-to-design-a-4-bit-magnitude-comparator-circuit/

Submitted by :

Vanshika Tanwar

Dronacharya Group Of Institutions, Greater Noida, Uttar Pradesh

Dr.APJ Abdul Kalam Technical University, ,India