Design Of 1-Bit Full Adder Using CMOS Mirror Logic

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Abstract

This paper presents a 1-bit full adder cell designed by using the CMOS mirror technique. The full adder circuit is one of the most widely used building blocks in all arithmetic and digital data processing systems. This circuit accepts two 1-bit inputs and produces two 1-bit outputs i.e. sum and carry. We use the property of inversion and self-duality to design this circuit. Because nowadays we have to deal with huge bits of data, we can switch to more advanced adder architectures like RIPPLE CARRY, CARRY SKIP, CARRY SELECT, CARRY LOOK AHEAD, etc. The major drawback of the CMOS mirror circuit is that it consumes more power and occupies more area due to the greater number of transistors used.

1. Reference Circuit Details

Transistor level implementation of full adder using CMOS mirror logic uses 28 transistors out of which 14 are nmos and 14 are pmos. By using CMOS mirror design we can save an area of 12 transistors as compared to the conventional CMOS approach. If a function obeys both inversion and self-duality properties then we can mirror the nmos stack to pmos i.e. pull-up stack is symmetrical to pull-down, unlike the opposite to pull-down stack in conventional CMOS. By this approach, we can reduce pmos stack size and can have equal rise and fall delays. Instead of realizing two functions independently, we will use cout signal to generate sum signal. The full adder circuit presented in this paper can be further used as a building block to generate an N-bit adder, which accepts two n-bit inputs and produces n-bit sum. One such adder architecture is known as ripple carry adder where these full adder blocks are cascaded one after the other. Each full adder in this architecture produces a 1-bit sum and passes the carry to the subsequent full adder. In this way carry ripples through each of the full adder stages. Speed of this carry rippling through each stage define the speed of the adder. Nowadays there are some advanced static CMOS techniques like CPL, TG, GDI, etc., to design a high speed and low power consumption full adder but tuning the circuit alone is not the feasible solution as we have to deal with huge bits of data at a time. In this case, optimizing the architecture of the adder circuit can come in handy.

2. Circuit
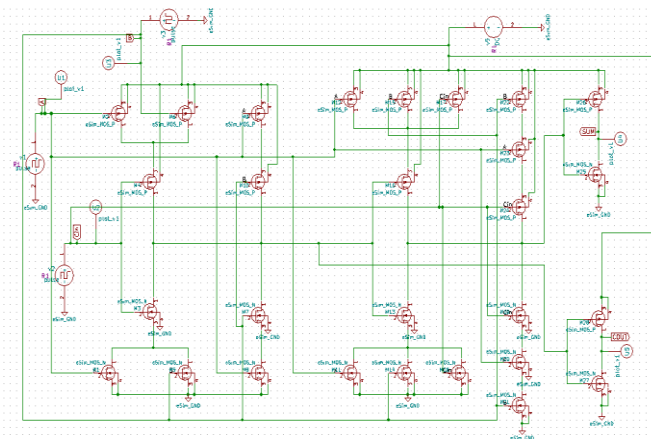
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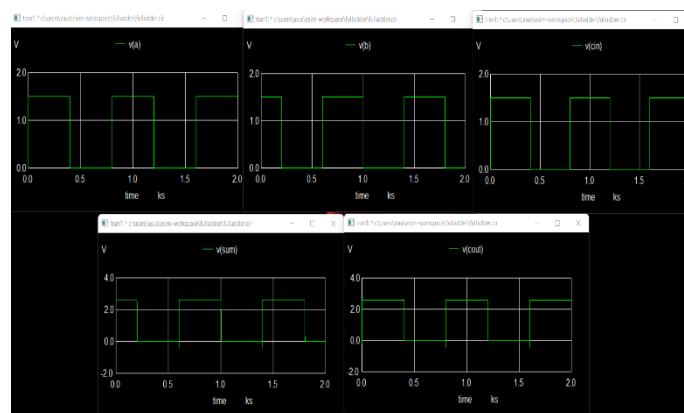
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