Design and Implementation of 6T SRAM in CMOS Technology

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Abstract

SRAM is a memory component and is used in various VLSI chips due to its unique capability to retain data. This memory cell has become a subject of research to meet the demands for future communication systems. In this paper a 6T SRAM cell is designed by using Verilog and esim software. Static random-access memory (SRAM) is a static memory cell which is widely used in various electronic systems. It is faster and consumes less power as compared to other memory cells [1-2]. It does not require refreshing periodically. Because of this, SRAM is the most popular memory cell among VLSI designers.

1.Reference Circuit Details

A conventional 6T SRAM cell consists of two inverters which are connected back-to-back. Fig. 1 shows the basic structure of a 6T SRAM memory cell [1]. The data which must be stored is latched in these two inverters. The process of storing a data is known as Write operation and the process of recovering the data is known as Read operation. Write operation is used for uploading the contents in a SRAM cell while Read operation is used for fetching the contents. The read operation is done with the help of sense circuits which sense BL and BLB data line before discharging it completely [4-5]. Basically, SRAM performs three operations which are Hold, Read and Write operations. ... Whenever the two access pass transistors of the word line (WL) are in OFF state, then the bit line and bit line bar (BL & BLB) are also in OFF condition, hence the memory cell is in hold state .

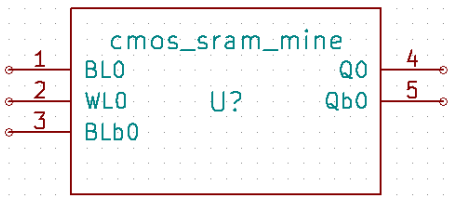

Fig.1. A 6T SRAM Cell Designed in NgVeri Tab

2. Implemented Circuit

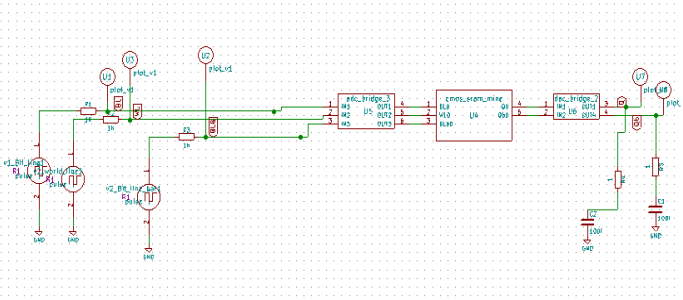

Fig.2 Circuit Diagram of the standard 6T SRAM cell operation

The schematic diagram of the designed 6T SRAM cell is shown in Fig. 2. This circuit contains PMOS NMOS , Pulse voltage source , Dc voltage source. They are connected in manner to form 6T SRAM cell.

3.Implemented Waveform

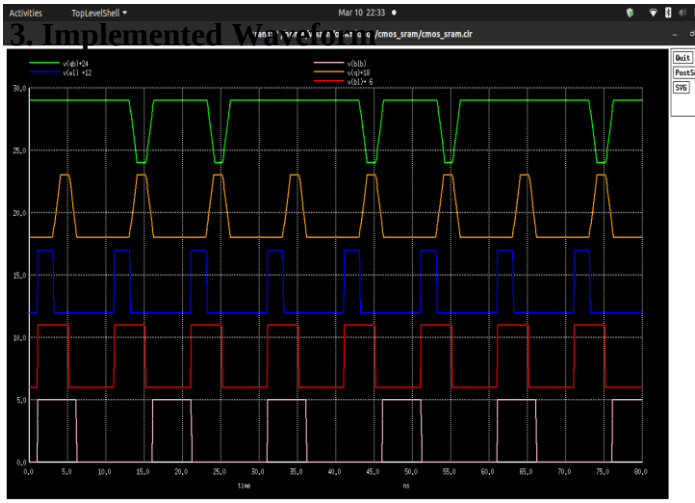

Fig.3 Implemented Waveform of CMOS based 6T SRAM cell

4. Reference

1.Rohit Kumar Sah1 , Inamul Hussain 2 , Manish Kumar3 1,2,3 Department of ECE, North-eastern Regional Institute of Science & Technology, Nirjuli, India, https://www.iosrjournals.org/iosr-jvlsi/papers/vol5-issue2/Version-1/C05212022.pdf