Title of the Project:
Mixed-Signal Implementation of MOD-10 (decade) Ripple Counter using NgVeri tool of eSim

Theory:
Decade counter or BCD counter, as the name suggests it has ten distinct states, it counts sequence from zero (0000) to decimal nine (1001). A decade counter is also often used for dividing a pulse frequency exactly by 10. The input pulses are applied to the paralleled clock inputs, and the output pulses are taken from the output of flip-flop D, which has one-tenth the frequency of the input signal. In this project, we are going to design digital blocks with the Verilog behavioural design of the JK flip-flop and NAND gate that is used as a basic block for the decade counter. And to use these digital blocks we are going to use digital to analog and analog to digital converters.

Reference Circuit Diagram:

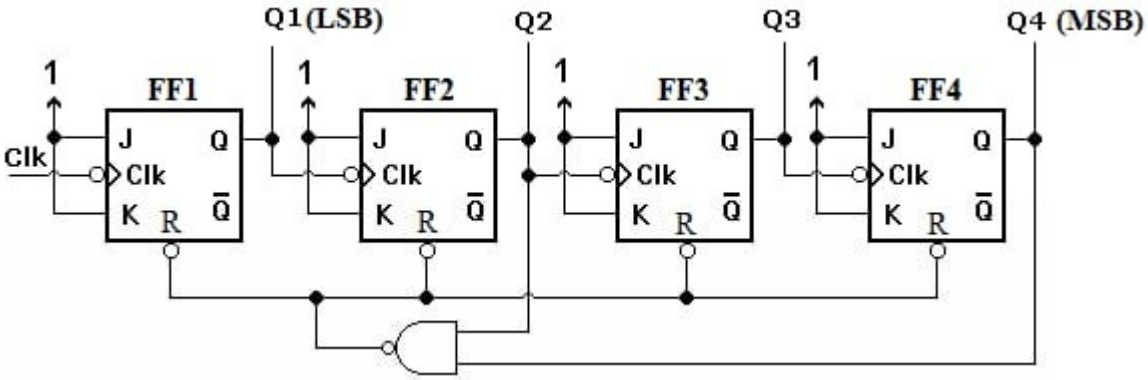

Figure 1: MOD-10 Counter

Schematic Diagram:

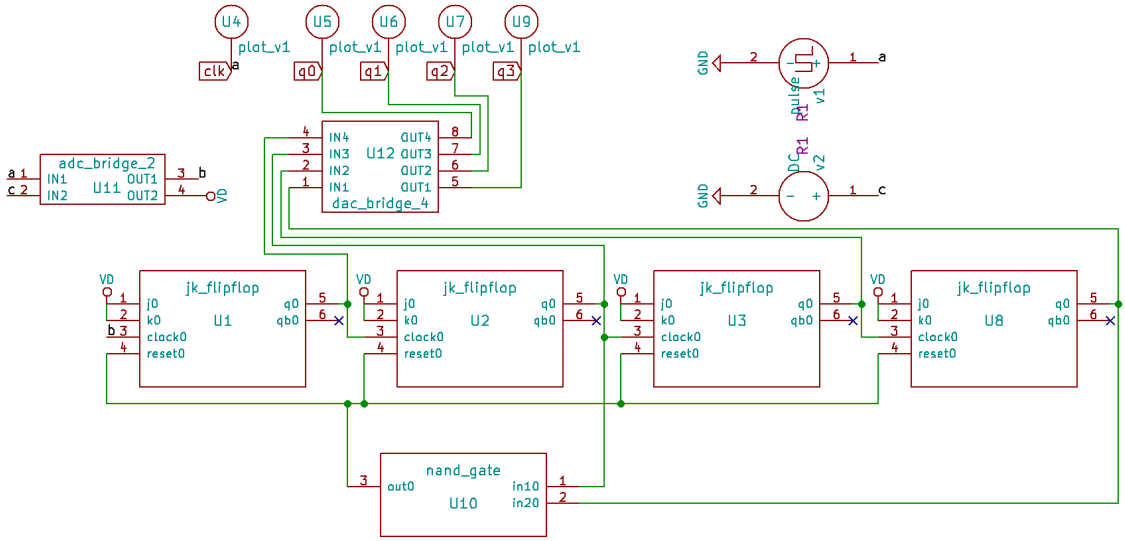

Figure 2: MOD-10 Decade Counter Schematic

Verilog Behavioral module of JK Flip-Flop:

```
module jk_flipflop (j,k,clock,reset,q,qb);

    input j,k,clock,reset;
    output reg q,qb;
        always@(negedge clock)
            begin
                case({reset,j,k})
                    3'b100 :q=q;
                    3'b101 :q=0;
                    3'b110 :q=1;
                    3'b111 :q=~q;
                    default :q=0;
                endcase
              qb<=~q;
    end
endmodule
```

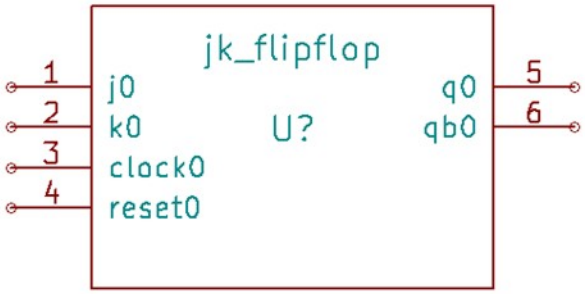

Figure 3: Schematic view of JK Flip-Flop

Verilog Behavioral module of NAND gate:

```
module nand_gate(in1, in2, out);

    input in1, in2;
    output out;

    assign out = ~ (in1 & in2);

endmodule
```

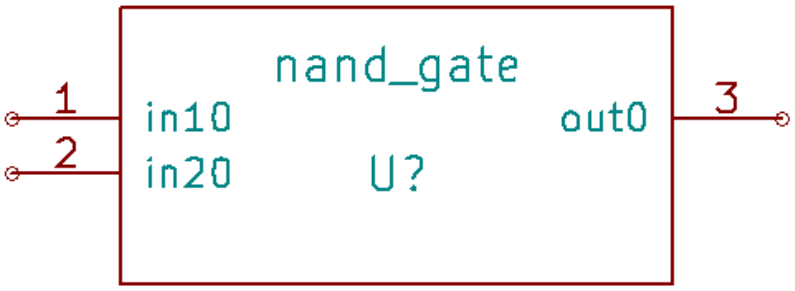

Figure 4: Schematic view of NAND Gate

NgSpice Waveform:

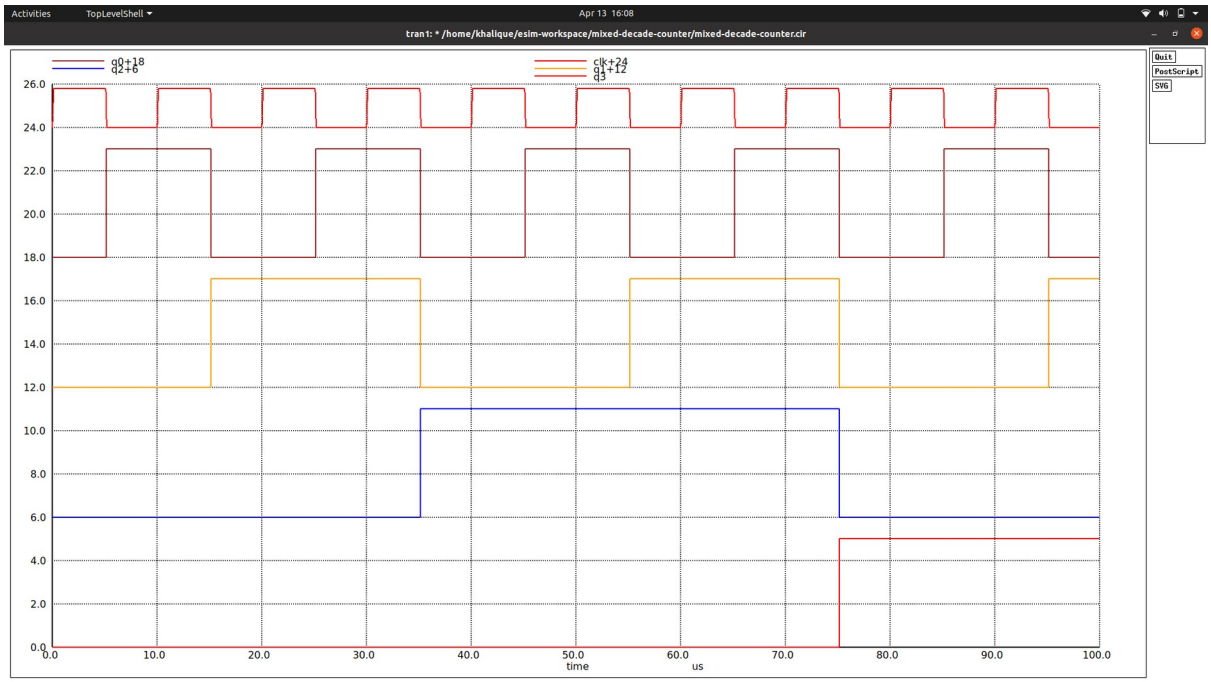

Figure 5: NgSpice Waveform

References:

- Fundamentals of pulse and digital circuits Ronald J Tocci
- https://www.electronicshub.org/decade-counterbcd-counter/

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