Sky130 8-T SRAM Cell for High-Speed Applications

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Abstract

SRAM or Static Random Access Memory is a form of semiconductor memory widely used in electronics, microprocessors and general computing applications. The main concern for SRAM cell design is stability. The stability of memory is affected by the aspect ratio of MOSFET and operating conditions. Memory stability aims to operate reliably and correctly. Stability in the SRAM cell is measured by Static Noise Margin (SNM). SNM is the minimum voltage noise that can flip the state of SRAM. While reading the stored data from SRAM, the stored value should not change.

Circuit Details

In this design, two voltage sources VS1 and VS2 connected to the outputs of the bit and bit bar line, respectively. Two NMOS transistors VT1 and VT2 are connected with inputs of bit and bit bar line directly to switch ON and switch OFF the power supply source during writing “0” and write “1” operations, respectively. These power supply sources reduce the voltage swing at the 'out' node when a write operation is being performed.

A. Write '0' operation

During the write '0' operation, the bit line goes low and the bit bar line goes high. So, the transistor VT2 goes ON and the transistor VT1 goes OFF. Thus the voltage source VS2 forces to decrease the voltage swing at the output of the bit bar line.

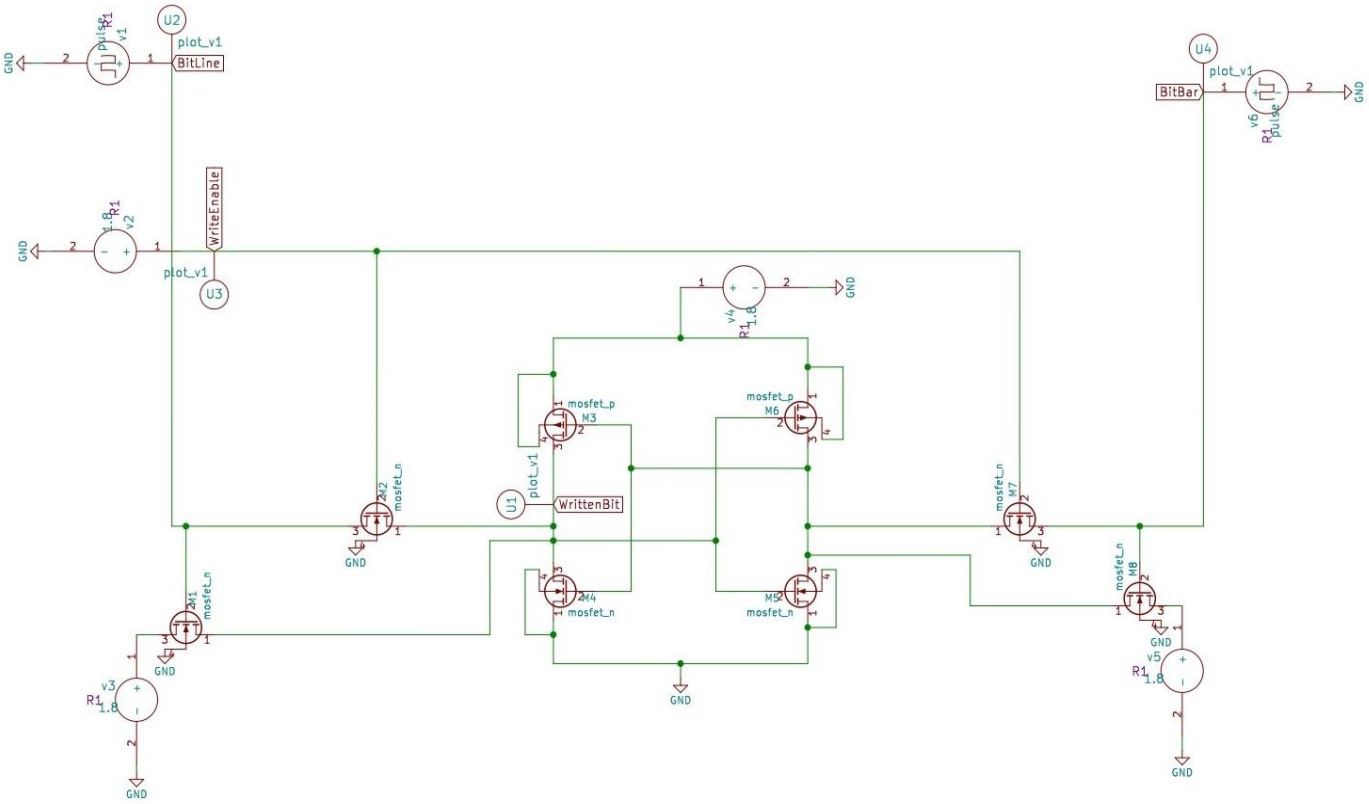
B. Write '1' operation

Similarly, when we perform the write '1' operation, transistor VT1 is ON and transistor VT2 goes to the OFF condition, so the voltage source VS1 decreases the voltage swing at the bit line output.

Due to the decrease in voltage swing, dynamic power dissipation is almost constant even if we increase the frequency of the SRAM cell.

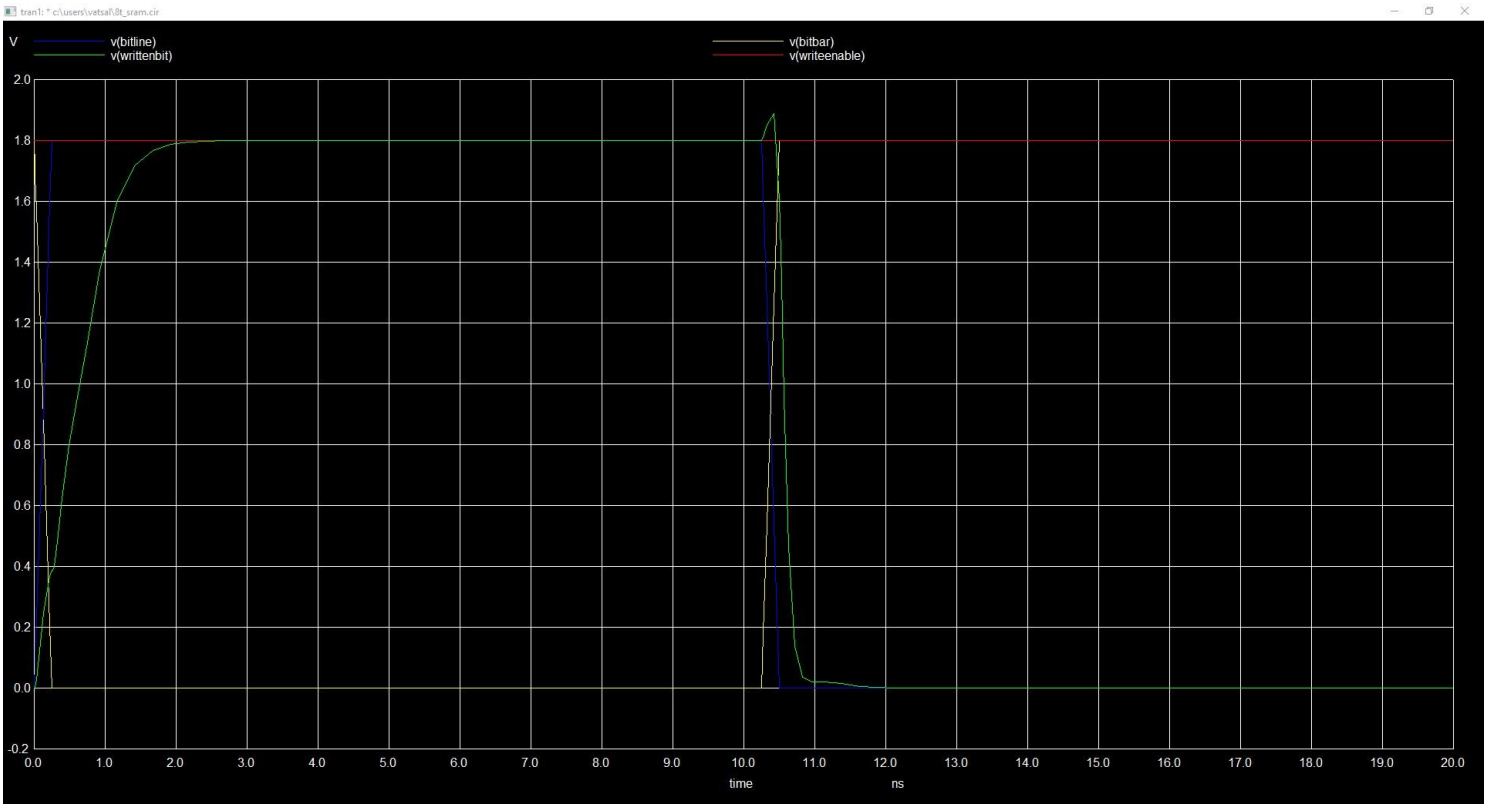
In this SRAM model, voltage sources VSI and VS2 decrease the voltage swing during switching activity. With the increase in frequency, the switching will also increase, but the voltage source decreases its voltage swing simultaneously at the output. So at a higher frequency, the dynamic power dissipation is almost constant. These two voltage sources also provide extra voltage during the write operations on the bit line, bit bar line and word line. This extra voltage will provide a better noise margin on the bit line and word line during write operations.

IMPLEMENTED CIRCUIT

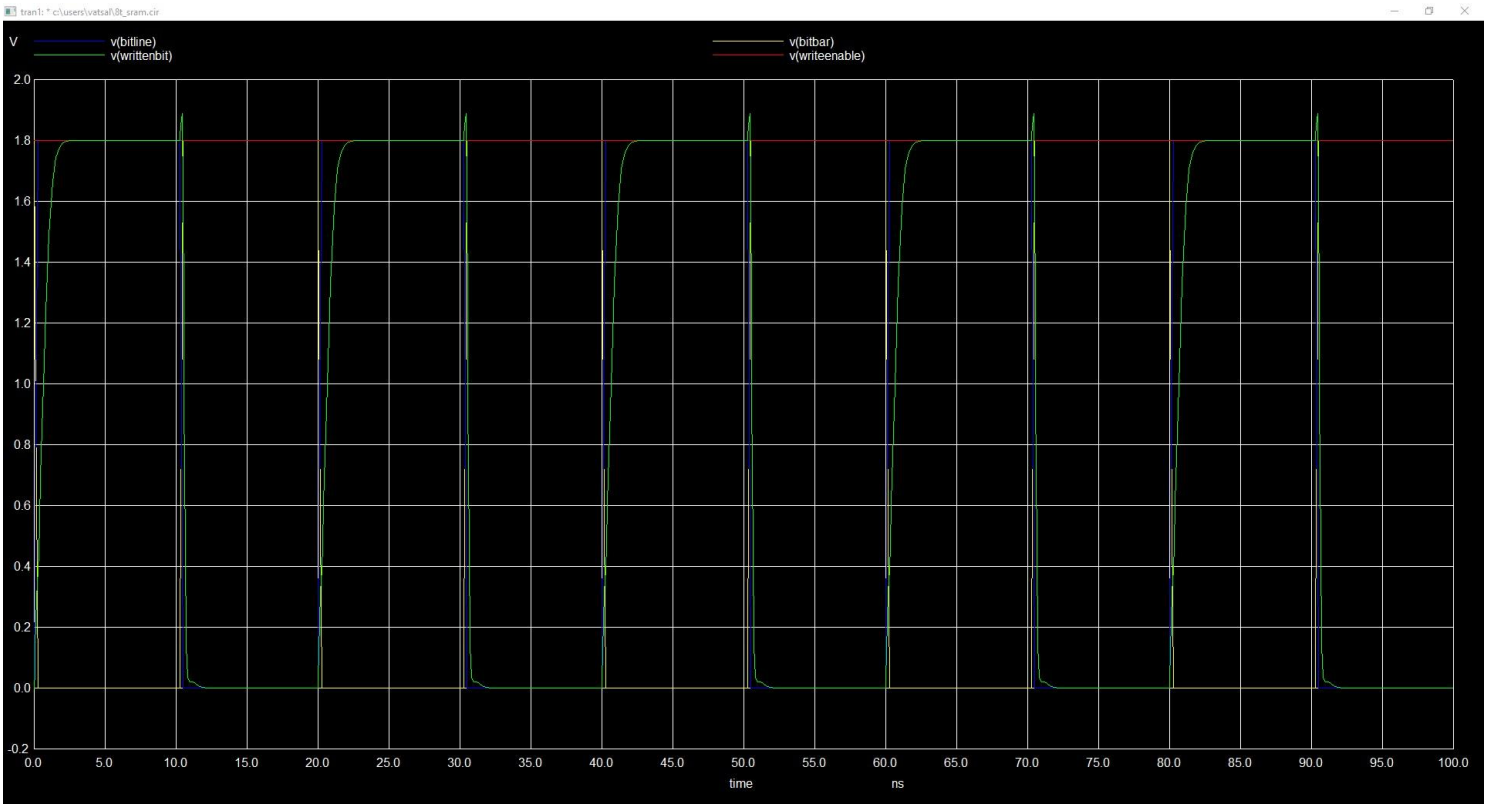


Simulation Results with Sky130 and NGSpice

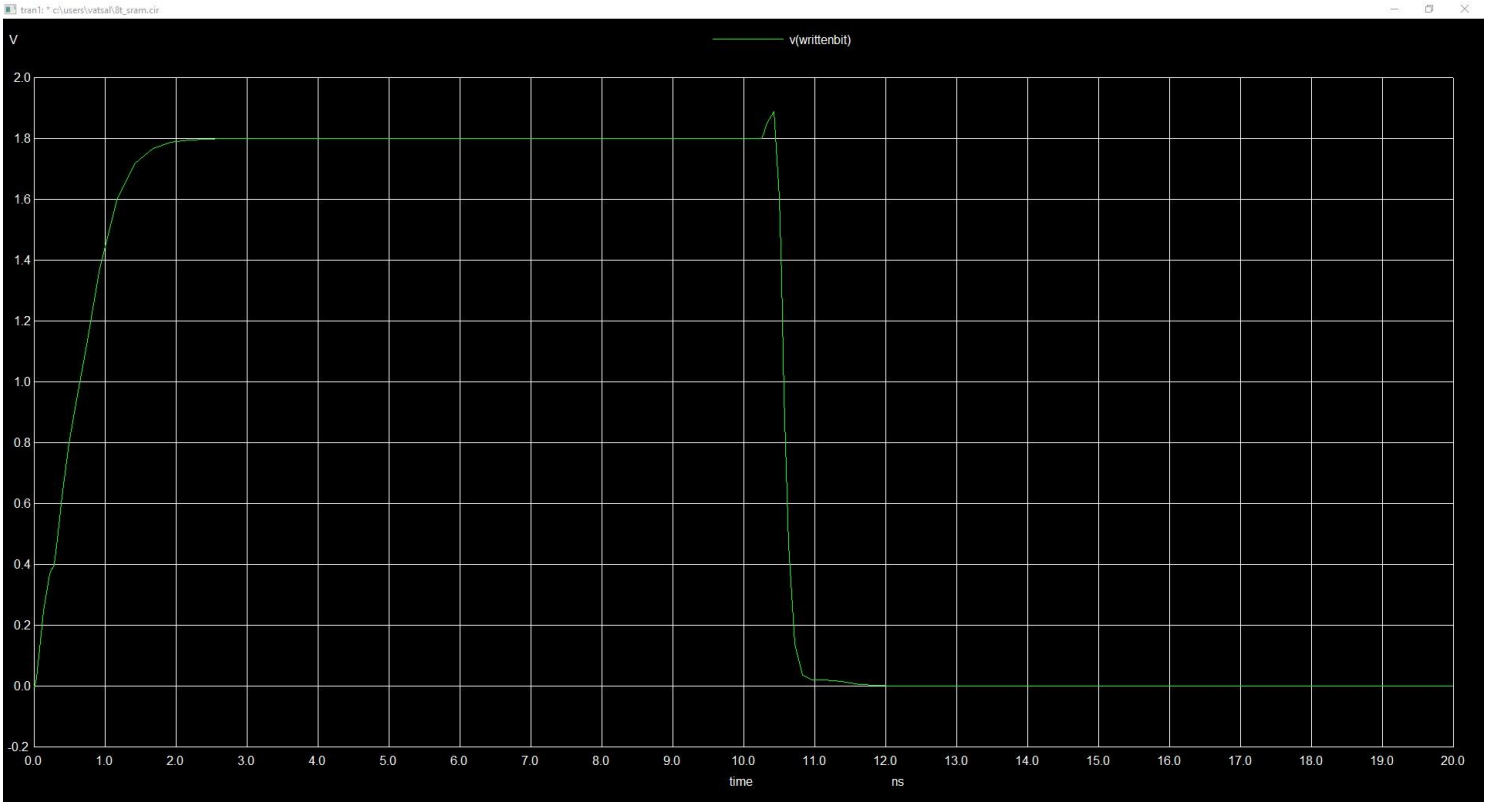
1. 20 ns Combined Signals



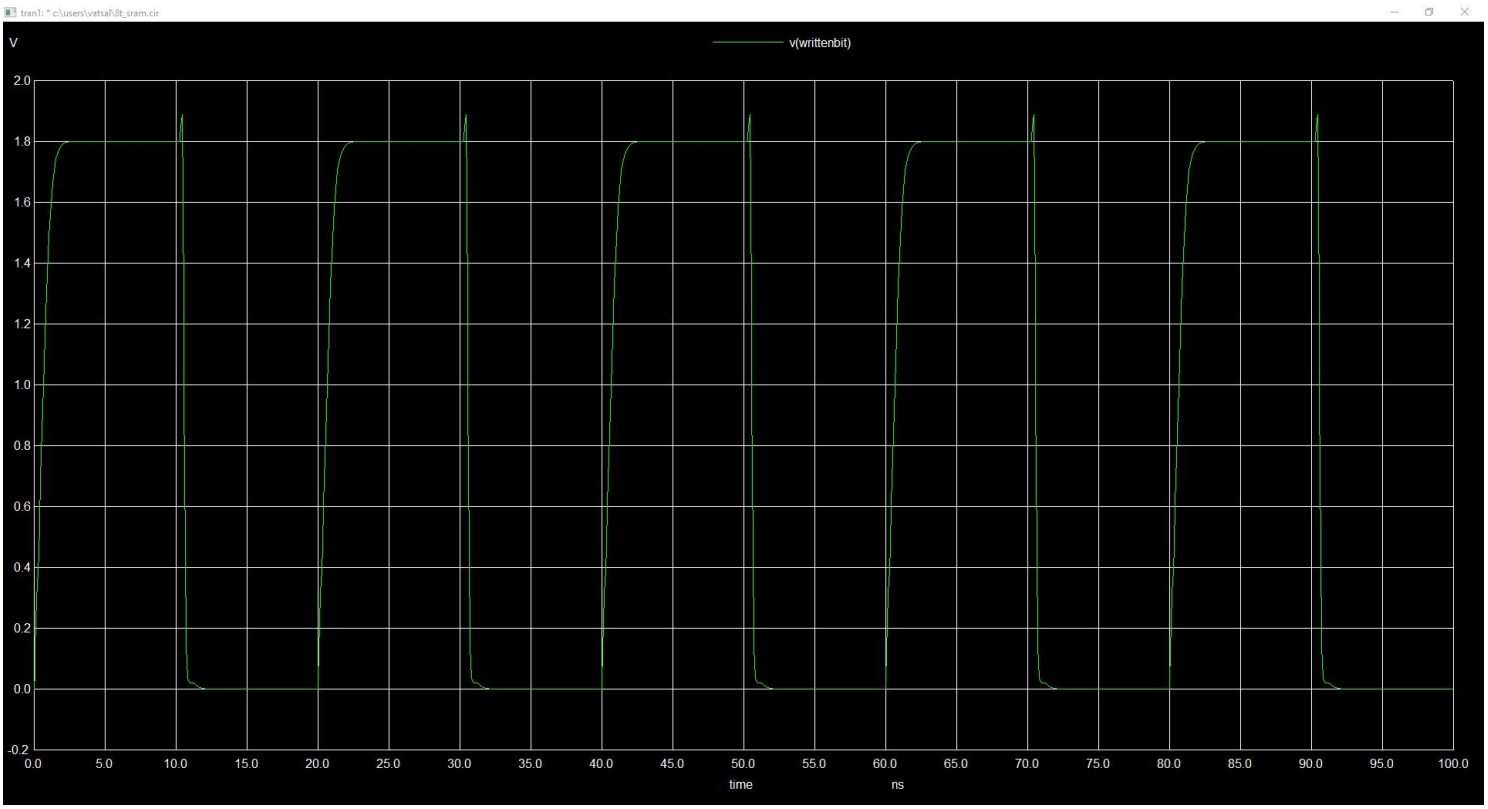
2. 100ns Combined Signal



3. 20ns Output Signal



4. 100ns Output Signal



Conclusion

As the simulations show the SRAM Cell works perfectly up to 100MHz frequency with a small delay and good write stability. The operating voltage of the circuit is 1.8V and the CMOS technology node is 130nm.

This SRAM cell has two voltage sources that are used for reducing the voltage swing during switching activity which results in the reduction of dynamic power dissipation as well as improvement of the stability during the write operation. The 8-T SRAM cell consumes less power and is more stable in comparison to the conventional 6-T SRAM cell. Although the number of transistors and area is increased for the 8-T SRAM cell in comparison to conventional SRAM cell. This 8-T SRAM cell can be used to provide low power solutions in high-speed devices like laptops, mobile phones, programmable logic devices etc.

References

Write Stability Analysis of 8-T Novel SRAM cell for High-Speed Application