# ABSTRACT

## Design and implement asynchronous MOD 10 counter using JK Flip Flops

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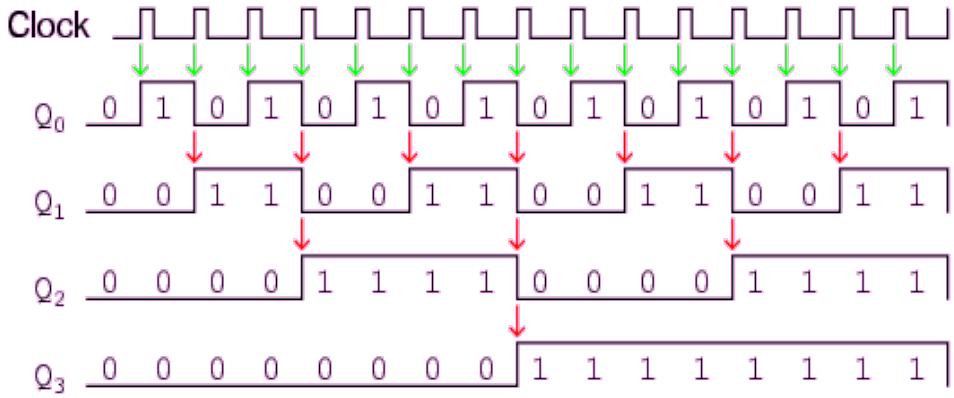
**Theory:-**

"Asynchronous counter" is a counter circuit, which created from the series of J-K flip-flops. The clock signal will be given to the clock input of the first J-K flip-flop then the output of the first J-K flip-flop will connect to the input of the adjacent flip-flop. The output signal, which represents the current binary counting value, is the output signal ( *Q* ) of all J-K flip-flop. While the output ( *Q* ) of the first J-K flip-flop is the least significant bit (LSB) of the binary value.

The maximum number of counting value depends on the number of J-K flip-flops in the circuit. For example, the 4 bits counter is composed of 4 J-K flip-flops. This maximum number, which this counter can count, is $2^4$ = 16. Hence, this counter can count from 0 to 15. If the output ( *Q* ) of the first J-K flip-flop is connected to the clock input of the adjacent J-K flip-flop, this counter will be the count-up counter. For example, the connecting of flip-flops in Fig. 1 is "4-bits count-up asynchronous counter".However, if the output ( *Q* ) of the first J-K flip-flop is connected to the clock input of the adjacent J-K flip-flop, this counter will be the count-down counter, as shown in Fig.



## Design

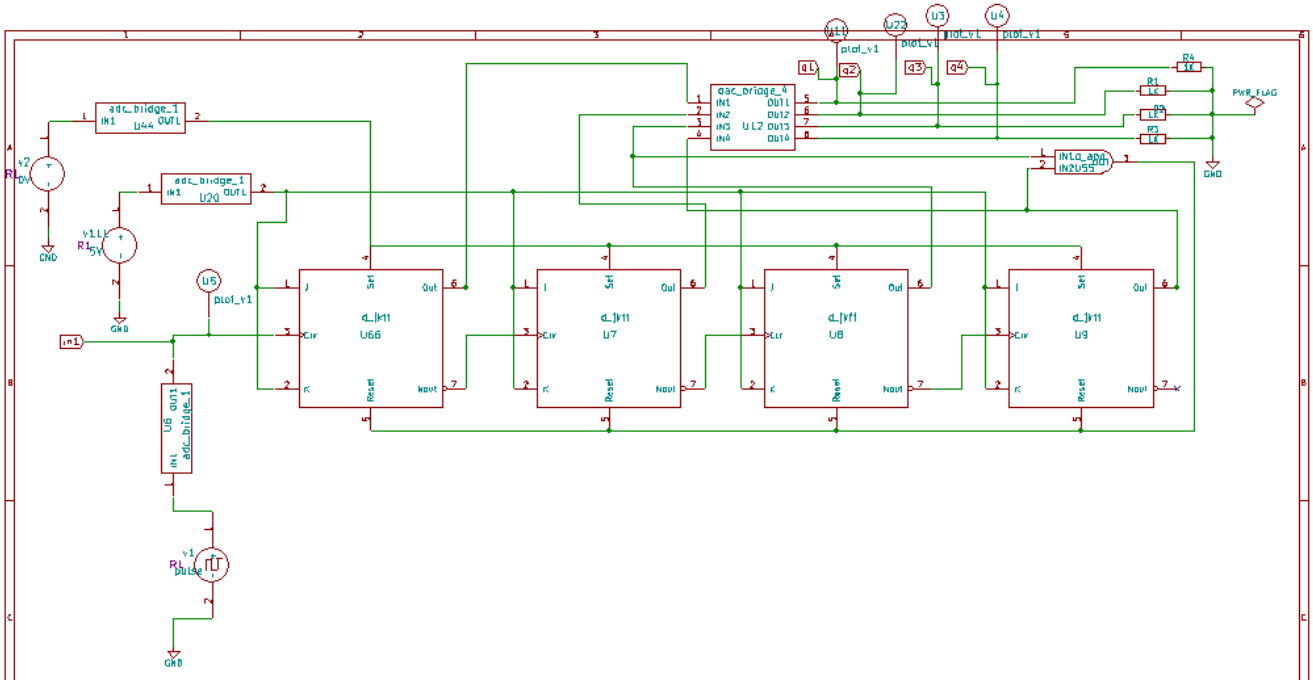


Fig 1: MOD 10 asynchronous counter

2. Ngspice Plots:

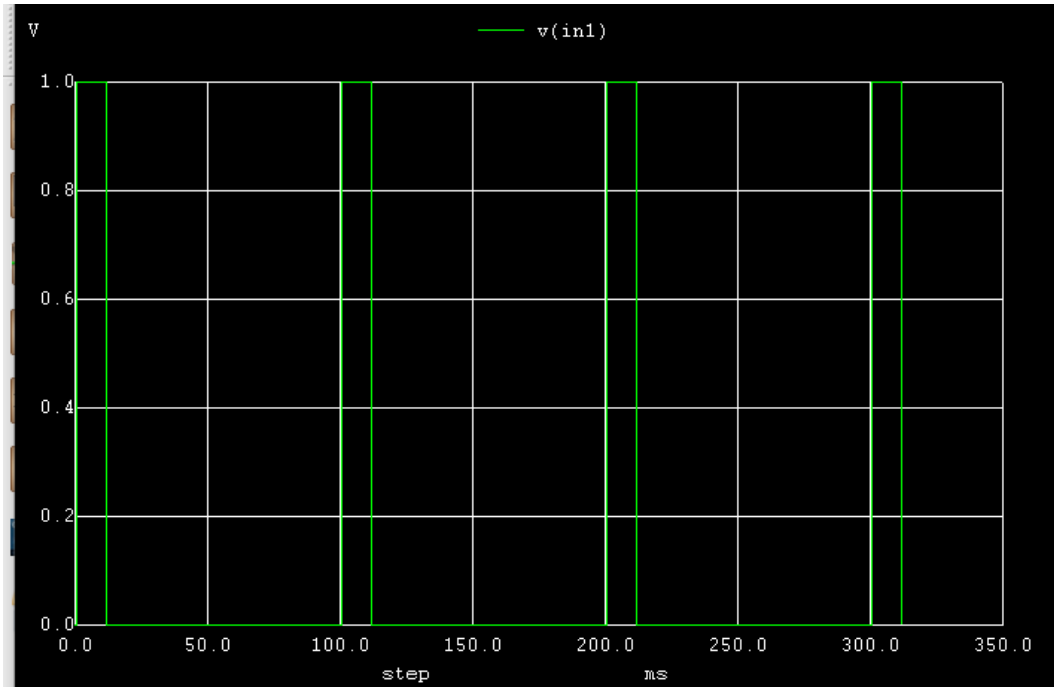



Fig 2:Ngspice Input Waveform

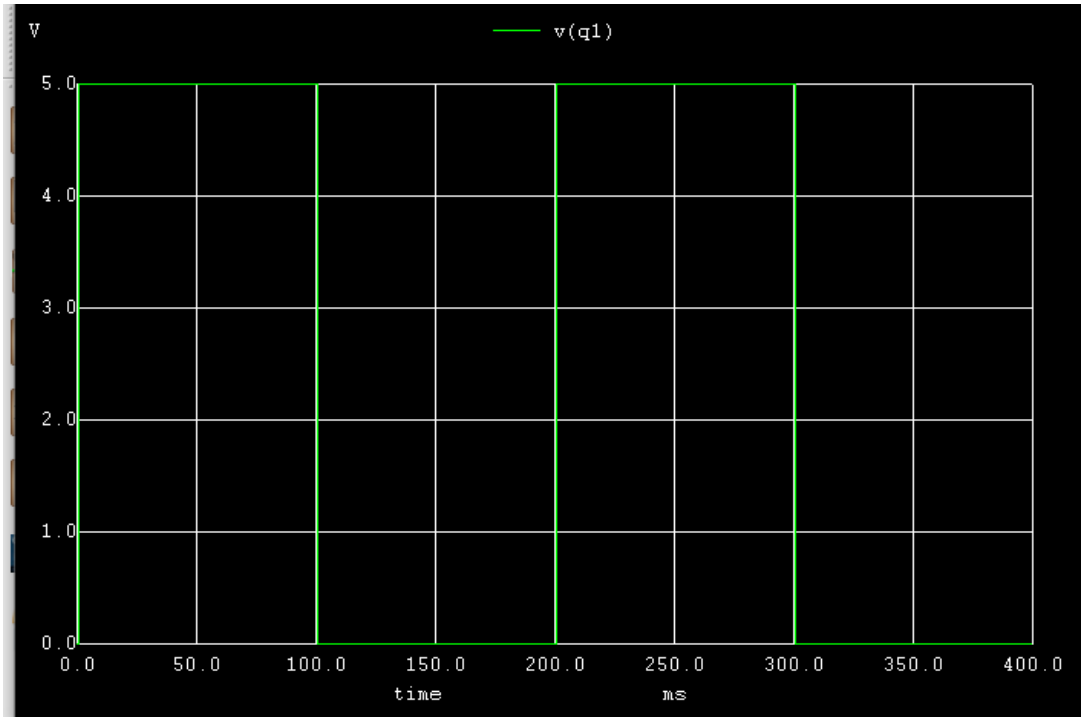



Fig 3:Ngspice output plot of q1

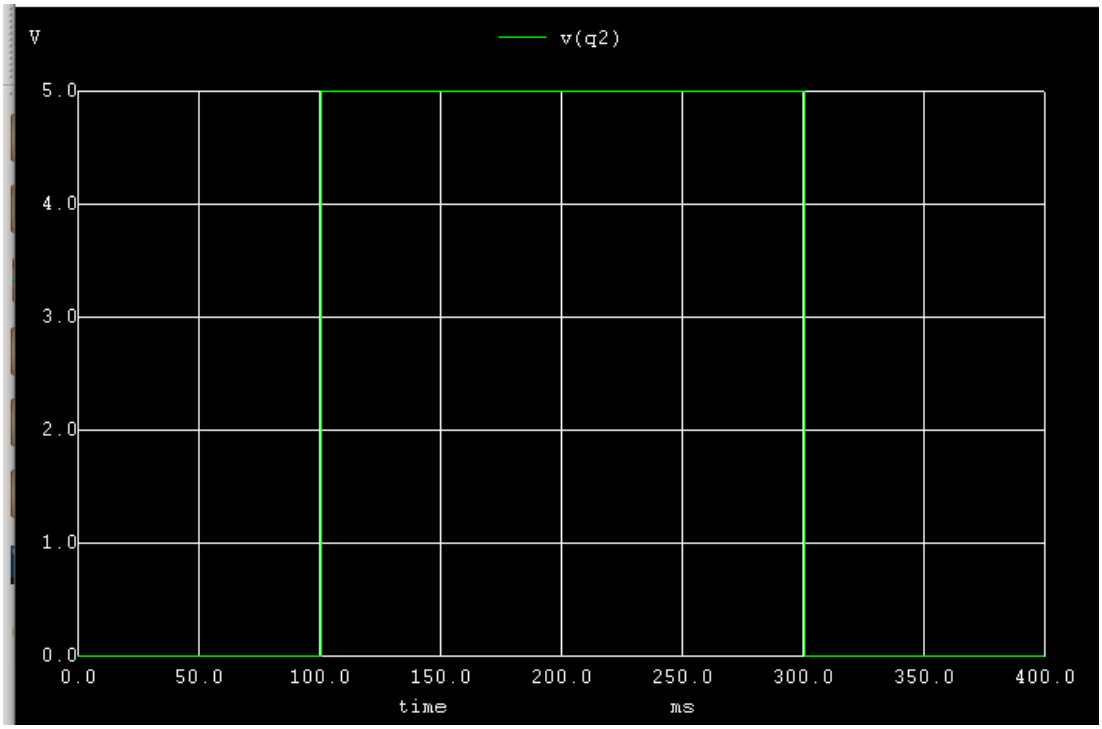



Fig 4:Ngspice output plot of q2

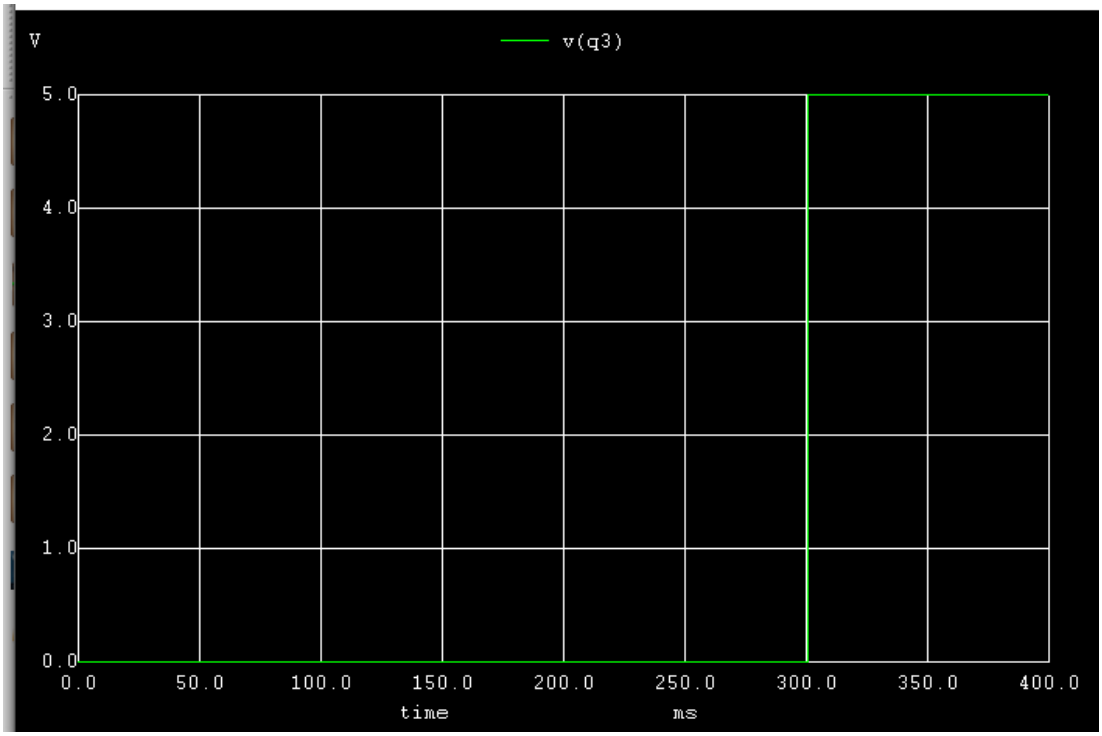



Fig 5:Ngspice output plot of q3

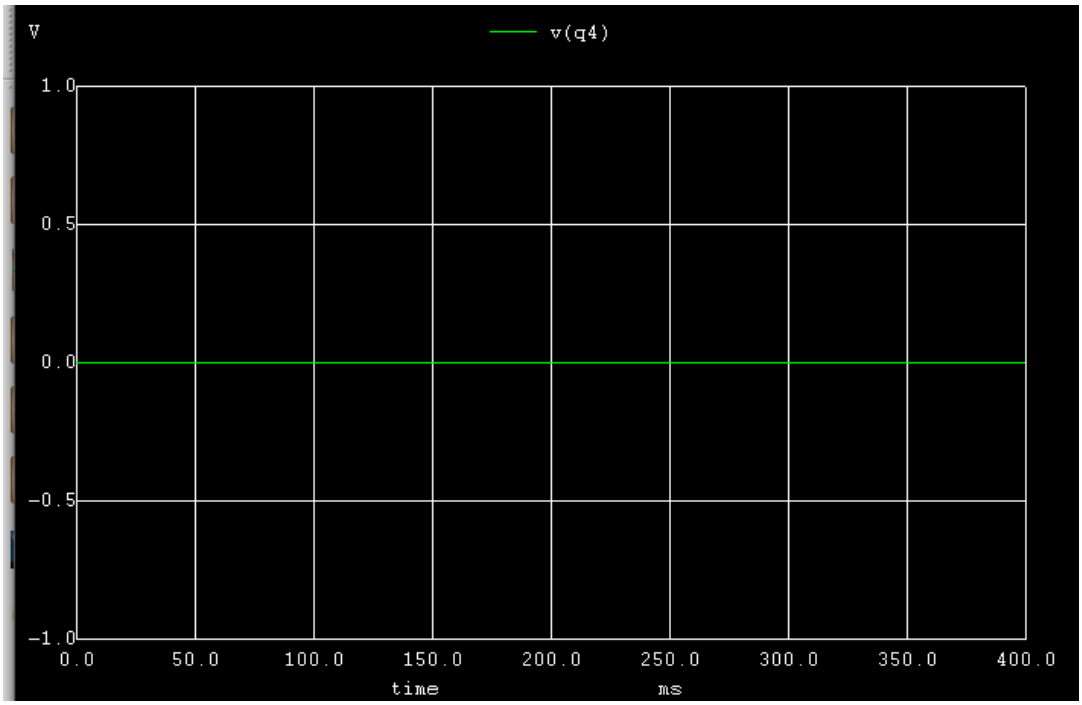



Fig 6:Ngspice output plot of q4

Python Plots:

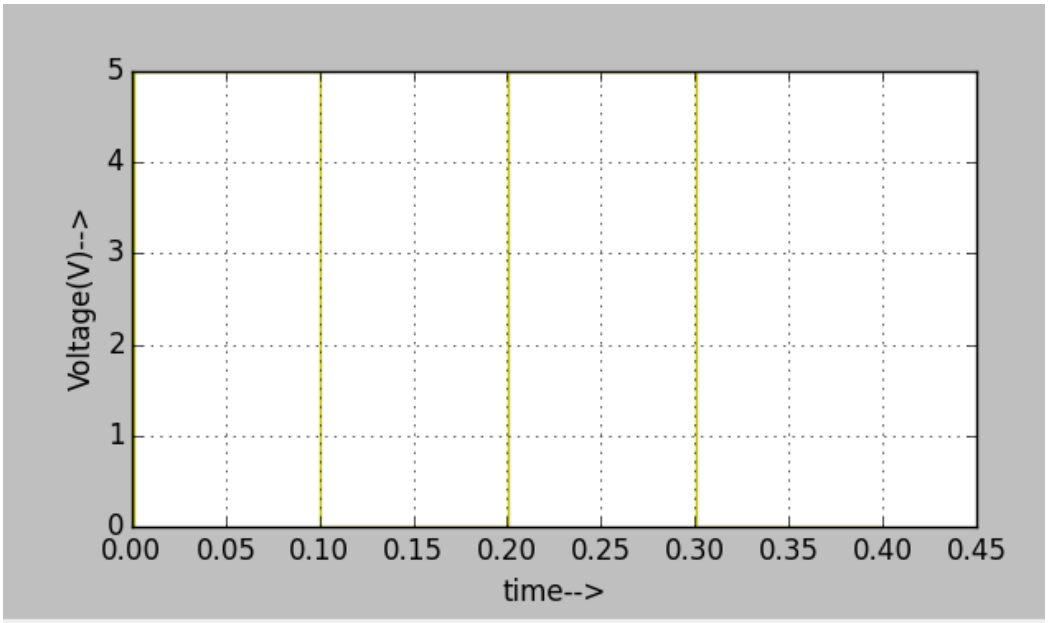



Fig 7:Python plot of q1

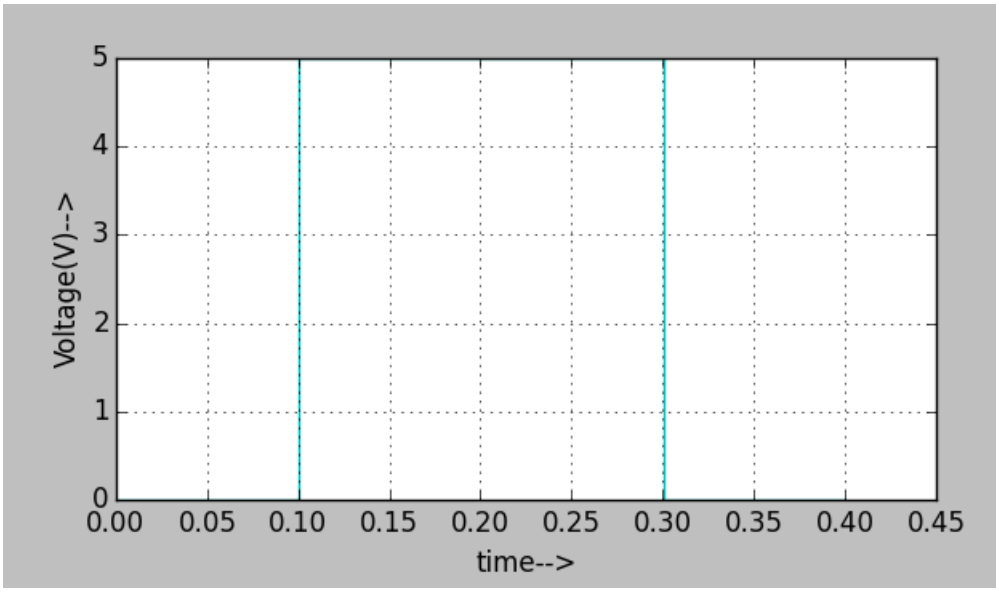



Fig 8:Python plot of q2

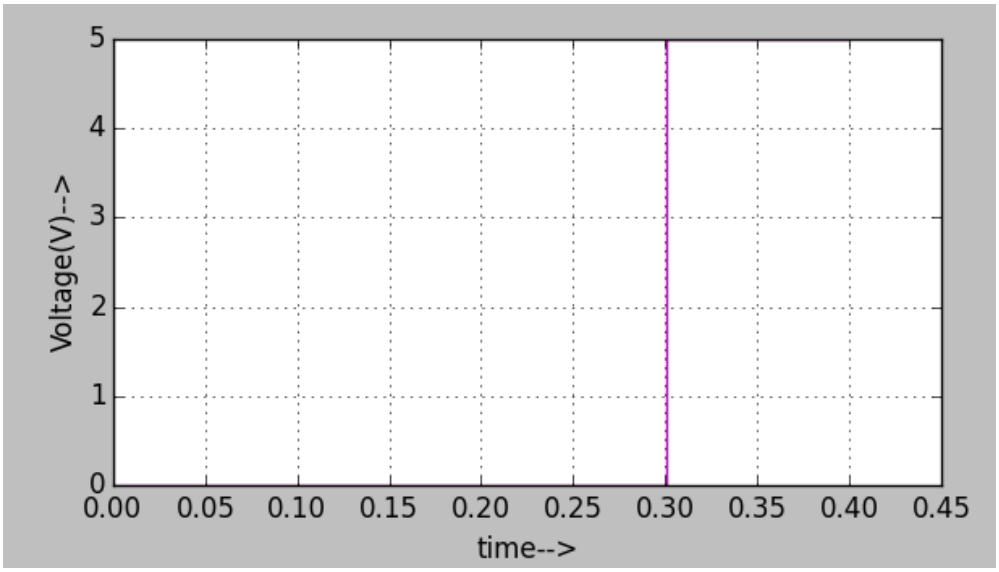



Fig 9:Python plot of q3

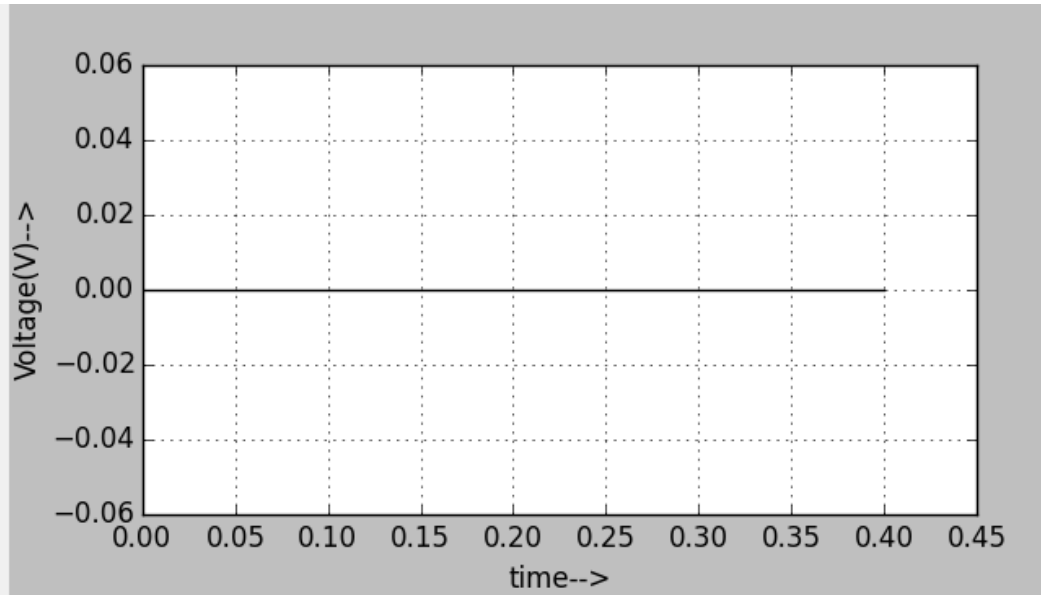



Fig 10:Python plot of q4

Reference:

1. -http://elektronika-dasar.web.id/asynchronous-bcd-decade-counter/.