Mixed Signal Design of Variable Frequency Divider using eSIM and NgVeri

Trinath Harikrishna
B.Tech in ECE, SRM Institute of Science and Technology
e-mail: htrinath@gmail.com

***Abstract* – The scope of this work is to present a variable frequency divider implemented in the Mixed Signal domain using eSim and NgVeri. Here variable term signifies that based on the input provided the clock pulse can be divided by two, four or eight.This can be achieved by using a digital block to enable the series of frequency dividers**

***Keywords* – FREQUENCY DIVIDER, VARIABLE FREQUENCY DIVIDER**

I. INTRODUCTION

The frequency divider is a very important block in many analog and digital applications. It is most importantly used in the PLL for dividing the output signal from the VCO. A simple way to design a frequency divider is to loop the qbar output to D input in a D flipflop.

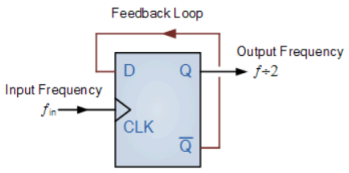

Fig. 1. Frequency Divider Block Diagram

II. Selector Circuit

This is a custom encoder which can designed using the NgVeri feature of the eSIM. In this there are two inputs based on which the output will vary as follows:

00 – the circuit will not give any output.
01 – will obtain a divided by 2 frequency output.
10 – will obtain a divided by 4 frequency output.
11 – will obtain a divided by 8 frequency output.

III. Frequency Divider

As shown in the above figure we can see that when the qbar of a D-flipflop is looped we get a divide by 2 frequency divider. To explain the operation of a frequency divider assume initially q is 0 and qbar is 1 for every positive edge of the clock i.e two clock cycles these values keep inverting hence causing a division in frequency

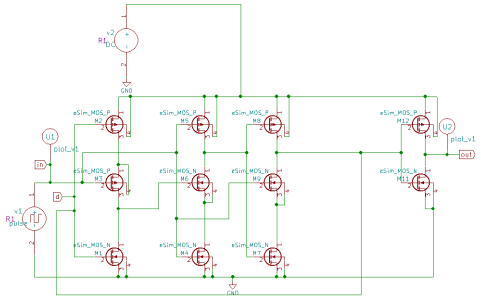

Fig. 2. Frequency Divider Schematic

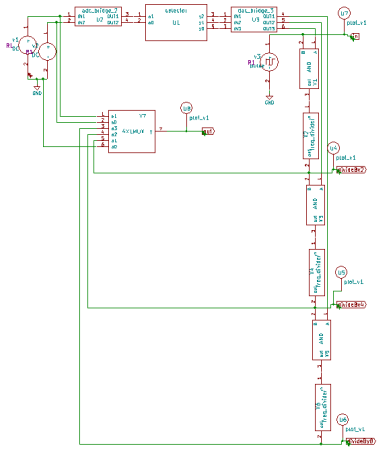

Fig. 3. Variable Frequency Divider Schematic

IV. Transient Analysis of the Frequency Divider

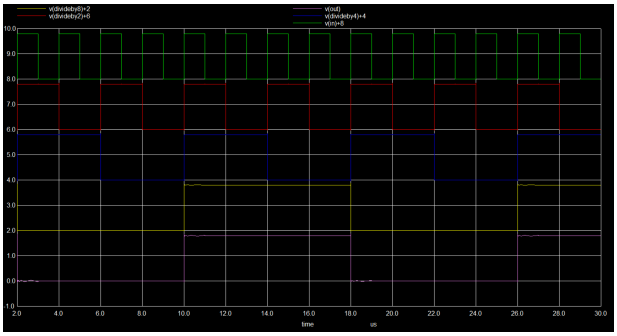

Fig. 4. Transient Analysis of Frequency Divider

References

[1] Lam, Jerry and Plett, Calvin. (2012). Modified TSPC clock dividers for higher frequency division by 3 and lower power operation. 437-440. 10.1109/NEWCAS.2012.6329050.

[2] J. Rogers, C. Plett and F. Dai, Integrated circuit design for high-speed frequency synthesis, Artech House, 2006