Title of the experiment:

Simulation Of Two-Input RTL AND Gate using eSim.

Theory:

Logic gates are the basic building blocks of any digital system. Logic gates are electronic circuits having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as

1. AND gate
2. OR gate
3. NOT gate
4. NAND gate
5. NOR gate
6. Ex-OR gate
7. Ex-NOR gate

A simple 2-input logic AND gate can be constructed using RTL (Resistor-Transistor-Logic) switches connected together as shown below with the inputs connected directly to the transistor bases. Both transistors must be saturated “ON” for an output at Q.

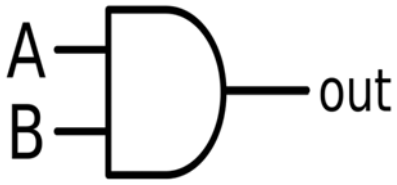

Figure-1:Logic Symbol of AND Gate

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Figure-2:Truth Table of AND Gate

Schematic Diagram:

The circuit schematic of Simulation of 2-Input RTL AND Gate and the function

Y= A.B in eSim is as shown below:

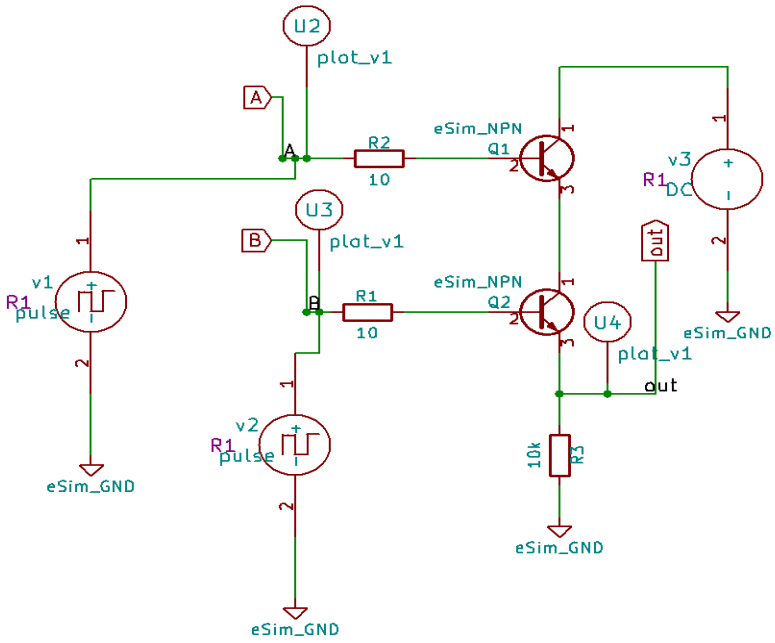

Figure 3: The 2-Input RTL AND Gate and the function **Y= A.B** in eSim

Truth Table:

Sr.No.	Input		Output
	A	B	Y
1	0	0	0
2	0	1	0
3	1	0	0
4	1	1	1

Simulation Results:

1.Ngspice Plots

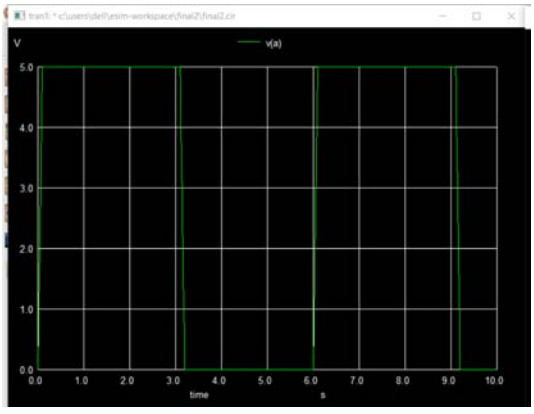

Figure 4: Ngspice plot of input A

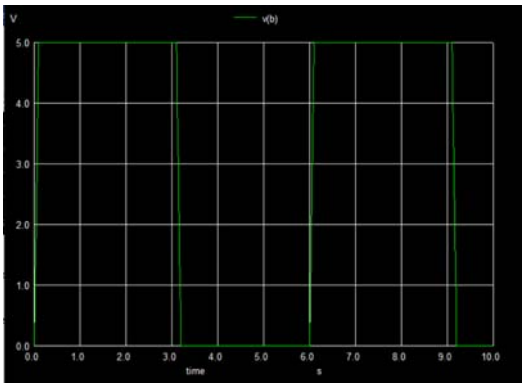

Figure 5: Ngspice plot of input B

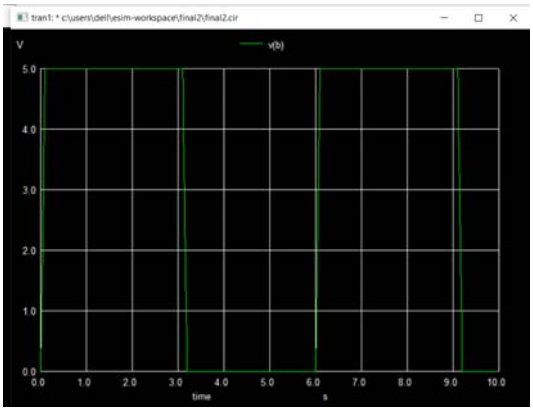

Figure 6:Ngspice plot of output variable Y

2.Python Plots:

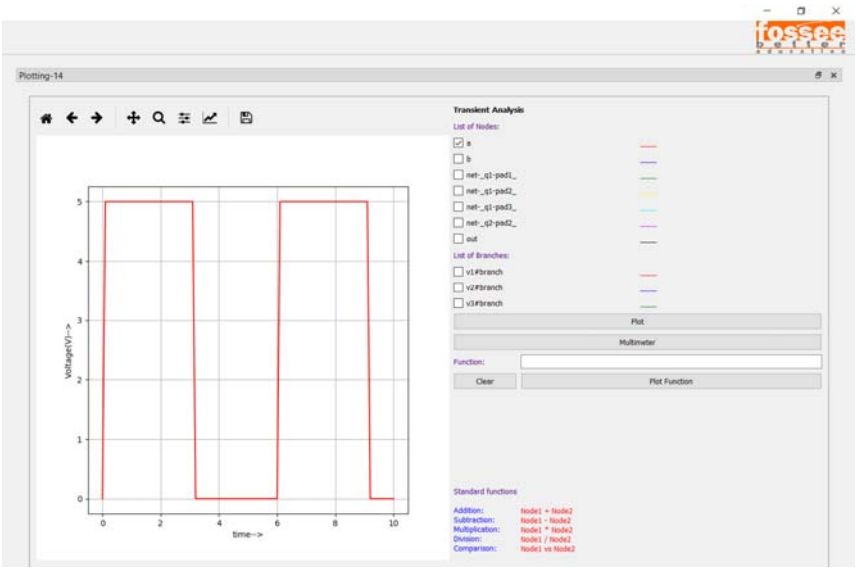

Figure 7:Python plot of input A

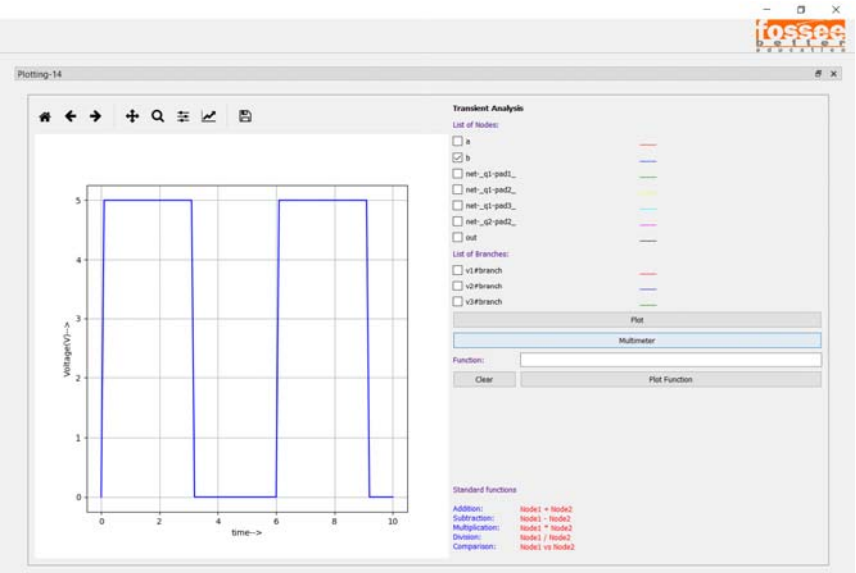

Figure 8: Python plot of input B

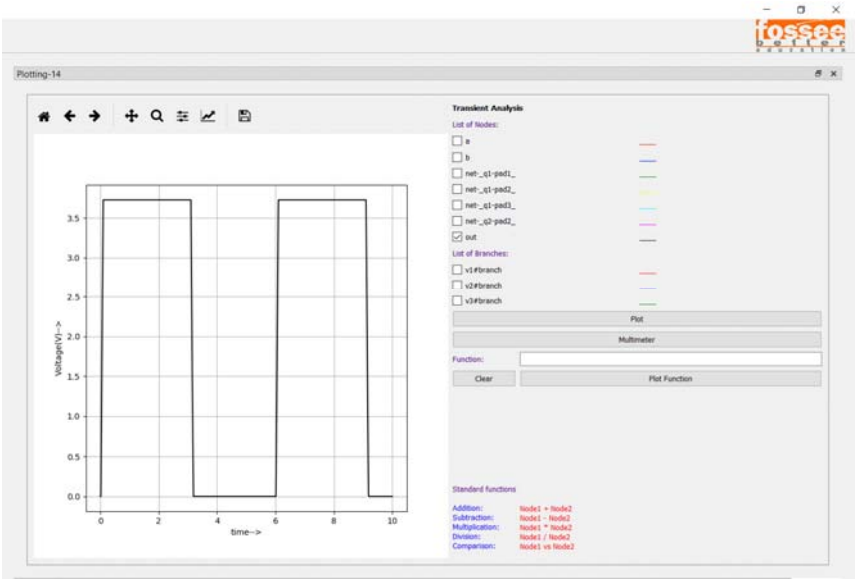

Figure 9: Python plot of output Y

Conclusion:

Thus, we have studied Simulation of 2-Input RTL AND Gate and function **Y= A.B,** using eSim and the waveforms are verified using truth table.

Source/Reference(s) :

1) Modern Digital Electronics by R.P.Jain