Title of the experiment:

Design of static CMOS Complex circuit function $Y = \overline{(a+b+c).d}$

Theory:

This function is a complex logic function in a single stage of logic which is formed by using a combination of series and parallel switch structures. This function is called as OR-AND-INVERT-3-1(OAI31) gate because it performs ANDing of three inputs and ORing of single input. The OR expression (a+b+c) is implemented by using parallel connections of NMOS transistors. ANDing this result with input D is implemented by taking series connections of NMOS transistors. Opposite connections are done for PMOS transistors. All the values can be verified from the truth table.

NMOS transistor is turned ON when gate terminal is applied with logic level 1. PMOS transistor is turned on when gate terminal is applied with logic level 0. This circuit is having four inputs a, b, c, d and one input. First ORing of three inputs a, b, c is done. Output of ORing is multiplied with d. This result is inverted using PMOS to get the output Y. The NMOS pull down network pulls the output low if d is 1 i.e., 3Volts and either a or b or c are 1, so d is in series with parallel combination of a, b, c. The PMOS pull-up network is the conduction complement, so d must be in parallel with the series combination of a, b and c. Power supply of 3 Volts is applied for proper conduction of circuit. In this implementation design of complex circuit function Y using 180 nm technology is proposed. All the values can be verified from the truth table.

Schematic Diagram:

The circuit schematic of static CMOS Complex circuit function $Y = \overline{(a+b+c).d}$ in eSim is as shown below:

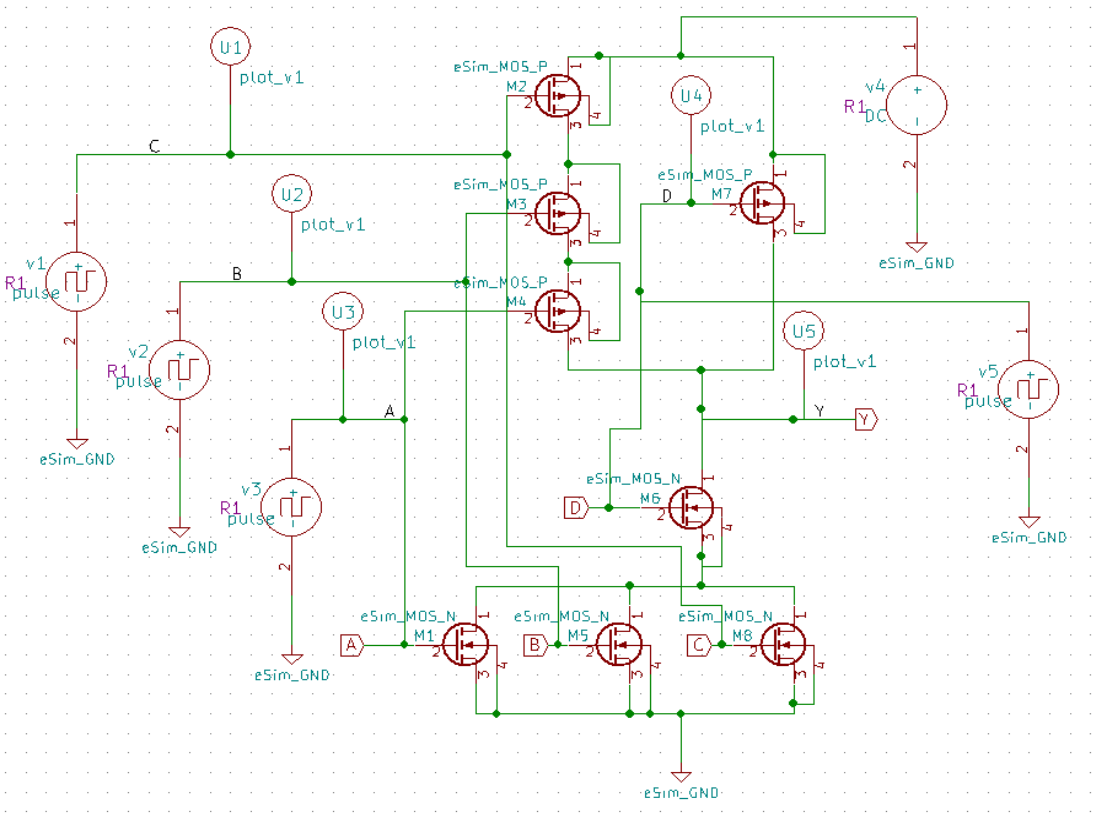

Figure 1: CMOS implementation of Complex circuit function $Y = \overline{(a+b+c).d}$ in eSim

Truth Table:

Sr.No.	Input				Output $Y = \overline{(a+b+c).d}$
	a	b	c	d	Y
1	0	0	0	0	1
2	0	0	0	1	1
3	0	0	1	0	1
4	0	0	1	1	0
5	0	1	0	0	1
6	0	1	0	1	0
7	0	1	1	0	1
8	0	1	1	1	1
9	1	0	0	0	1
10	1	0	0	1	0
11	1	0	1	0	1
12	1	0	1	1	1
13	1	1	0	0	1
14	1	1	0	1	1
15	1	1	1	0	1
16	1	1	1	1	0

Simulation Results:

1.Ngspice Plots

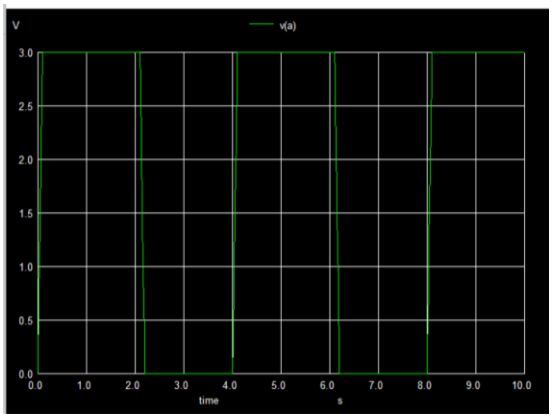

Figure 2: Ngspice plot of input a

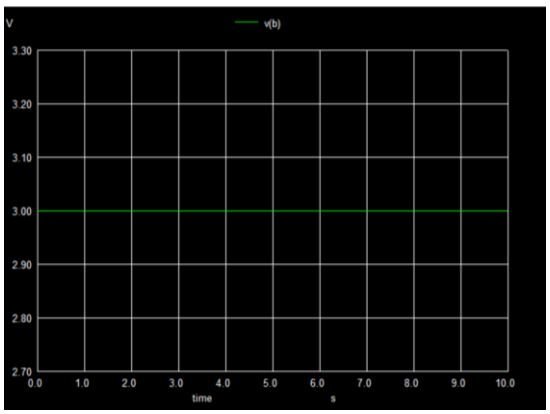

Figure 3: Ngspice plot of input b

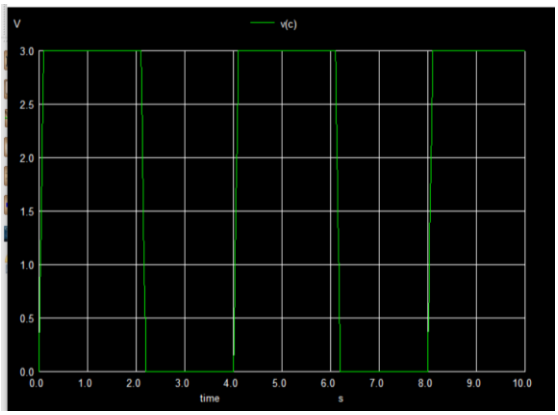

Figure 4:Ngspice plot of input c

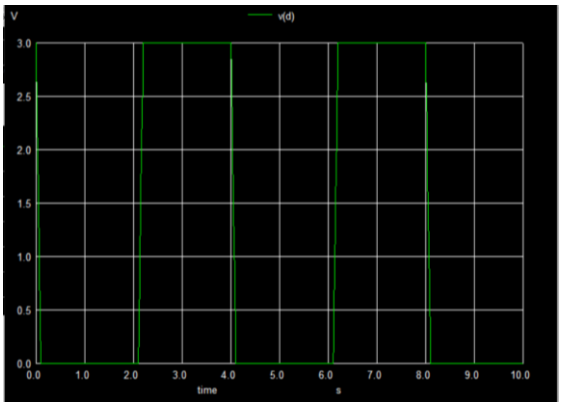

Figure 5:Ngspice plot of input d

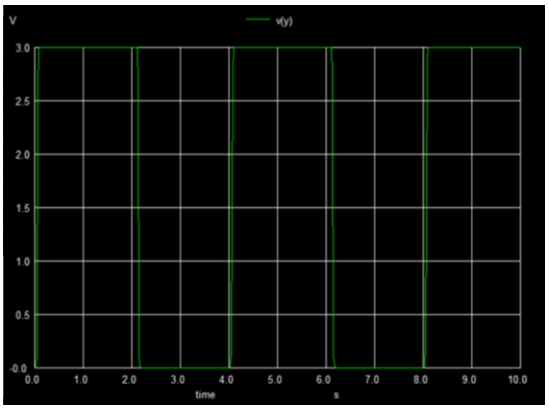

Figure 6: Ngspice plot of output Y

2.Python Plots:

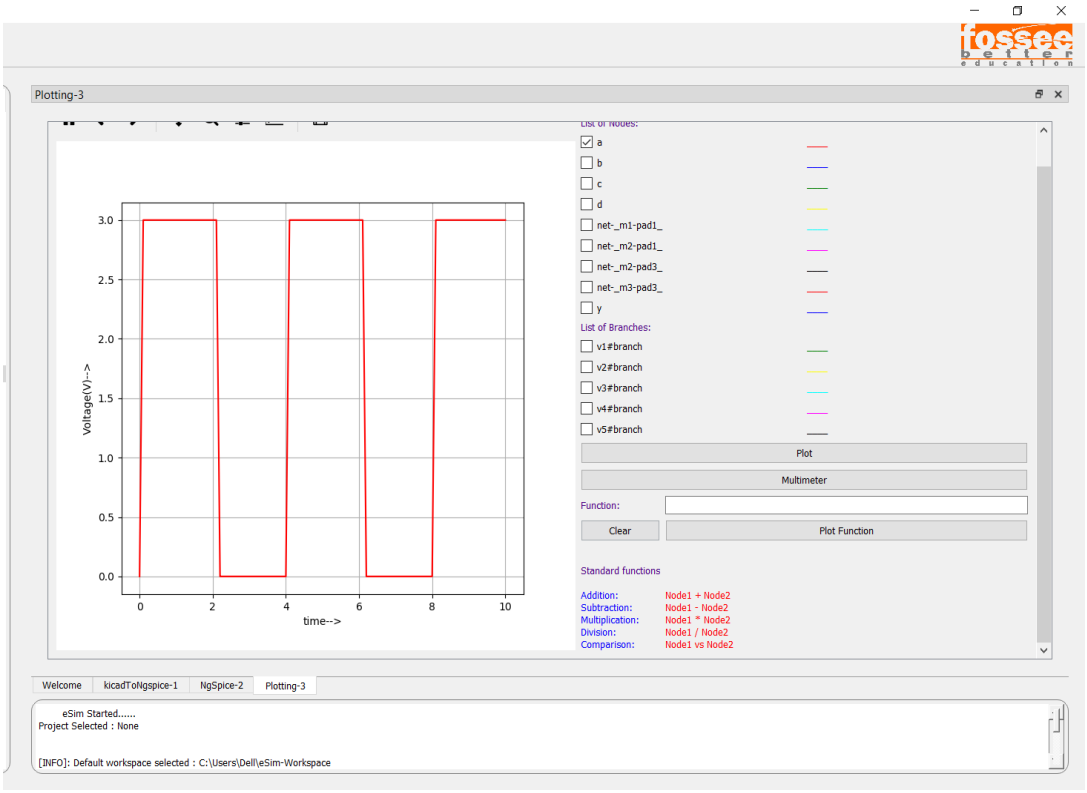

Figure 7:Python plot of input a

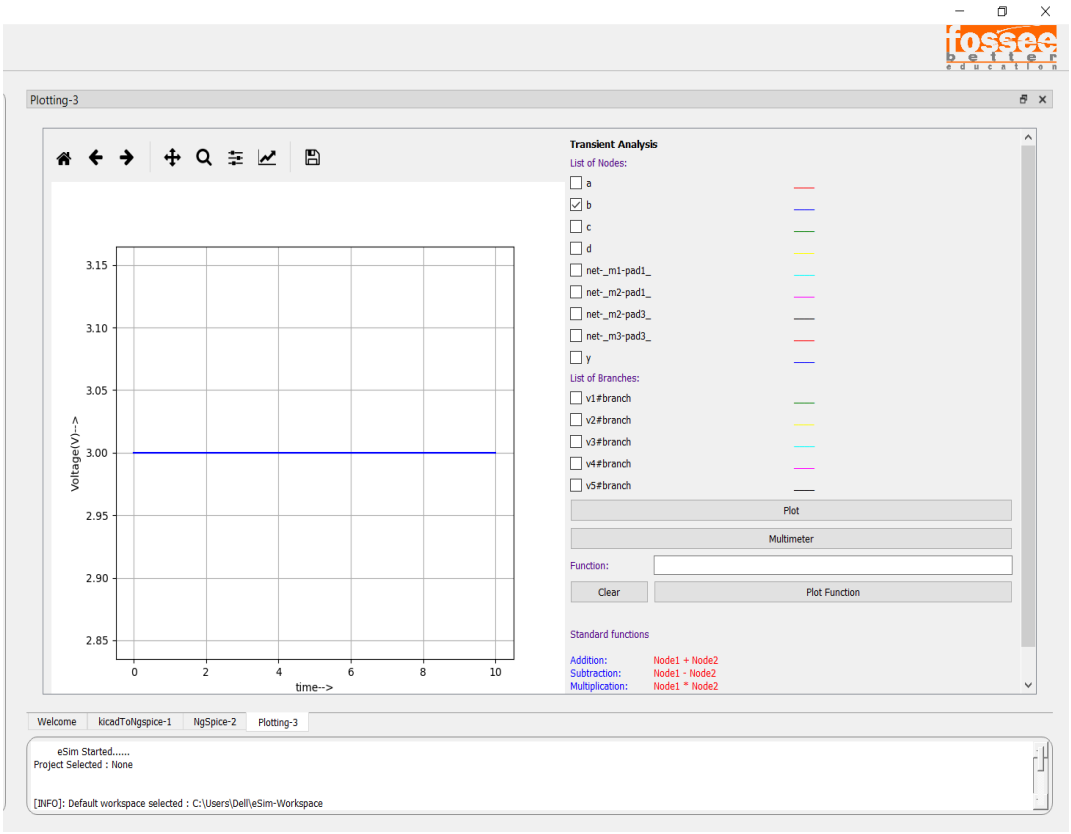

Figure 8: Python plot of input b

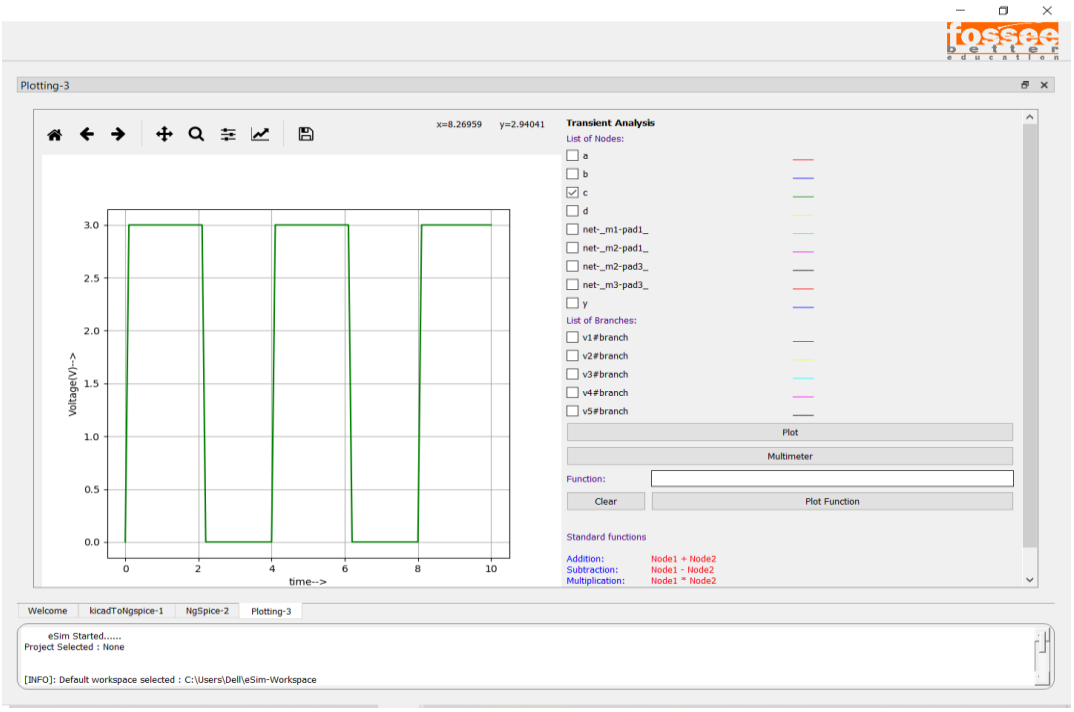

Figure 9: Python plot of input c

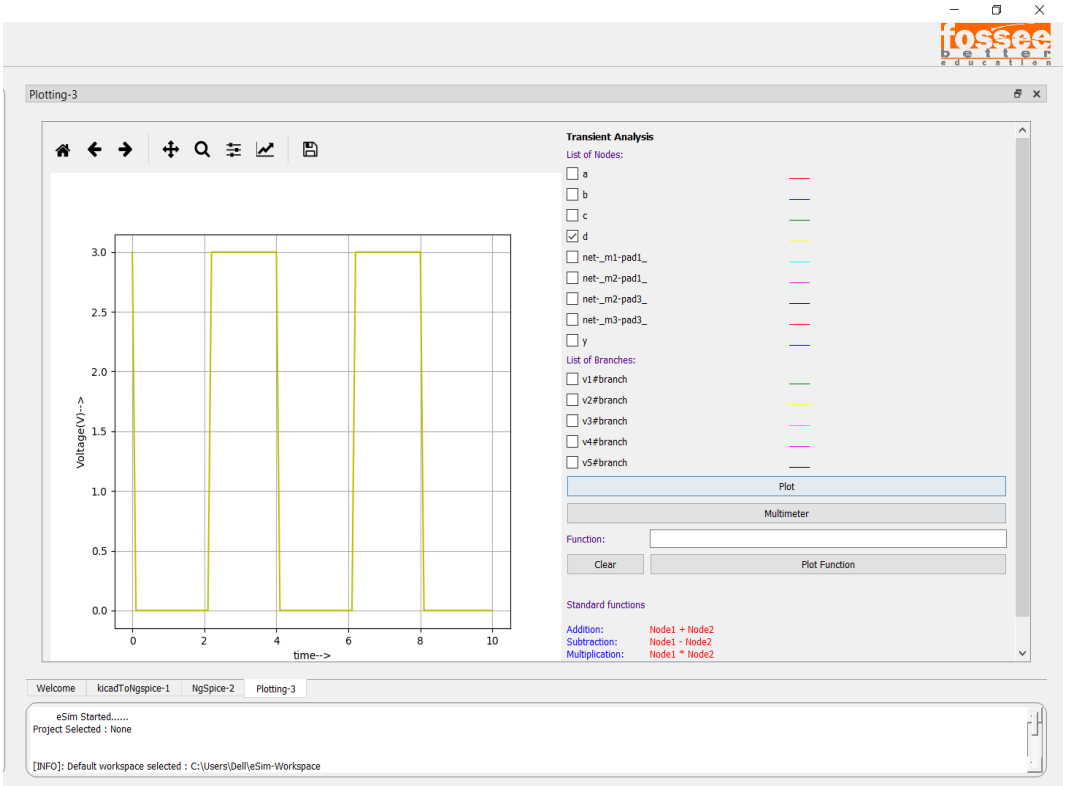

Figure 10: Python plot of input d

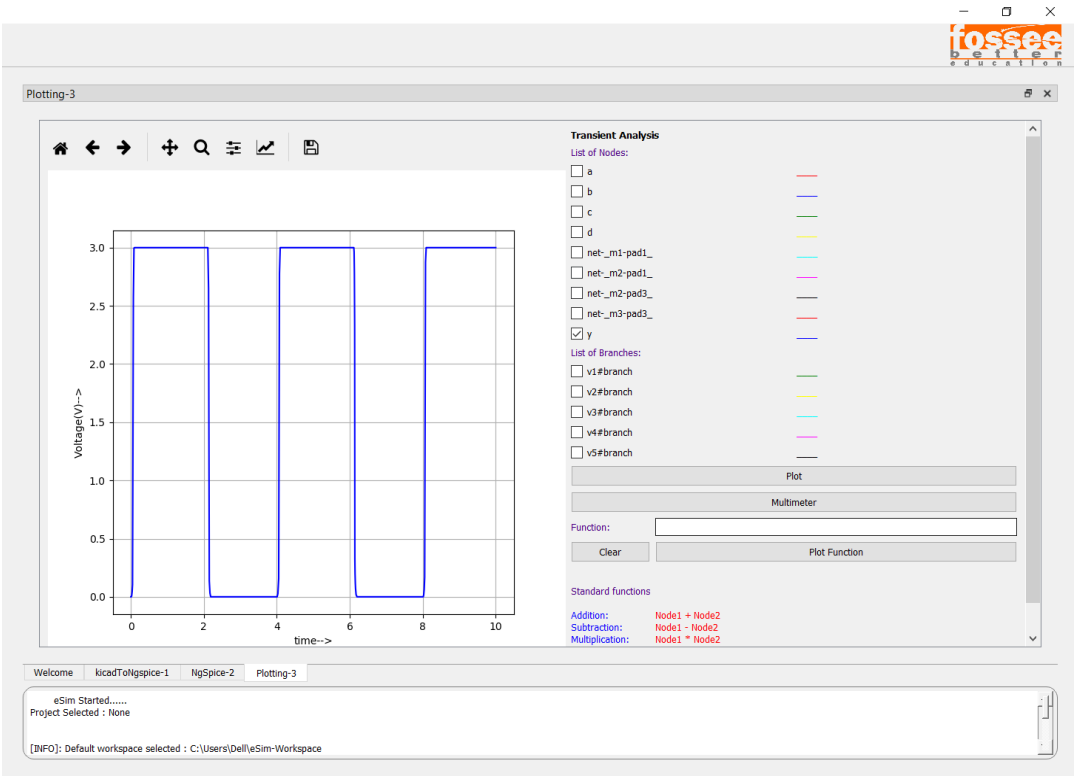

Figure 11: Python plot of input Y

Conclusion:

Thus, we have studied design of static CMOS Complex circuit function $Y = \overline{(a+b+c).d}$ using eSim and the waveforms are verified using truth table.

Source/Reference(s) :

1)CMOS VLSI Design: A circuit and systems perspective by Neil H.E.Weste, David M.Harris, fourth edition.