Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr. Maheswari. R

Title of the Project: -

Design of a Full Adder using 2 half adder usingSub circuits Builder in eSIM

Theory/Description: -

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.
A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.
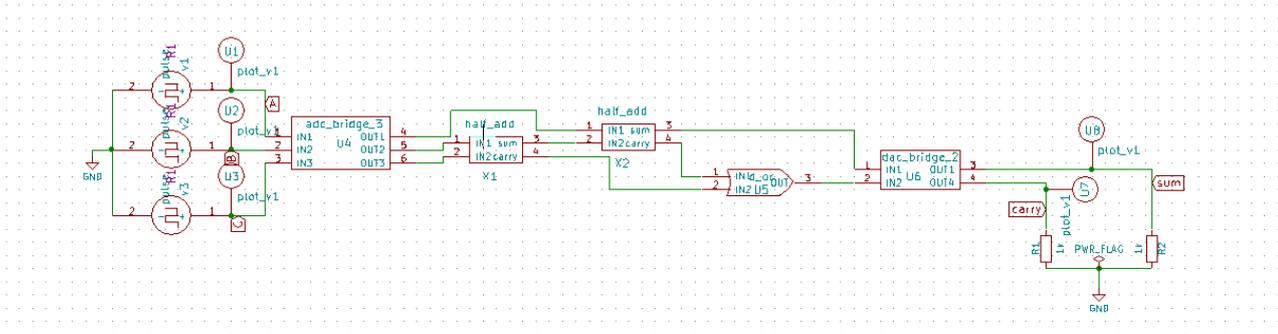We can implement a full adder circuit with the help of two half adder circuits.

Truth Table

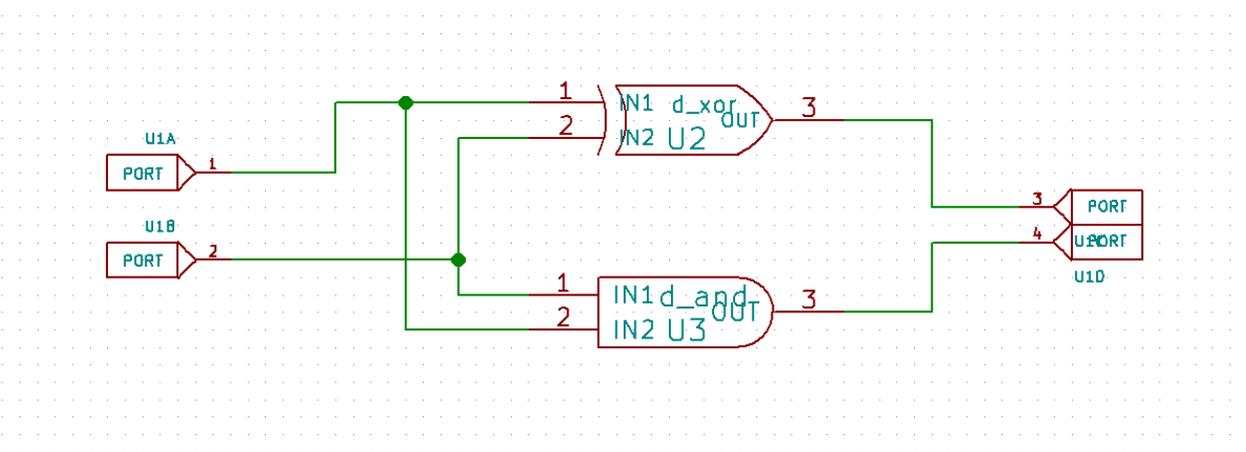| A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Circuit Diagrams: -

- This is the main functional circuit schematic for Full Adder which uses a subcircuit:

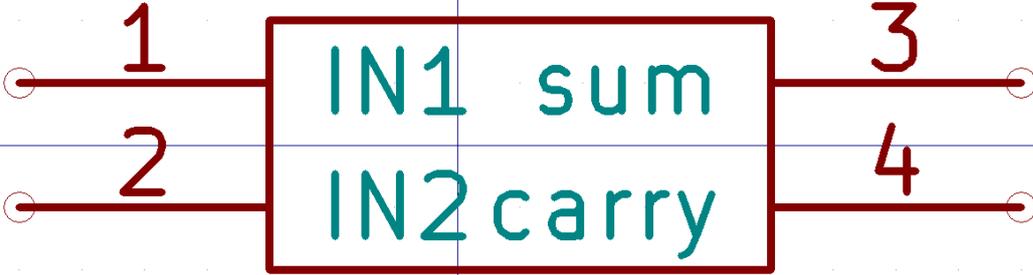**Main Circuit Schematic – Full Adder using Subcircuit**

A subcircuit is used for Full addition. The internal structure of the Half Adder is shown below:

Subcircuit Schematic for Half Adder

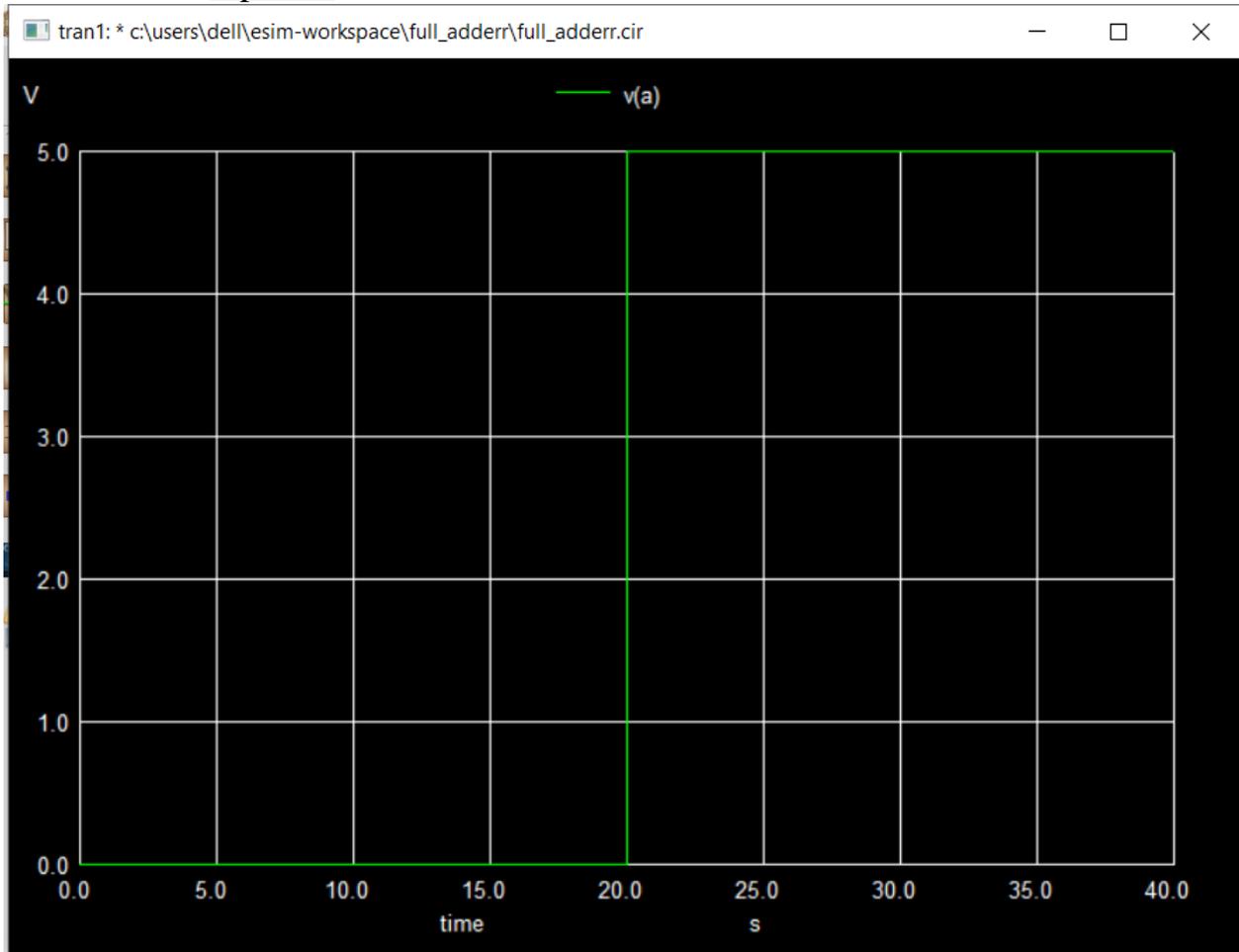- The symbol defined/designed to represent the subcircuit is shown below:
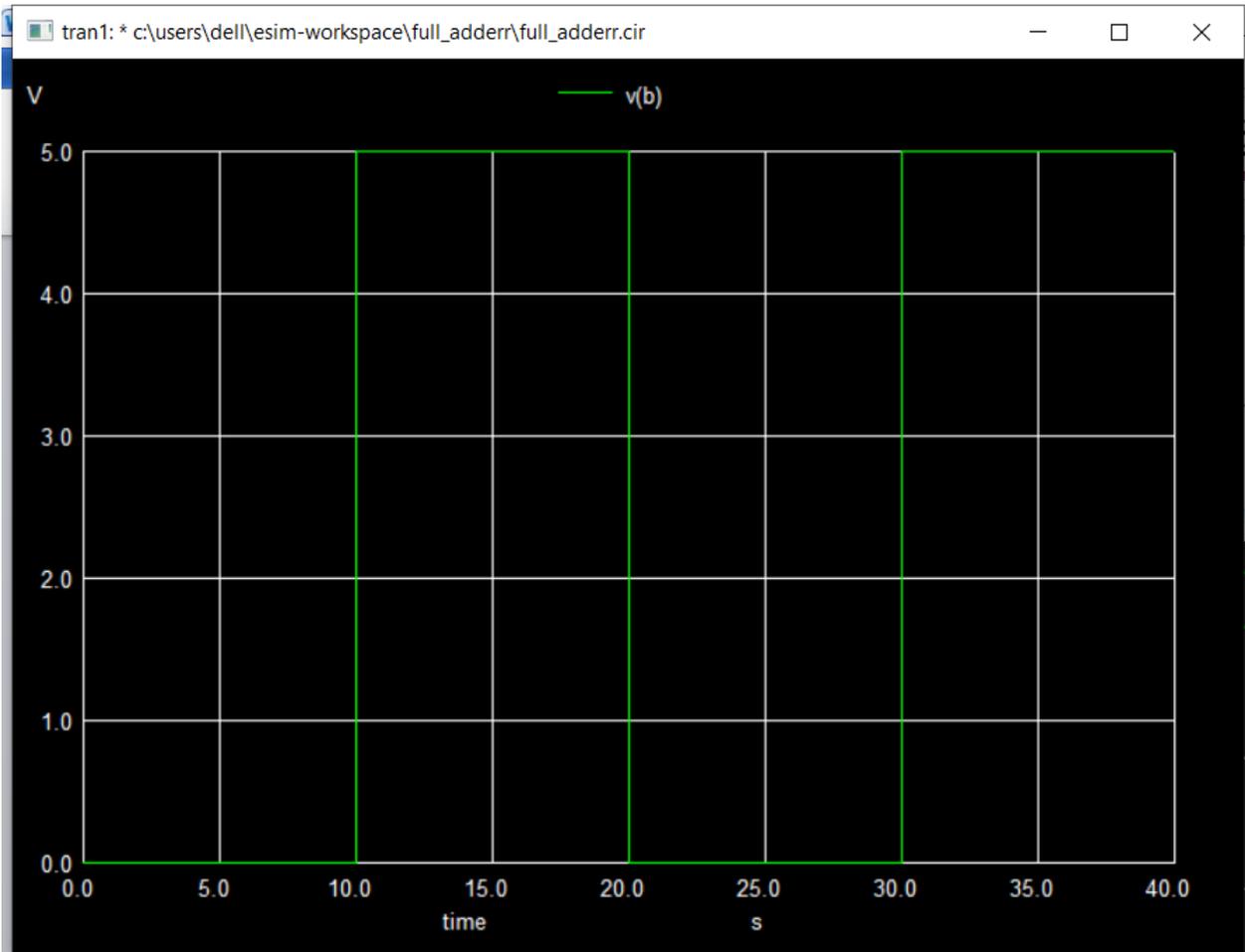
half_add

1 IN1 sum 3

2 IN2 carry 4

X?

Subcircuit Symbol for Half Adder

Result/Output: -
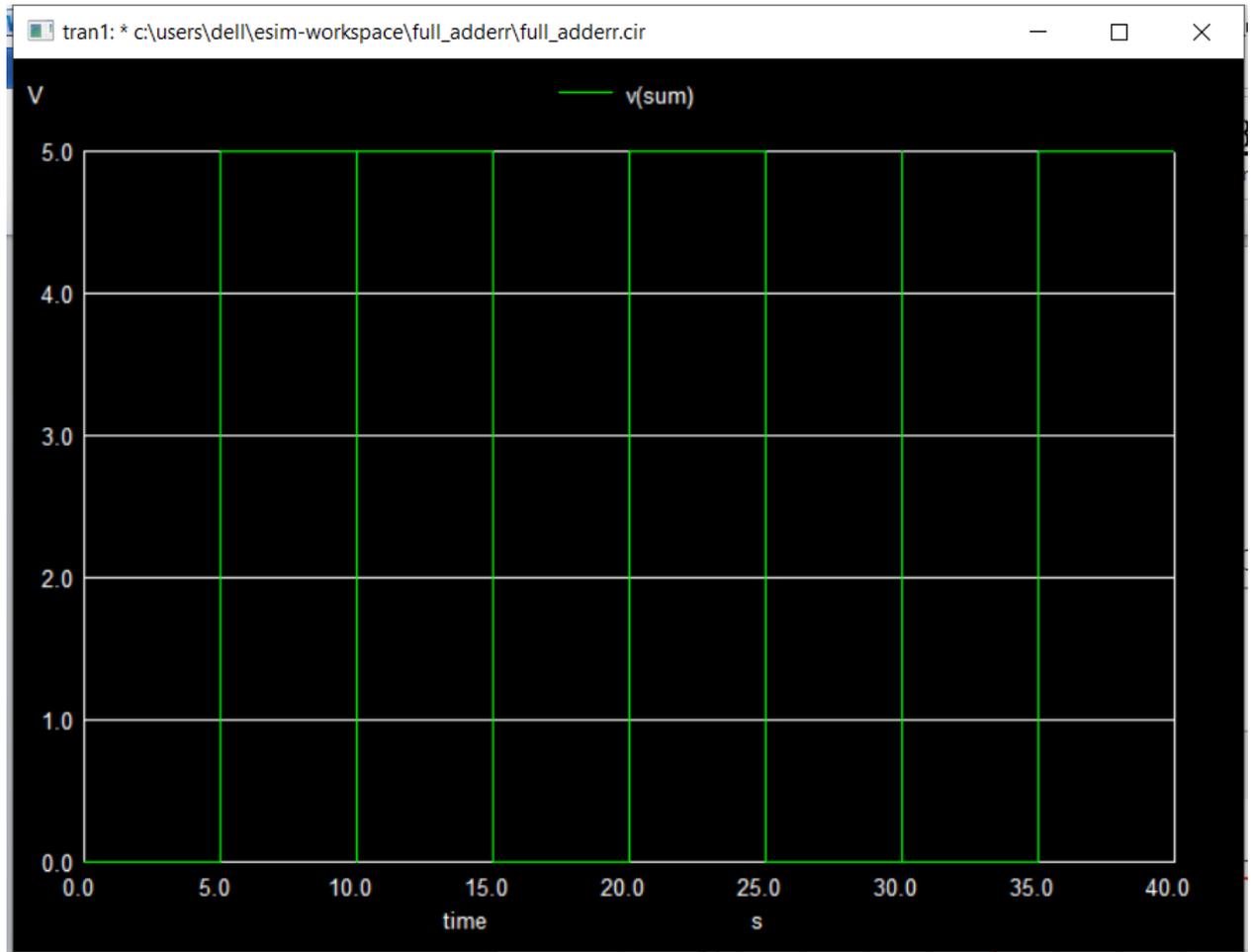
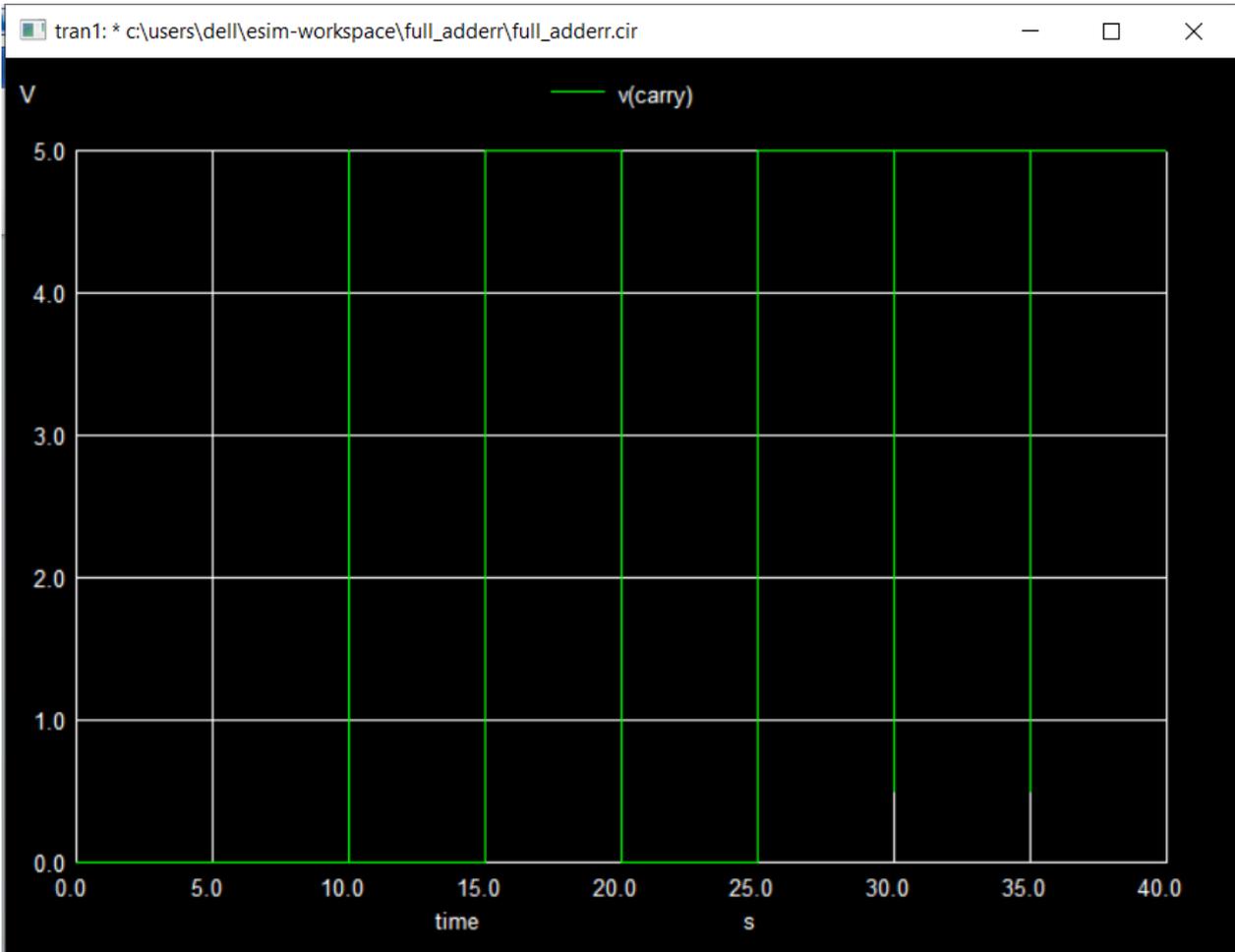- **Ngspice Plots: -**
  - Inputs: -

A

V

v(b)

B

V   —— v(c)

5.0

4.0

3.0

2.0

1.0

0.0
   0.0   5.0   10.0   15.0   20.0   25.0   30.0   35.0   40.0
                            time   s

C
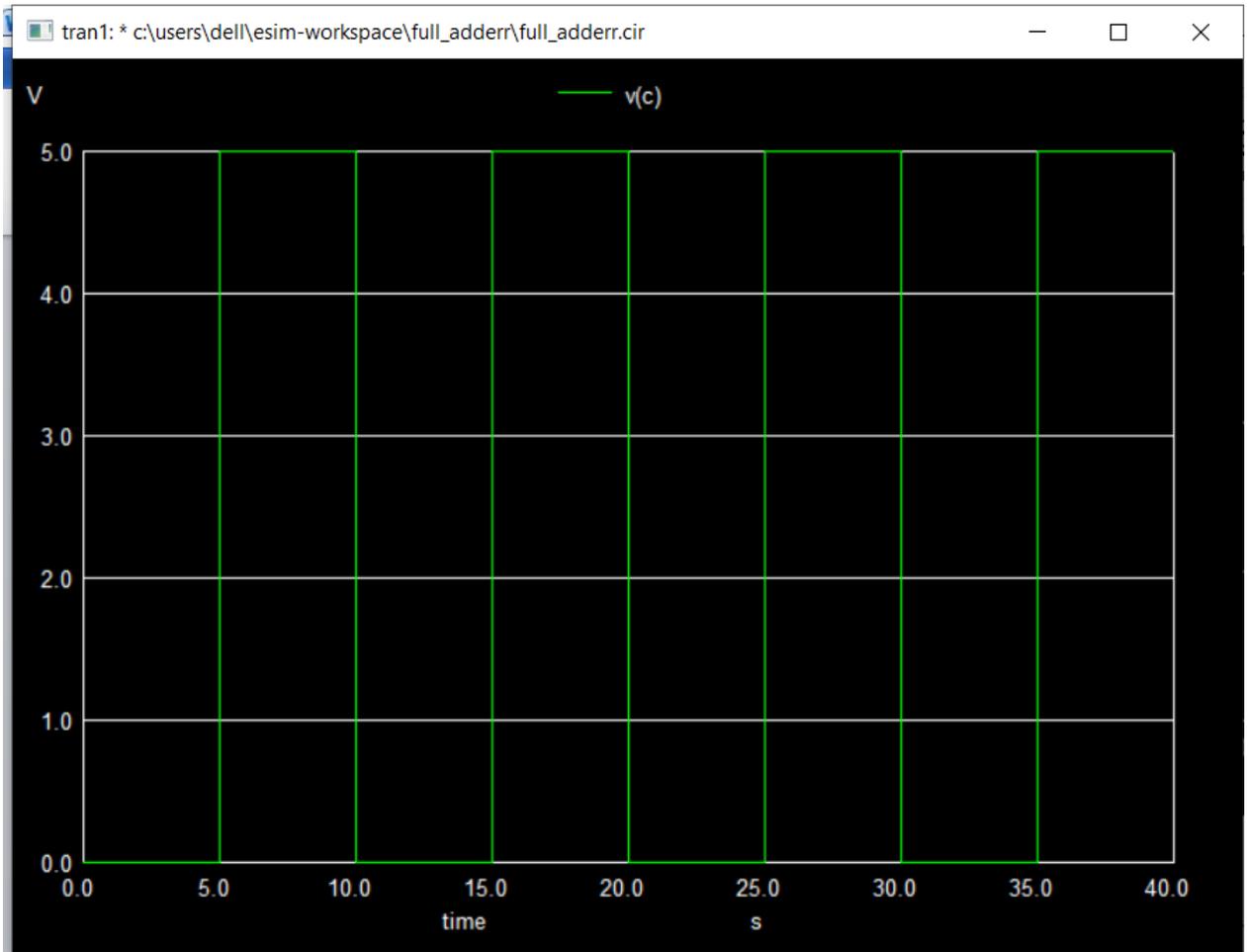
- Outputs: -

-

SUM

CARRY

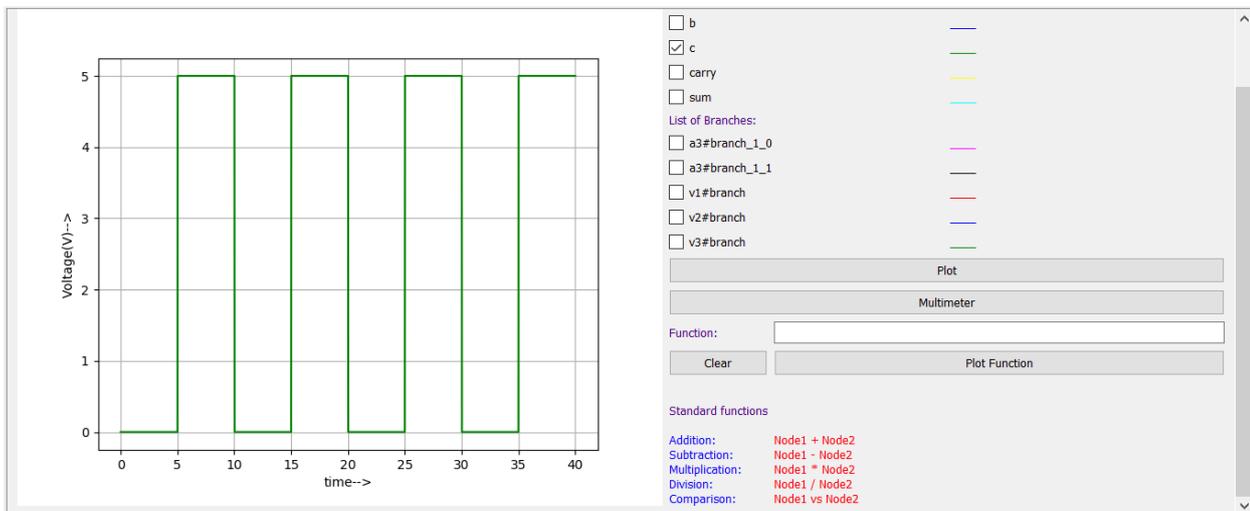- ## **Python Plots: -**
  - ### Inputs: -
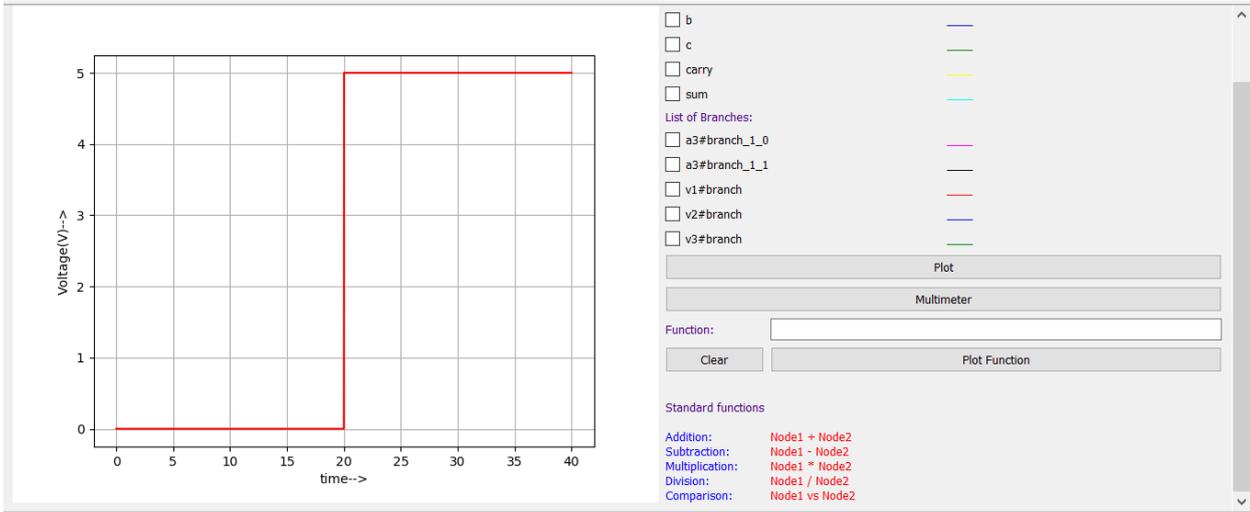
A
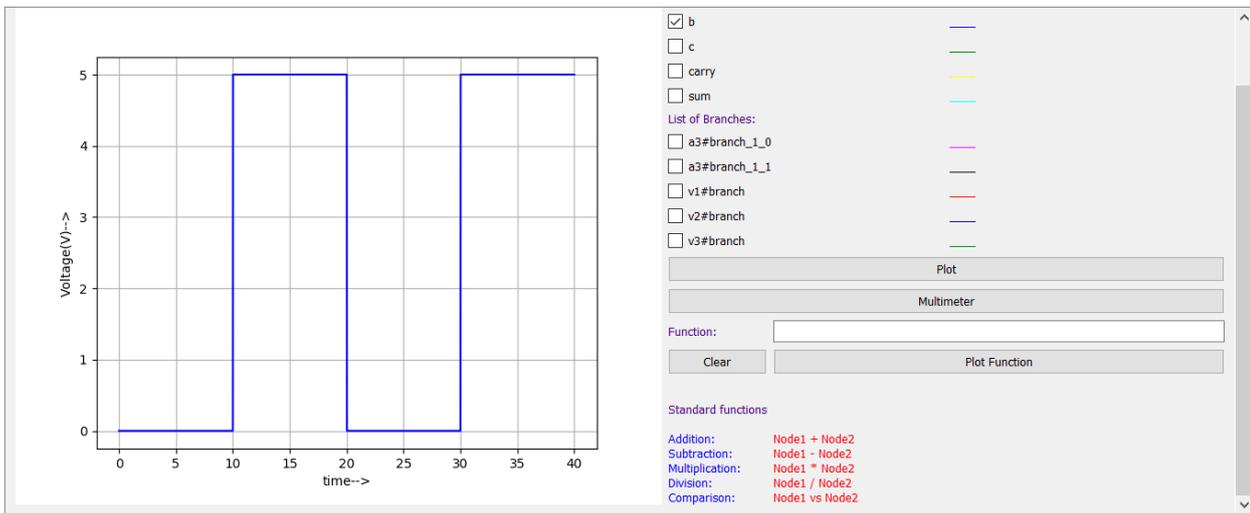
B

C
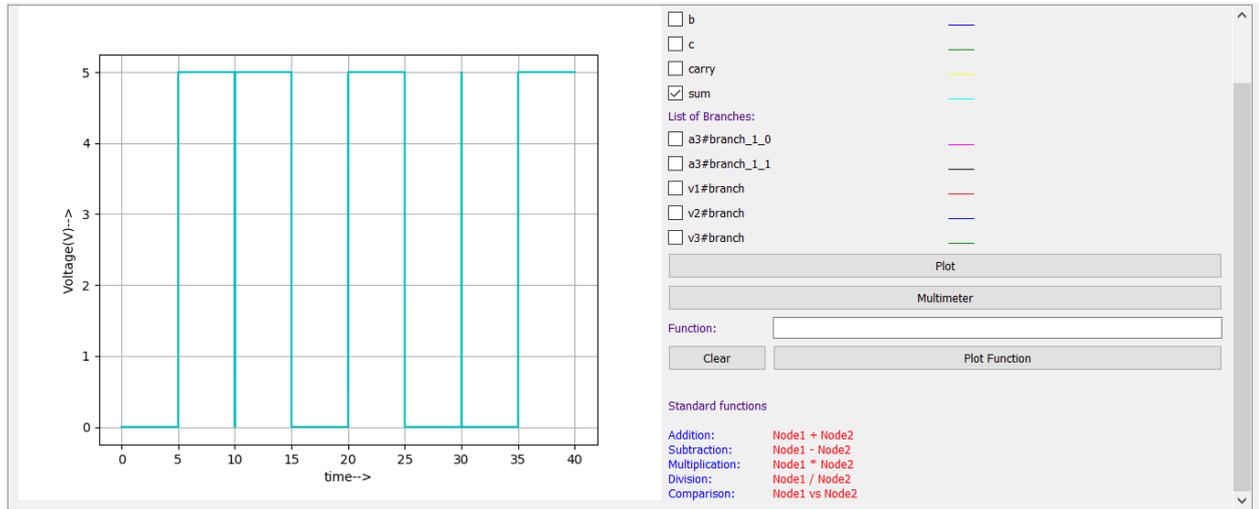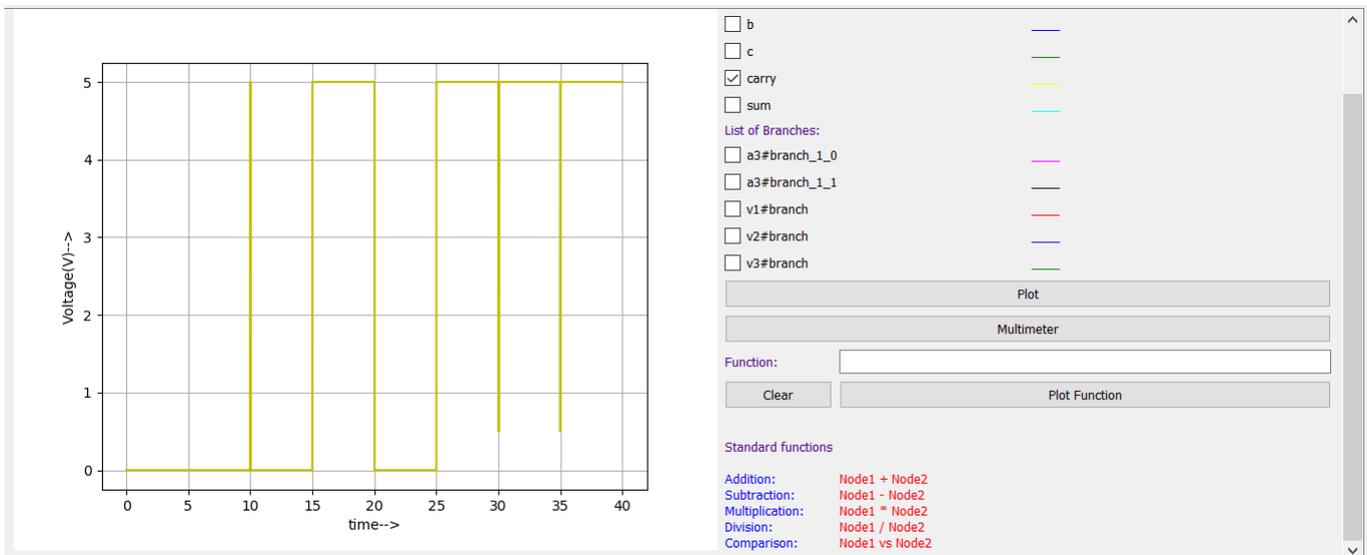
○ Outputs: -

SUM

CARRY

References: -

https://www.geeksforgeeks.org/full-adder-in-digital-logic/
https://www.javatpoint.com/full-adder-in-digital-electronics