Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr. MAHESWARI. R

Title of the Project: -

Design of XOR gate using NAND gates

Theory/Description: -

XOR gate (sometimes EOR, or EXOR and pronounced as Exclusive OR) is a digital logic gate that gives a true (1 or HIGH) output when the number of true inputs is odd.

An XOR gate implements an exclusive or A⊕B from mathematical logic; that is, a true output results if one, and only one, of the inputs to the gate is true. If both inputs are false (0/LOW) and both are true, a false output results.

XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. XOR can also be viewed as addition modulo 2.

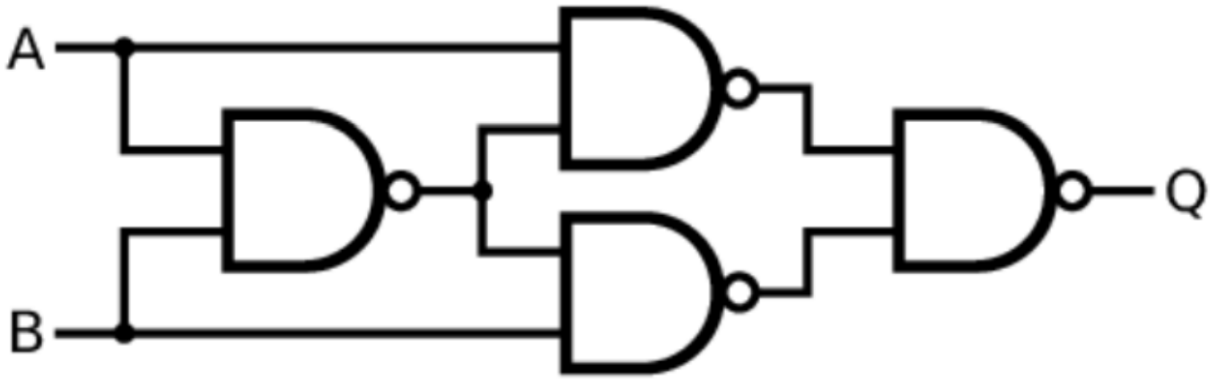
As a result, XOR gates are used to implement binary addition in computers. XOR is used in adders, subtractors, comparators, and controlled inverters. XOR gate can be implemented by only using the universal gates like only NAND gates or only NOR gates.

Truth Table for XOR Gate:

A	B	A XOR B (A ⊕ B)
0	0	0
0	1	1
1	0	0
1	1	1

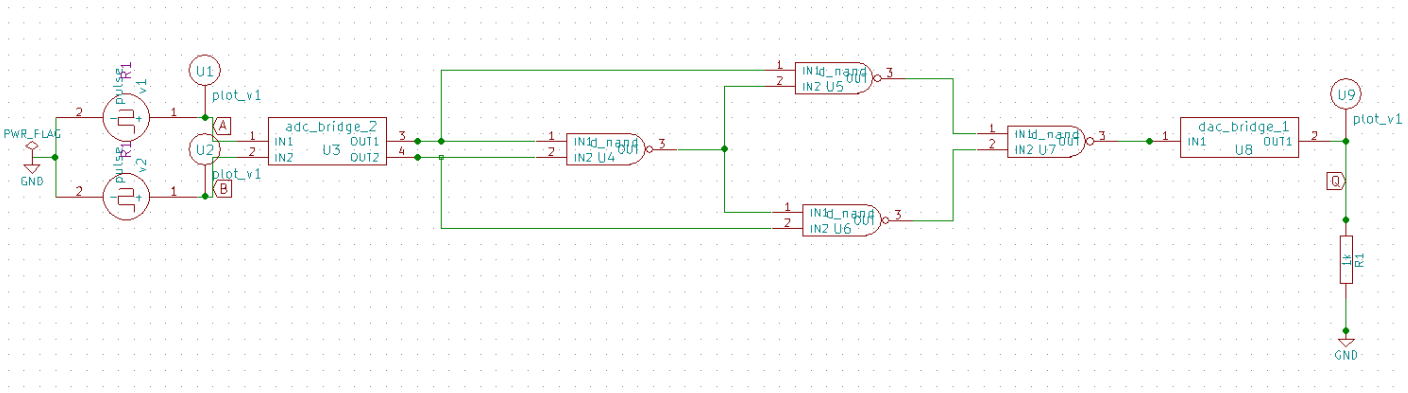
Here, A, B are inputs and A XOR B or (A ⊕ B) is output.

Circuit for Xor gate using Nand gates:

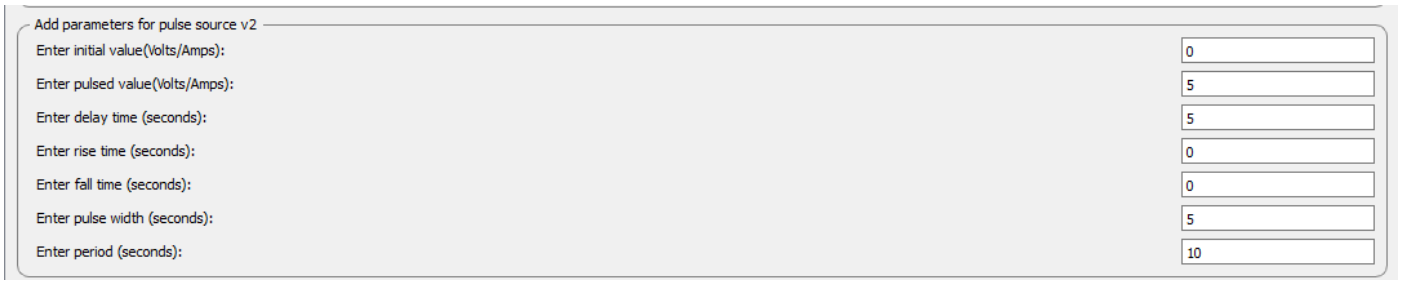


Schematic Diagram:

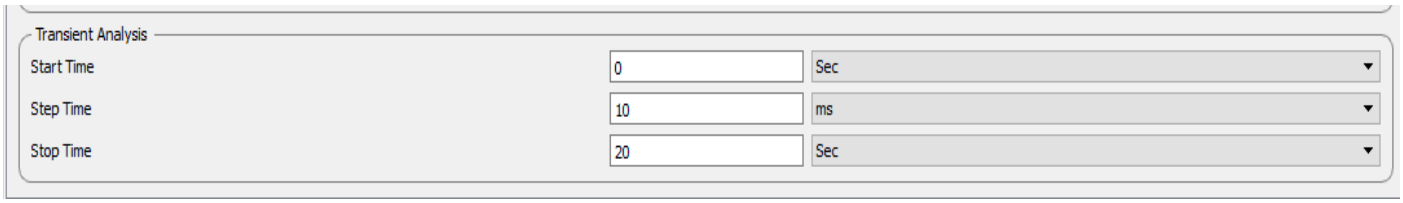
The circuit schematic for XOR gate using NAND gates in eSim is as shown below:



Source details:



Analysis:

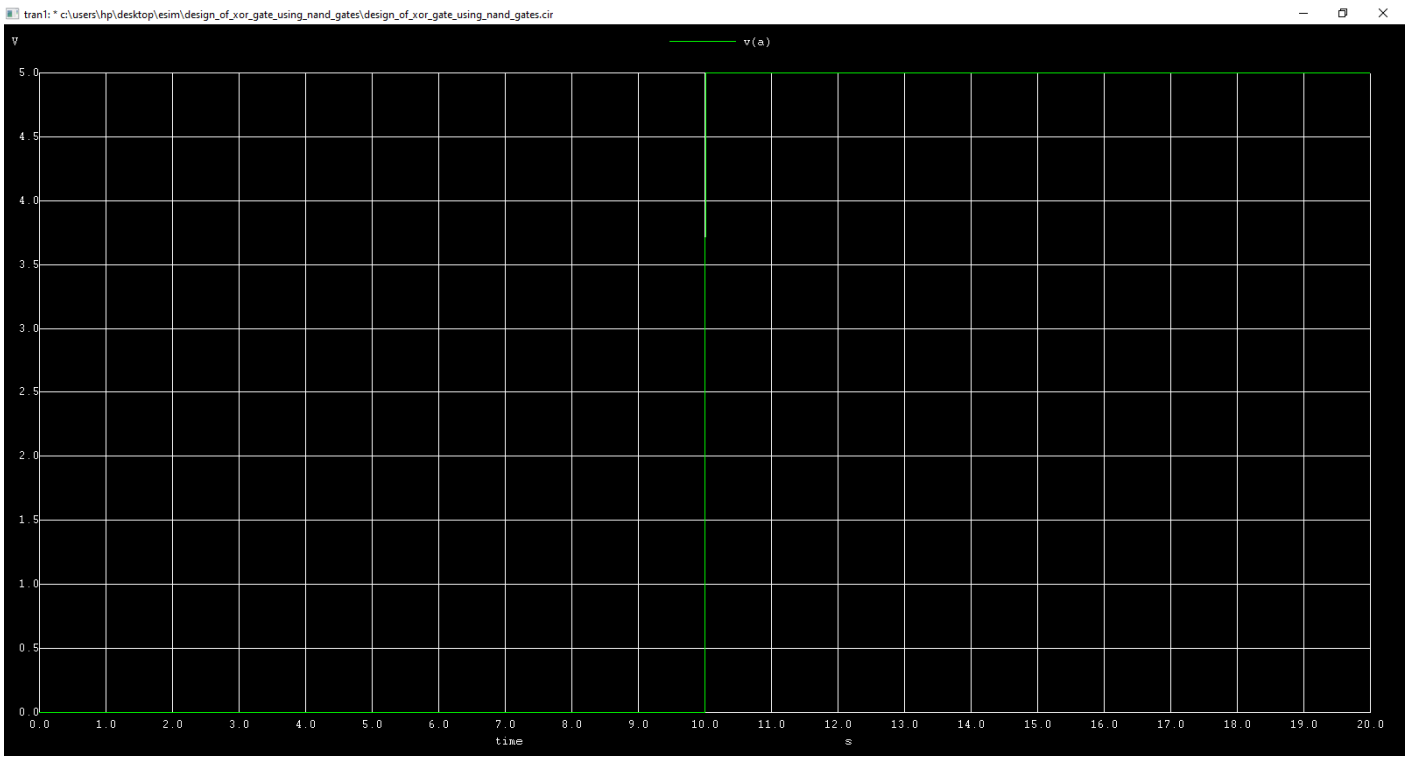


Simulation Results :

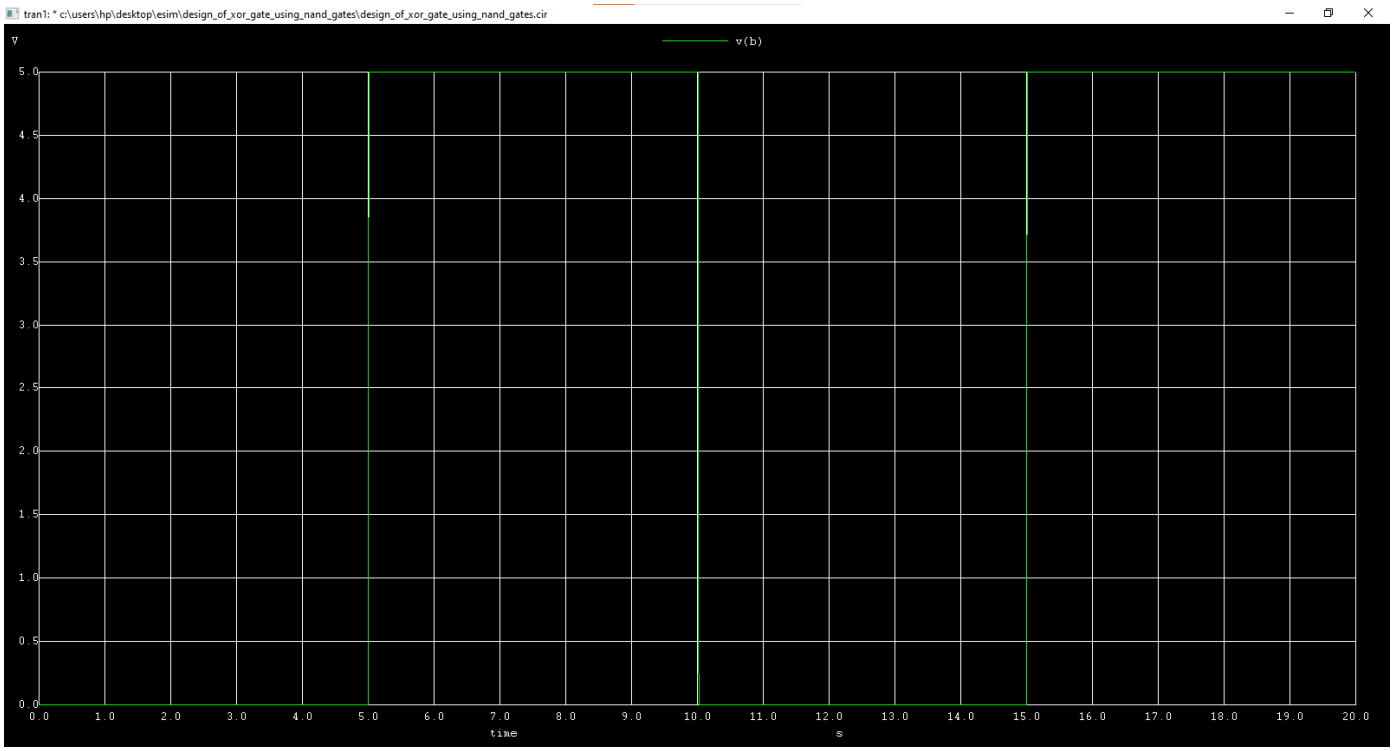
1) Ngspice plots:

Input waveforms:

A:

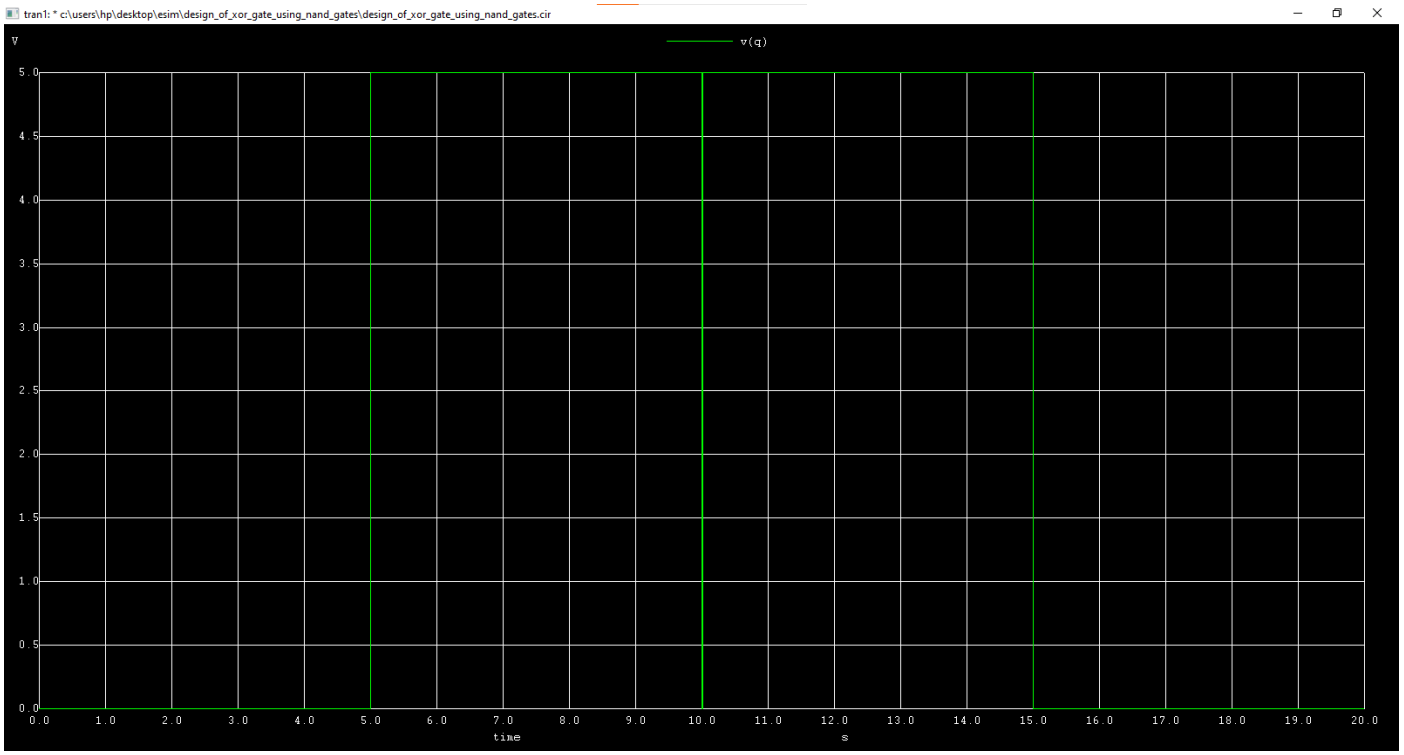


B:


tran1: * c:\users\hp\desktop\esim\design_of_xor_gate_using_nand_gates\design_of_xor_gate_using_nand_gates.cir
V
v(b)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0 14.0 15.0 16.0 17.0 18.0 19.0 20.0
time
s

Output Waveforms:

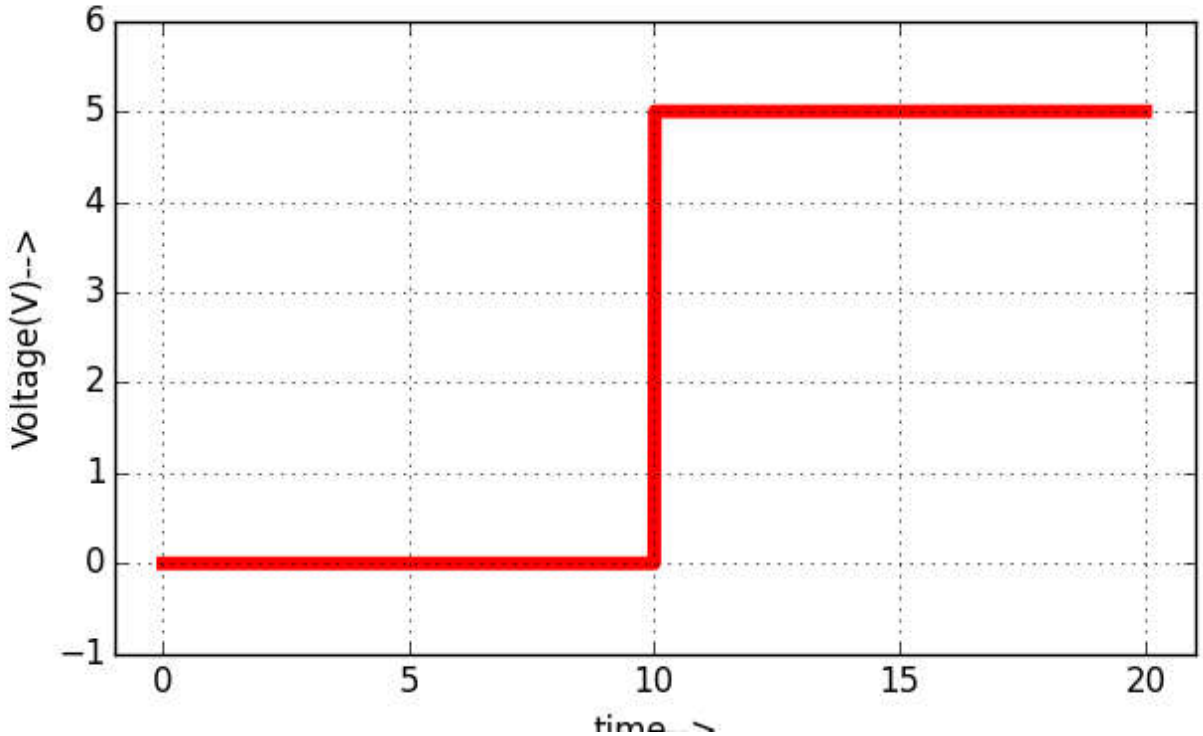
Q (A⊕B):



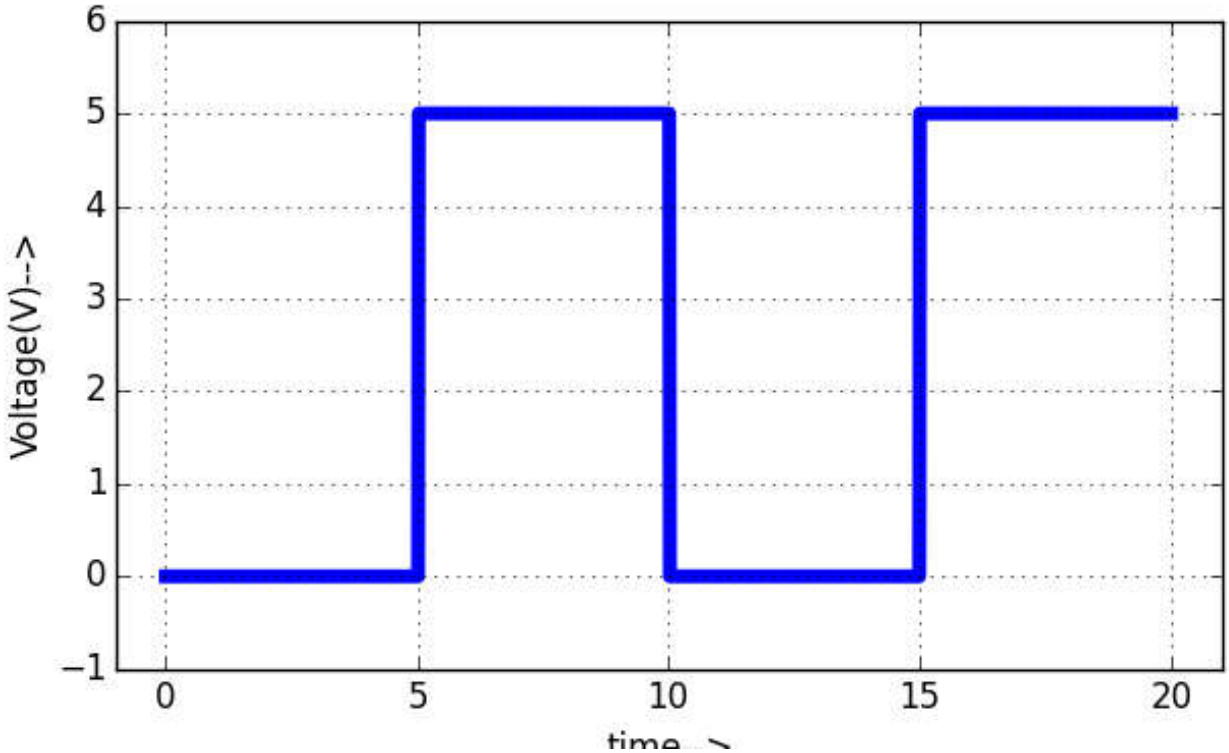
2) Python plots:

Input waveforms:

A:

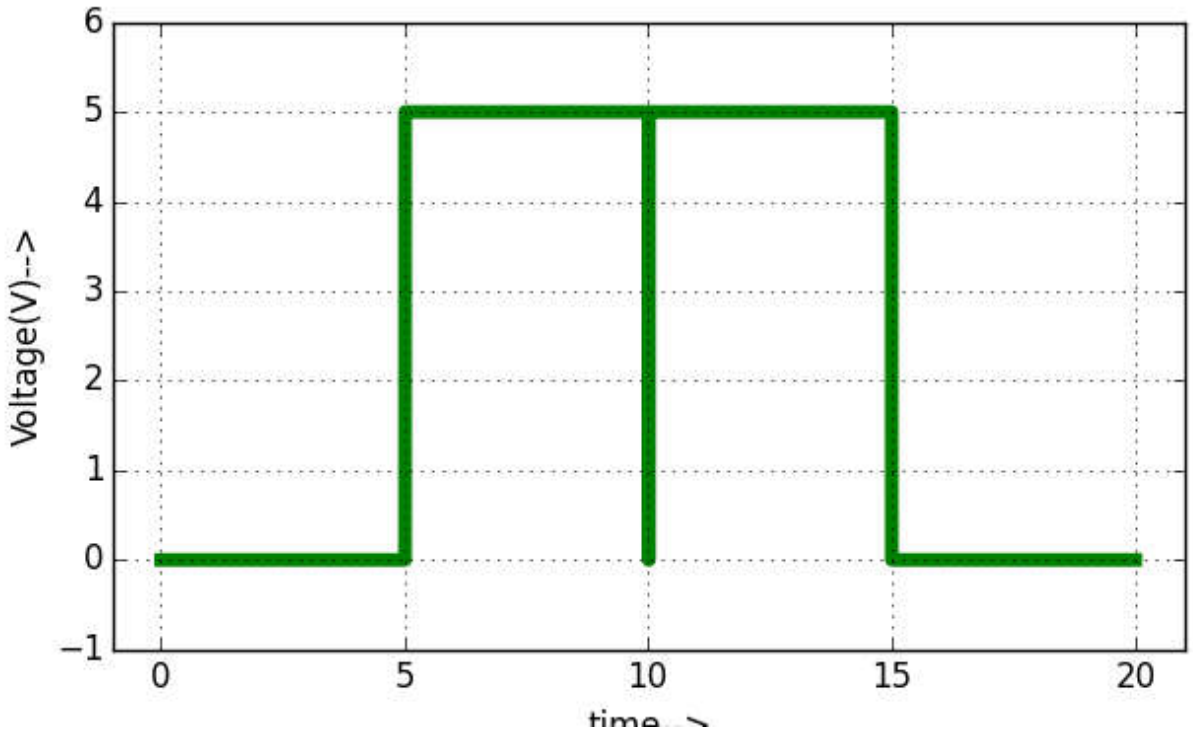


B:



Output waveforms:

Q (A⊕B):



Conclusion:

Thus, we have studied the design of Xor gate using Nand gates using eSim and we get the appropriate waveforms.

References:

- https://www.engineersgarage.com/vhdl-tutorial-7-nand-gate-as-universal-gate-using-vhdl/