Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project guide: Dr. Maheswari. R

Title of the circuit: 4 Bit Asynchronous DOWN Counter Using D Flip Flop

Theory/Description:

A 4-bit asynchronous DOWN counter is shown in above diagram. It is simple modification of the UP counter. 4-bit DOWN counter will count numbers from 15 to 0, downwards. The clock inputs of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to logic 1.

That means the flip flops will toggle at each active edge (positive edge) of the clock signal. The clock input is connected to first flip flop. The other flip flops in counter receive the clock signal input from Q output of previous flip flop, rather than Q' output.

Here Q0, Q1, Q2, Q3 represents the count of the 4-bit down counter. The output of the first flip flop will change, when the positive edge of clock signal occurs. For example, if the present count = 3, then the up counter will calculate the next

count as 2. The input clock will cause the change in output (count) of the next flip-flop.

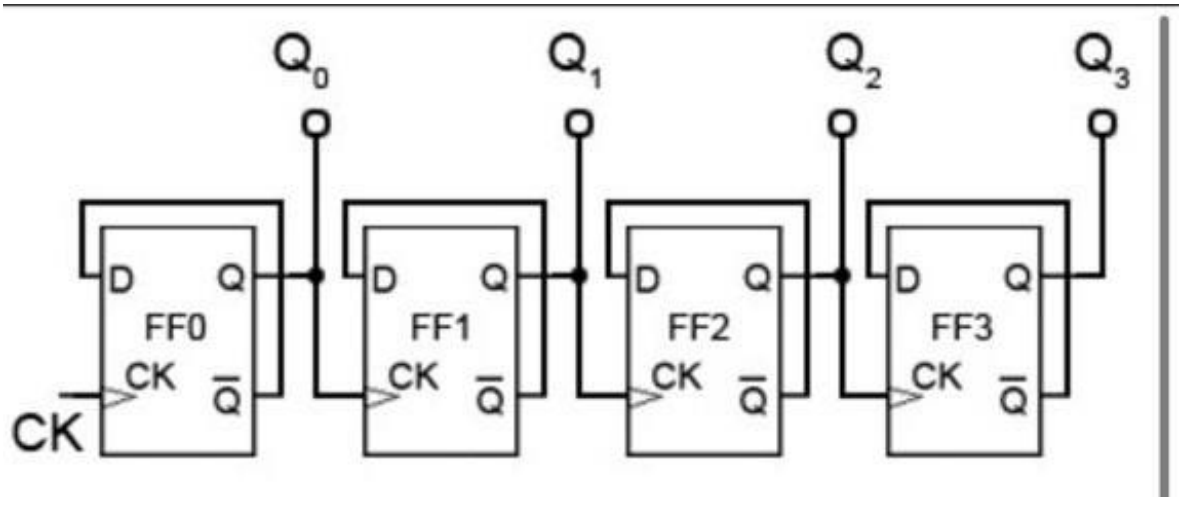
The operation of down counter is exactly opposite to the up-counter operation. Here every clock pulse at the input will reduce the count of the individual flip flop. So, the down counter counts from 15, 14, 13…0 i.e. (0 to 1510) or 11112 to 00002.

Both up and down counters are designed using the asynchronous, based on clock signal, we don't use them widely, because of their unreliability at high clock speeds.

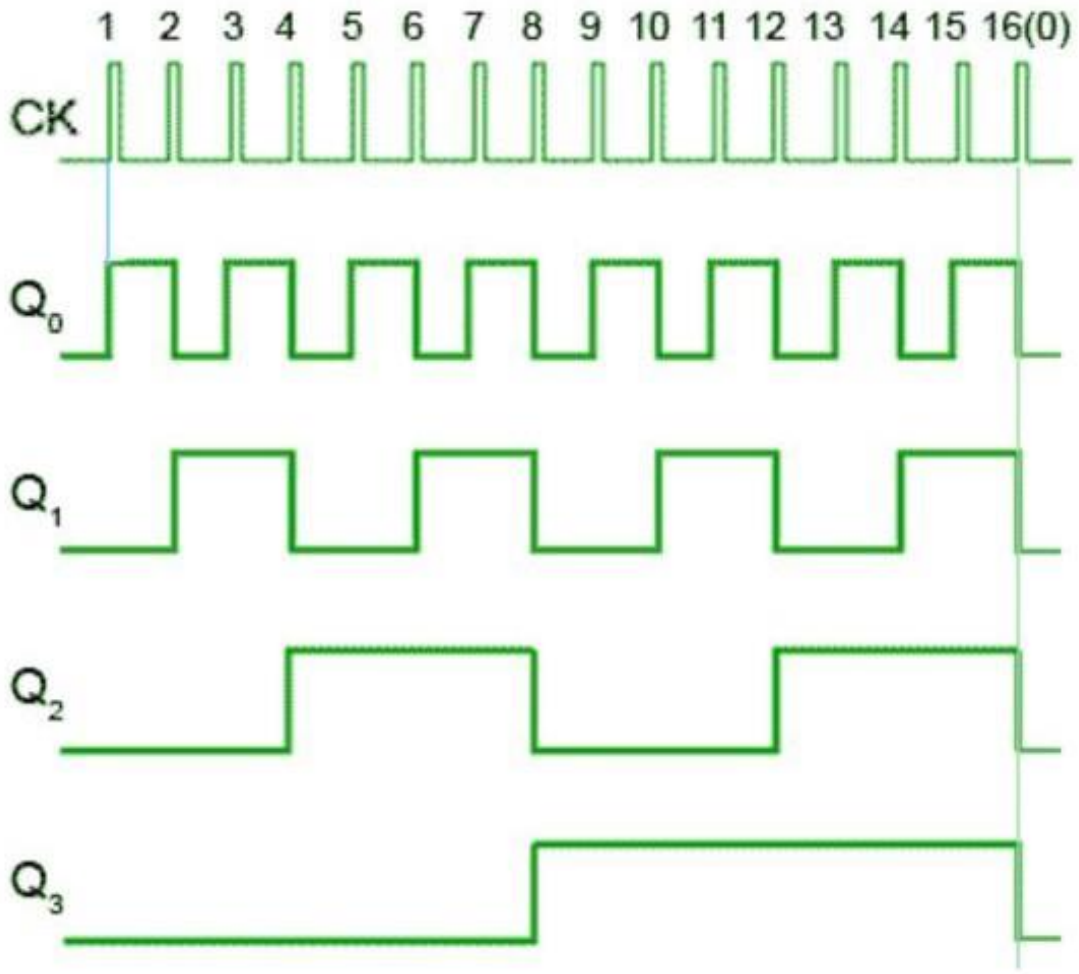
As asynchronous counters are formed by connecting flip-flops together and any number of flip-flops can be connected or "cascaded" together to form a "divide-by-n" binary counter, the modulo's or "MOD" number still applies as it does for asynchronous counters so a Decade counter or BCD counter with counts from 0 to 2^n-1 can be built along with truncated sequences.

For the 4-bit counter, we require 4 flip flops and we can generate 2^4 = 16-1=15 states and count (1111 1110 … 0000).

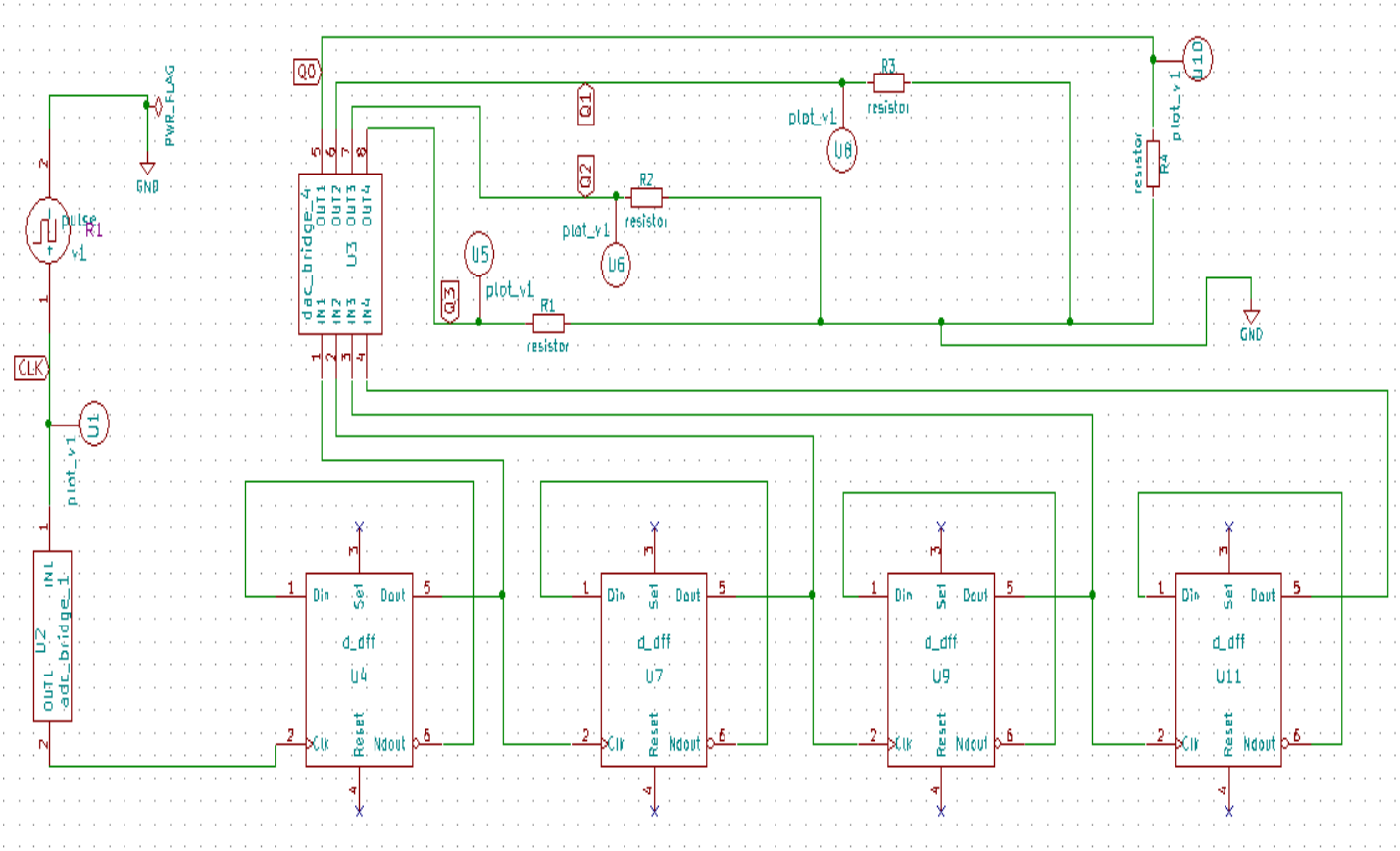
Circuit diagram:



Output:

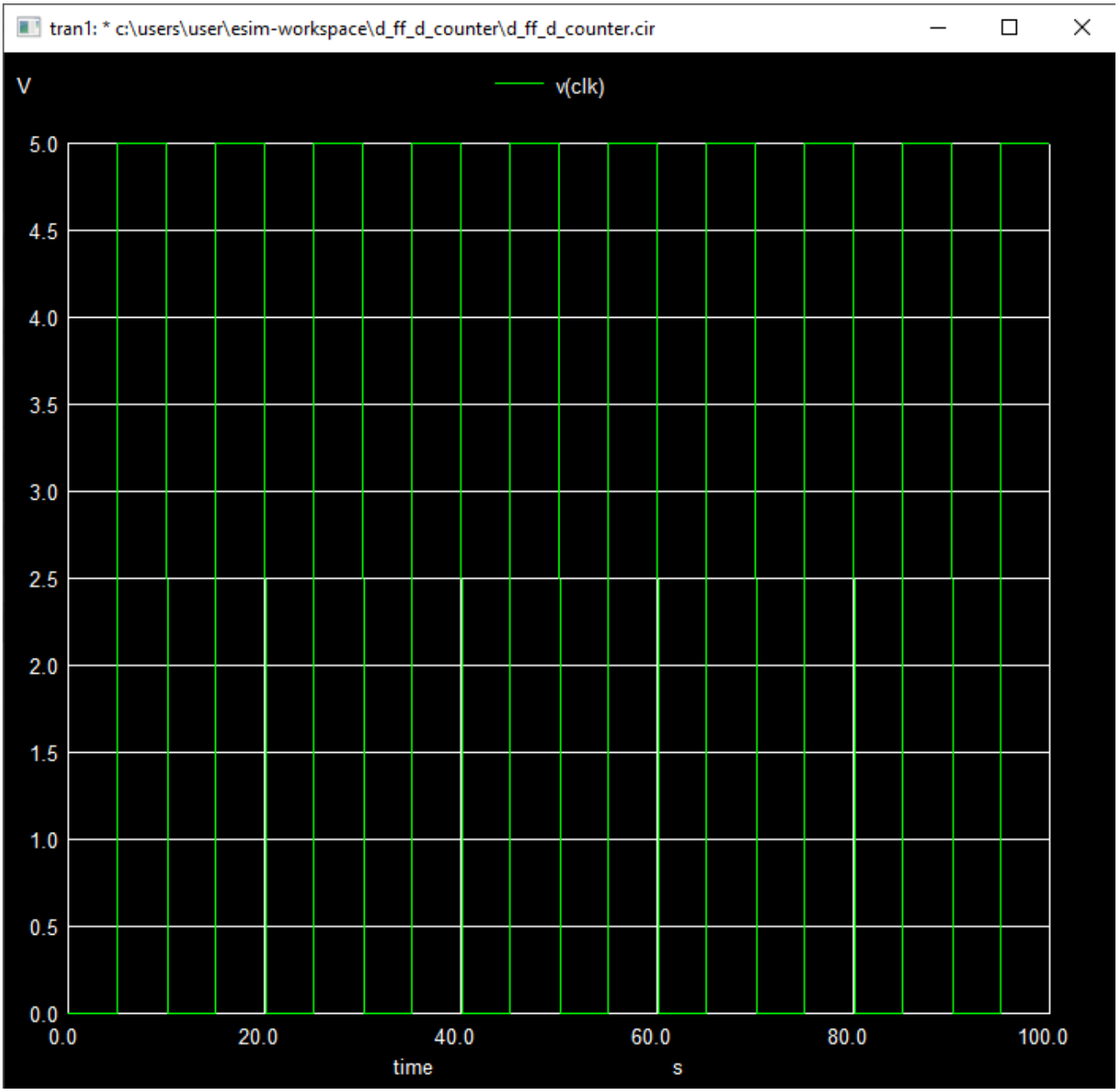


Esim circuit design:

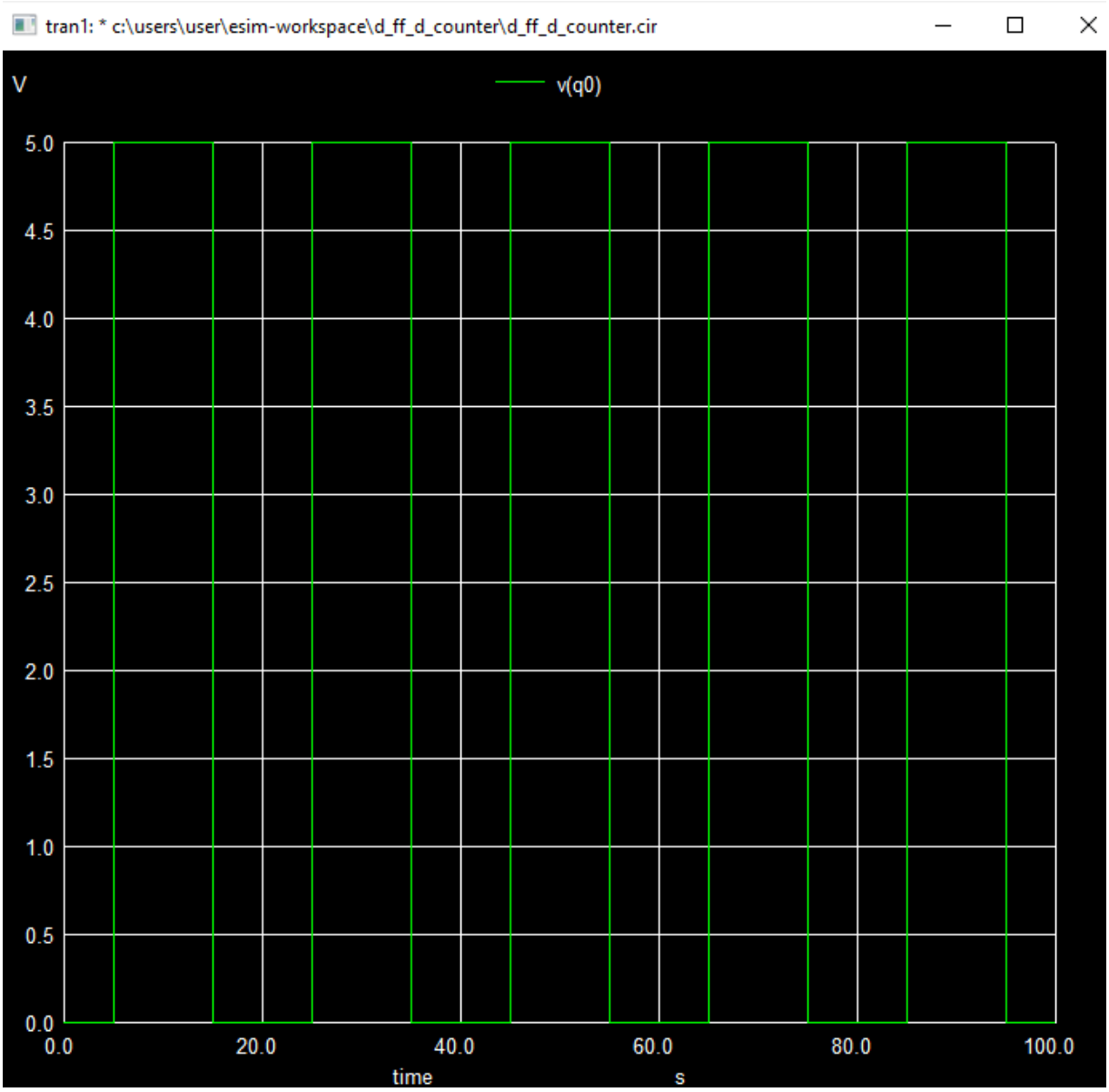


Output [Ngspice]:

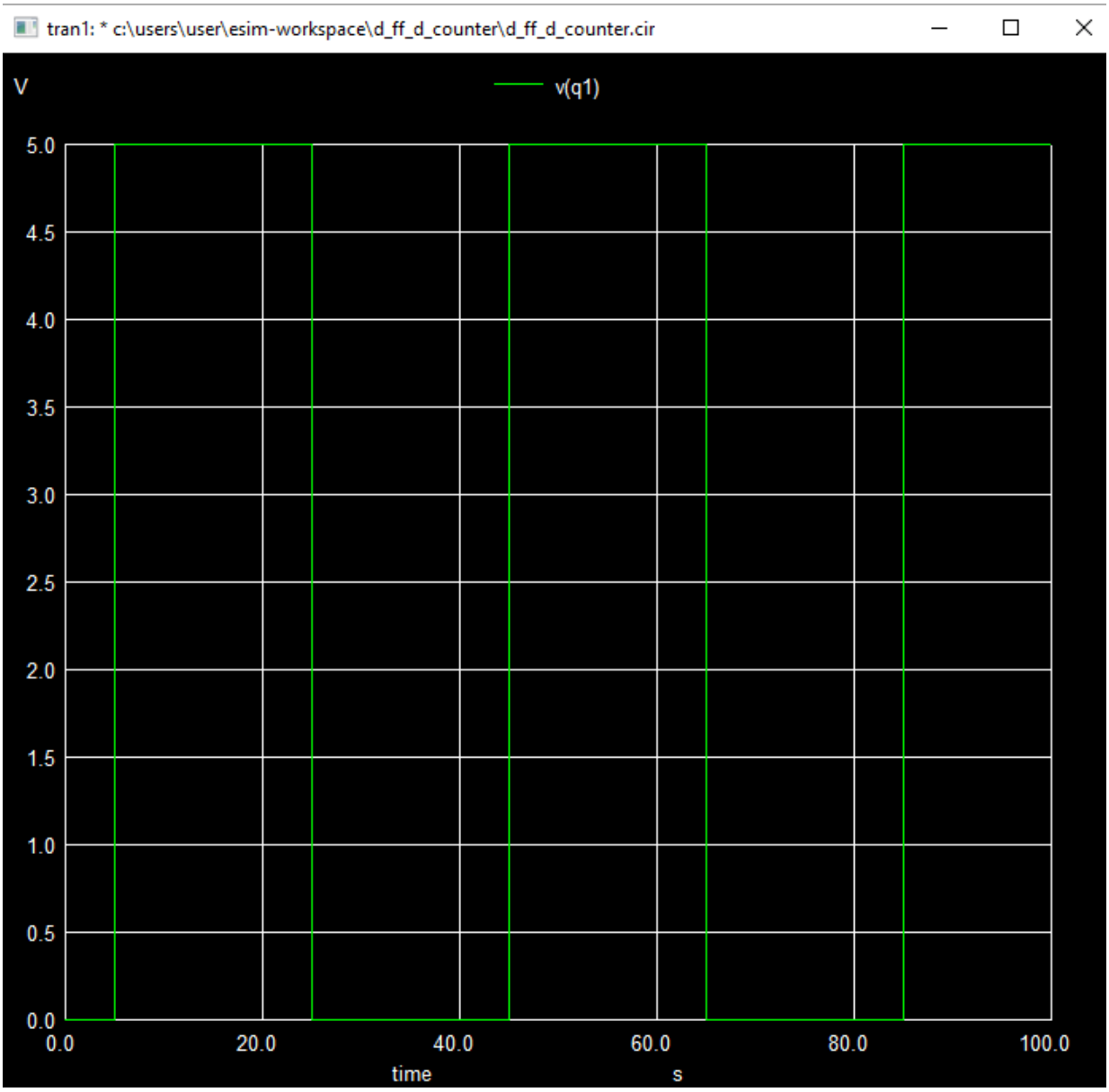
CLK


tran1: * c:\users\user\esim-workspace\d_ff_d_counter\d_ff_d_counter.cir
V
v(clk)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
s

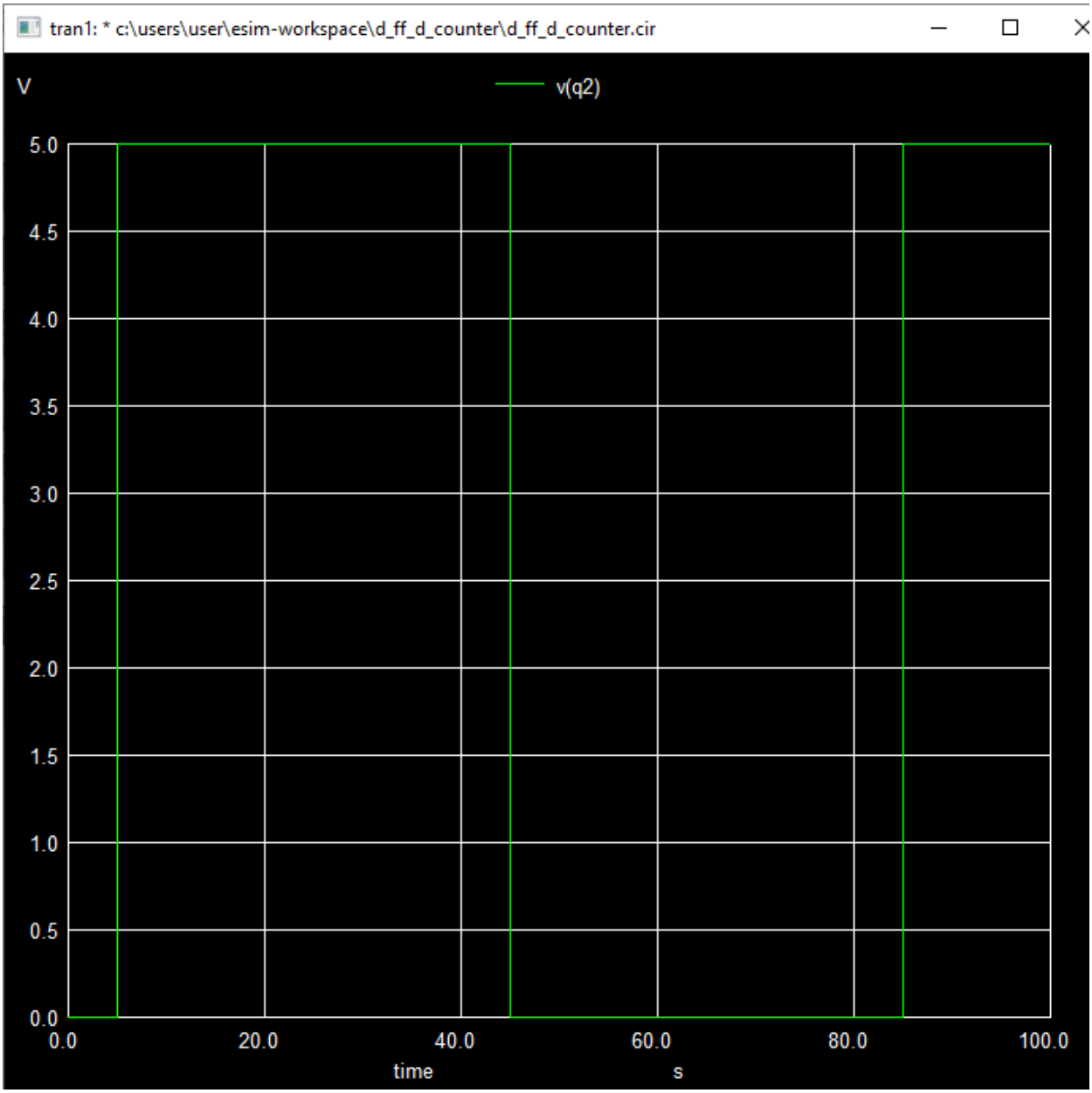
Q0


tran1: * c:\users\user\esim-workspace\d_ff_d_counter\d_ff_d_counter.cir
V
v(q0)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
s

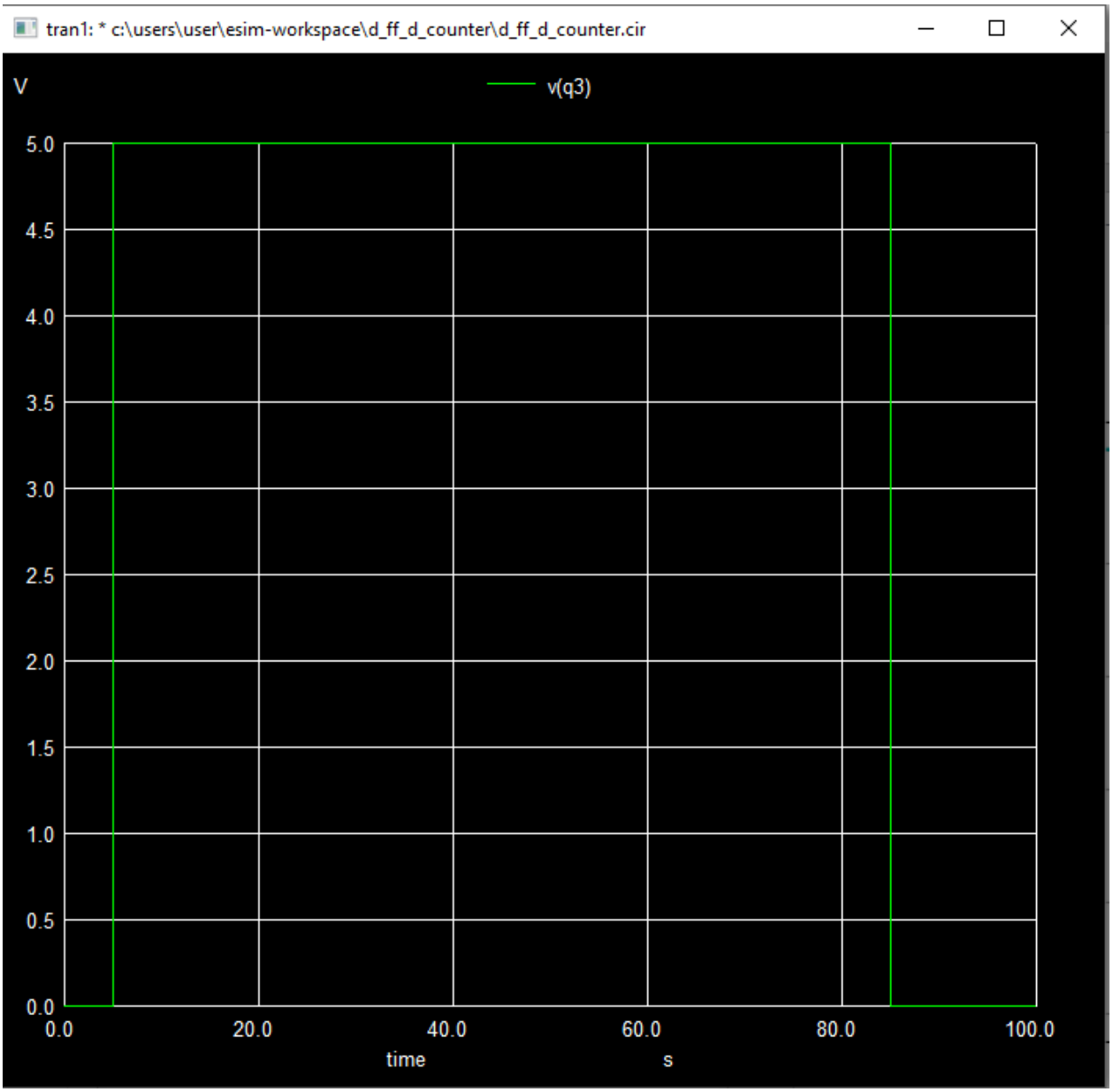
Q1


tran1: * c:\users\user\esim-workspace\d_ff_d_counter\d_ff_d_counter.cir
V
v(q1)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
s

Q2

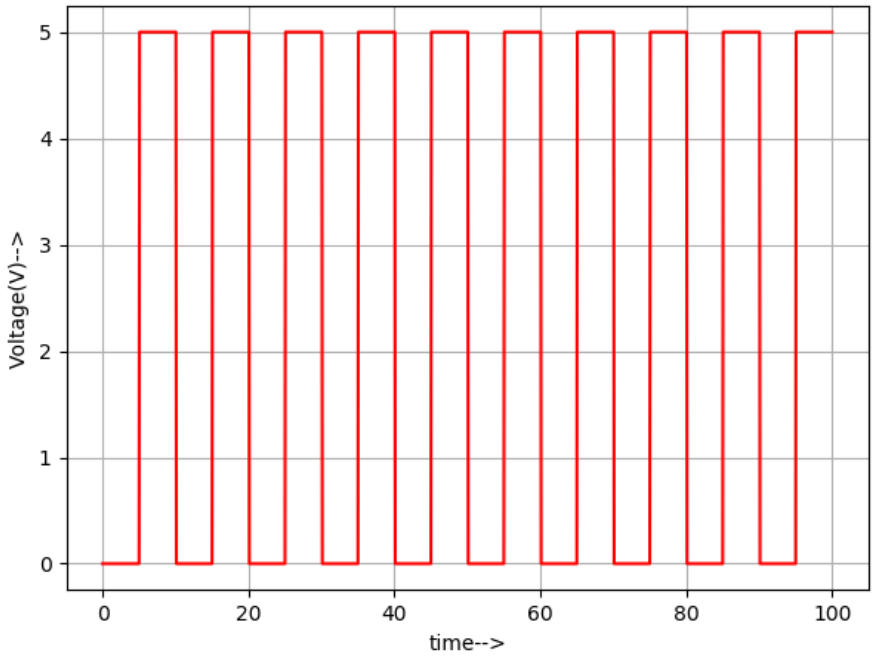

tran1: * c:\users\user\esim-workspace\d_ff_d_counter\d_ff_d_counter.cir
V
v(q2)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
s

Q3

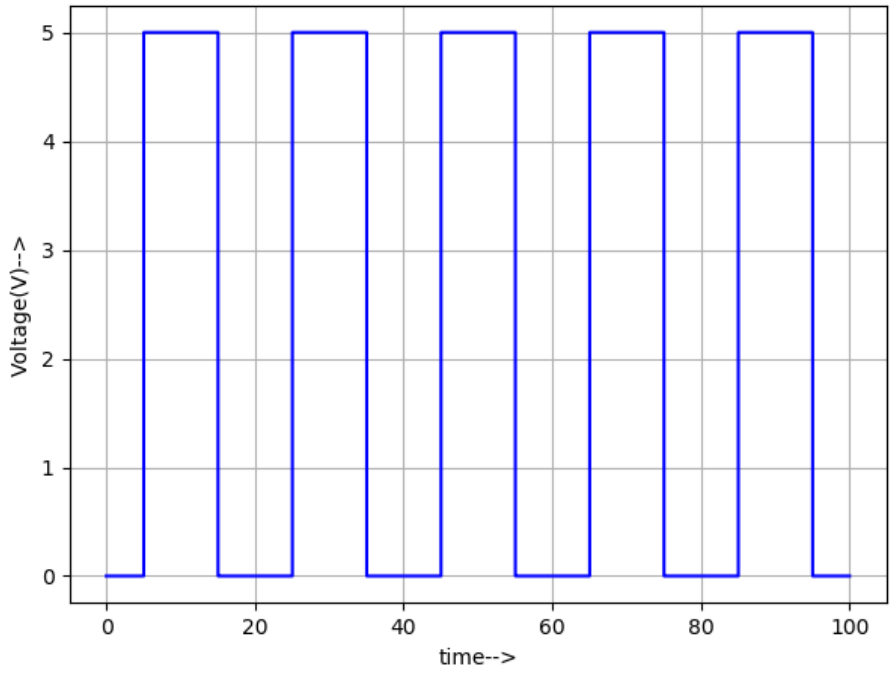


Output [python plot]:

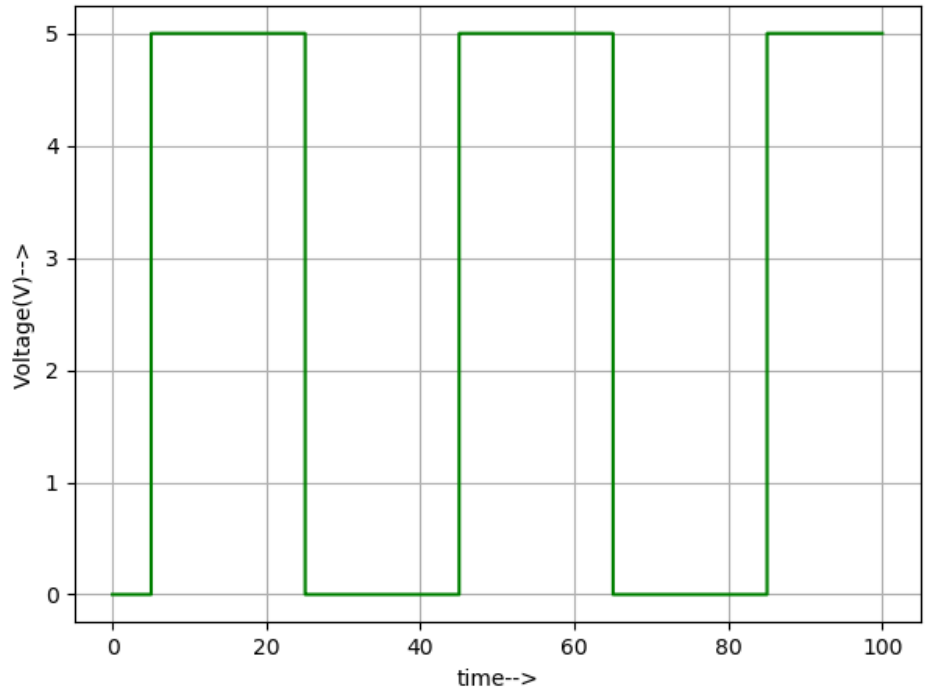
CLK


Voltage(V)-->
time-->
0
1
2
3
4
5
0
20
40
60
80
100

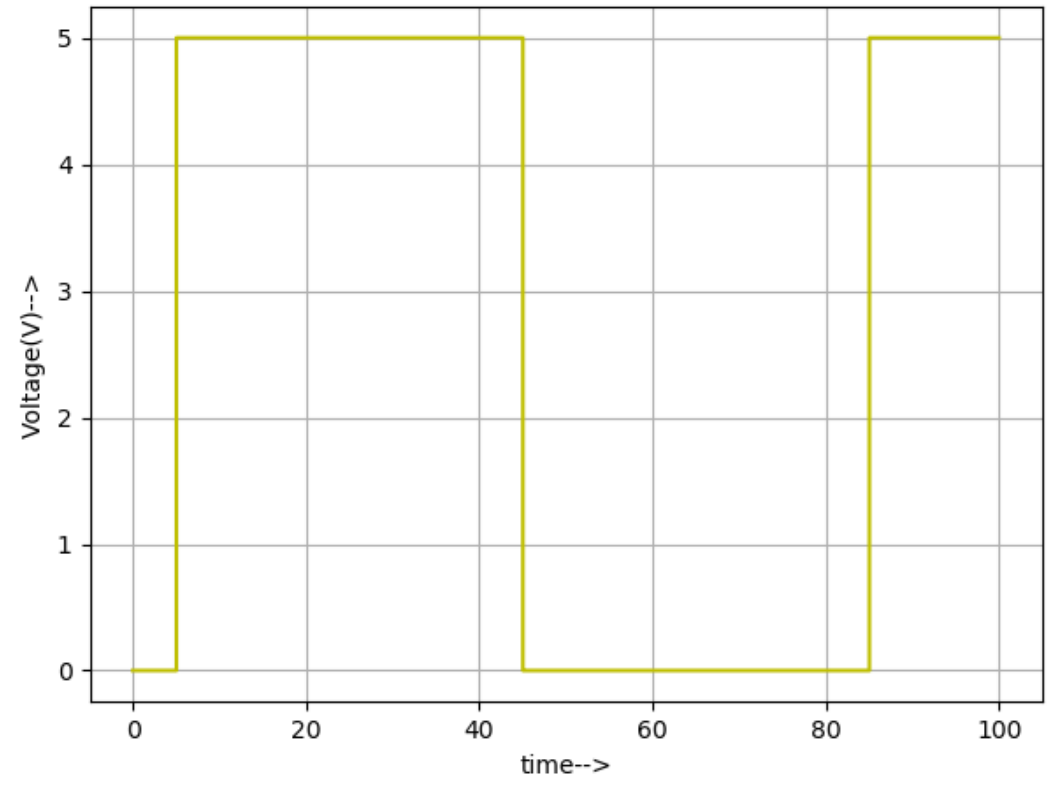
Q0


Voltage(V)-->
time-->
0
1
2
3
4
5
0
20
40
60
80
100

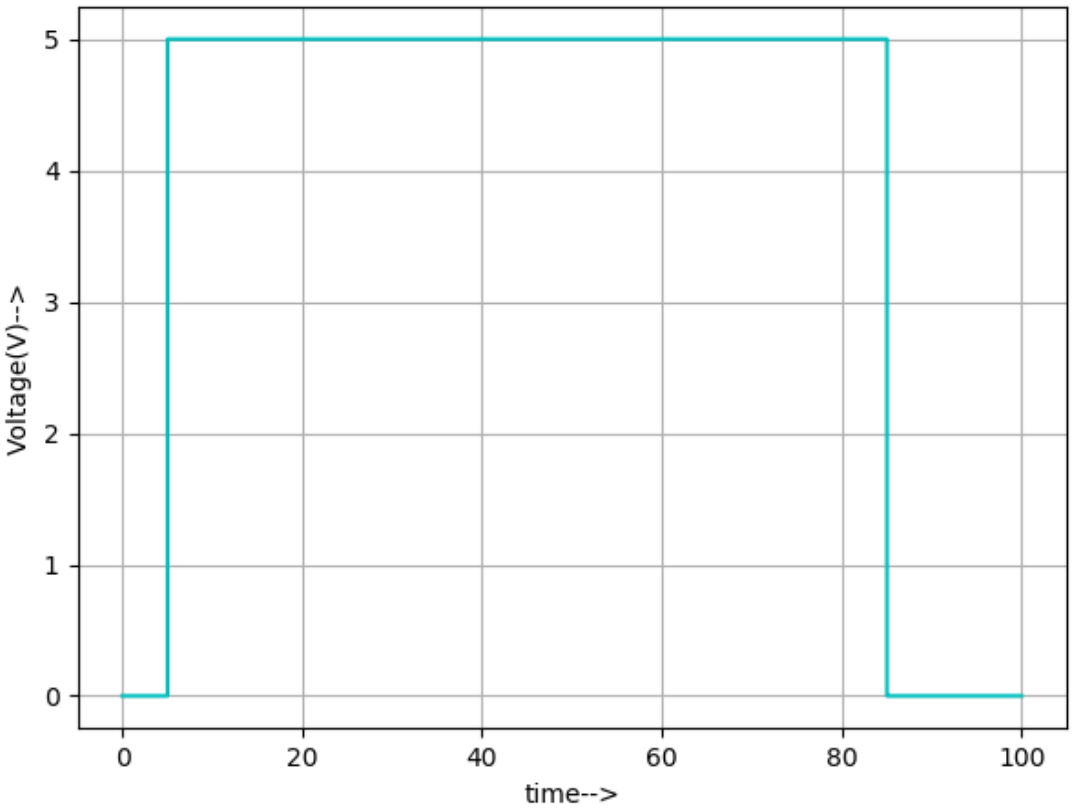
Q1


Voltage(V)-->
time-->
0
1
2
3
4
5
0
20
40
60
80
100

Q2


Voltage(V)-->
time-->
0
1
2
3
4
5
0
20
40
60
80
100

Q3



REFERENCES:

https://www.geeksforgeeks.org/asynchronous-down-counter/